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Bridging the gap between design and simulation of MOS circuits:

Implementation of the ACM model in Cadence and the associated extraction of parameters

Florianópolis
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Implementation of the ACM model in Cadence and the associated extraction of parameters

O presente trabalho em nível de mestrado foi avaliado e aprovado por banca examinadora composta pelos seguintes membros:

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Certificamos que esta é a **versão original e final** do trabalho de conclusão que foi julgado adequado para obtenção do título de mestre em Engenharia Elétrica.

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Orientador

Florianópolis, 2021.

To my parents Sheila and Antonio Cesar, my sister Pamela and her lovely children Julia, Pedro (*in memoriam*) and Maya.

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I find it fascinating that you can look at the same problem from different perspectives and approach it using different methods.

Maryam Mirzakhani

RESUMO

Modelos compactos do MOSFET são essenciais para o projeto e simulação de circuitos integrados. O modelo BSIM é amplamente utilizado em ferramentas EDA para executar simulações de circuitos MOS. Sua complexidade, tanto no que se refere ao grande número de parâmetros quanto a seus significados, no entanto, abre uma lacuna entre a simulação de circuito e o projeto executado pelo projetista, tornando difícil entender como os principais parâmetros do MOSFET se relacionam com os resultados finais. Para facilitar o entendimento do projetista quanto aos principais parâmetros que intervêm no projeto, este trabalho propõe um modelo simplificado do MOSFET, baseado no modelo *Advanced Compact MOSFET* (ACM), contendo apenas 4 parâmetros. A extração dos 4 parâmetros do modelo é realizada através de simulações automatizadas no simulador Cadence® Virtuoso®. Finalmente, para preencher a lacuna entre projeto e simulação, o modelo de 4 parâmetros foi implementado em Verilog-A para simular diferentes circuitos projetados com base no modelo ACM. Quatro circuitos foram simulados: inversor CMOS, oscilador em anel, fonte de corrente autopolarizada (SBCS) e amplificador de baixo ruído (LNA). Os resultados de simulação são apresentados e comparados com os resultados obtidos com o modelo BSIM. O modelo de 4 parâmetros destina-se, principalmente, à modelagem para ultra-baixa tensão (ULV) porque os efeitos secundários suprimidos não são tão acentuados no domínio ULV, o qual abrange pesquisas sobre aplicações de colheita de energia, redes de sensores para a Internet das Coisas e circuitos *always-on*.

Palavras-chave: Modelo ACM. Extração de parâmetros. Simulação de circuitos.

RESUMO EXPANDIDO

INTRODUÇÃO

Modelos MOSFET compactos são essenciais para o projeto e simulação de circuitos integrados. Os modelos de hoje começaram a ser desenvolvidos na década de 1960, quando só existiam dispositivos de canal longo. Com o avanço nas tecnologias de semicondutores, os dispositivos reduziram em tamanho e, consequentemente, os efeitos de canal curto passaram a interferir mais intensamente nos circuitos e, consequentemente, a afetar o projeto de forma mais significativa. Para mitigar o problema, esses efeitos foram incluídos nos modelos já existentes. O modelo de 4 parâmetros apresentado neste trabalho destina-se, principalmente, à modelagem para ultrabaixa tensão (ULV) porque os efeitos secundários suprimidos não são tão acentuados no domínio ULV, o qual abrange pesquisas sobre aplicações de colheita de energia, redes de sensores para a Internet das Coisas e circuitos *always-on*.

OBJETIVOS

O modelo BSIM é amplamente utilizado em ferramentas EDA para executar simulações de circuitos MOS. Sua complexidade, no entanto, abre uma lacuna entre a simulação de circuito e o projeto feito pelo projetista, tornando difícil entender como os principais parâmetros do MOSFET se relacionam com os resultados finais. Para mitigar a questão, propõe-se, neste trabalho, um modelo de 4 parâmetros baseado no modelo *Advanced Compact MOSFET* (ACM) para projetar e simular circuitos no simulador Cadence® Virtuoso®. O modelo também é utilizado para extrair cada um dos quatro parâmetros: a corrente específica, tensão de limiar, fator de rampa e fator de redução da barreira induzida pelo dreno (DIBL).

METODOLOGIA

Este trabalho introduz o modelo de 4 parâmetros e aborda como extrair cada parâmetro através de simulações automatizadas no simulador Cadence® Virtuoso®. Para preencher a lacuna entre projeto e simulação, o modelo de 4 parâmetros foi implementado em Verilog-A para simular diferentes circuitos projetados com base no modelo ACM. Quatro circuitos foram simulados: inversor CMOS, oscilador em anel, fonte de corrente autopolarizada (SBCS) e amplificador de baixo ruído (LNA). Os resultados de simulação são então apresentados e comparados com os do BSIM.

RESULTADOS E DISCUSSÃO

Nas simulações a nível de circuito, os resultados do ACM foram consistentes com os do BSIM. Os resultados do inversor CMOS, por exemplo, demonstraram que o modelo ACM para todas as regiões, assim como o modelo aproximado para inversão fraca podem ser utilizados para descrever o mesmo circuito com tensões de alimentação $V_{DD} < 300\,mV$. Sobretudo, esses modelos muito mais simples que o BSIM e mais próximos ao projetista resultaram em curvas semelhantes às do BSIM, cujas maiores diferenças ocorreram ao se calcular o ganho do inversor. O oscilador em anel foi utilizado para testar e avaliar o modelo dinâmico implementado. Os resultados evidenciaram o peso que as capacitâncias extrínsecas apresentam na frequência de oscilação. A experiência de simular o SBCS ilustrou a importância de se ter mais de um modelo em mãos para simulações de circuitos. A discrepância entre BSIM e ACM na ocasião alertou para a verificação do erro na simulação, porém, em geral, os resultados obtidos foram satisfatórios. Por fim, para testar simulação no domínio da frequência, o LNA simulado com modelo ACM também apresentou resultados consistentes com o LNA simulado utilizando BSIM.

CONSIDERAÇÕES FINAIS

Há espaço para melhorias, porém, a proposta deste trabalho era introduzir um modelo minimalista, mas realista no simulador. Um modelo que exigia apenas 4 parâmetros para funcionar, o que, no geral, foi realizado. Existem duas direções para seguir a partir deste trabalho: otimizar o modelo para o domínio ULV, que apresenta um grande campo de aplicações e espaço para inovações; e incluir dois parâmetros extras para modelar o ganho intrínseco, o que permitiria obter uma única equação que inclui o efeito de velocidade de saturação.

Este trabalho em si constitui uma coletânea de anos de estudo árduo e pesquisas resumidas em uma única peça, que apresenta como ir do projeto à simulação, ao mesmo tempo em que permite ao projetista extrair os parâmetros necessários por meio de simulações automatizadas, demonstrando e preenchendo, enfim, a lacuna entre o projeto e a simulação utilizando o modelo ACM de 4 parâmetros, conforme o título desta dissertação.

ABSTRACT

Compact MOSFET models are essential for design and simulation of integrated circuits. The BSIM model is widely used in EDA tools to run MOS circuit simulations. However, its complexity, regarding the huge number of parameters and their meanings, opens a gap between circuit simulation and hands-on design, making it hard to understand how the main MOSFET parameters are related to the simulation results. In order to assist the designer in understanding how the main MOSFET parameters affect the design, this work proposes a simplified MOSFET model, based on the *Advanced Compact MOSFET* (ACM) model, which contains only 4 parameters that are extracted through automated simulation setups on Cadence® Virtuoso® simulator. Finally, to bridge the gap between design and simulation, the 4-parameters model was implemented in Verilog-A to simulate different circuits designed with basis on the ACM model. To test the appropriateness of our proposal, four circuits (a CMOS inverter, a ring oscillator, a self-biased current source (SBCS) and a low-noise amplifier (LNA)) were simulated, either using the 4-parameter ACM model or the BSIM model. The simulation results demonstrate that the 4-parameter model is mostly suitable for ultra-low voltage (ULV) modeling. This is because some of the secondary effects not included in the 4-parameter model are not so accentuated in the ULV domain, which comprises applications such as energy harvesting, sensor nodes for the Internet of Things and always-on circuits.

Keywords: ACM model. Parameter extraction. Circuit simulation.

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LIST OF ABBREVIATIONS AND ACRONYMS

AC – Alternating Current

ACM – Advanced Compact MOSFET

AHDL – Analog Hardware Description Language

BSIM - Berkeley Short-Channel Insulated gate field-effect transistor Model

CMOS - Complementary MOS

CSIG – Common Source Intrinsic Gain

DC – Direct Current

DIBL – Drain-Induced Barrier Lowering

EDA – Electronic Design Automation

HDL – Hardware Description Language

IC – Integrated Circuit

IoT – Internet of Things

LNA – Low-Noise Amplifier

LV – Low-Voltage

MI – Moderate Inversion

MOS – Metal-Oxide-Semiconductor

MOSFET – MOS Field Effect Transistor

NMOS – N-Channel MOS

PMOS – P-Channel MOS

SBCS – Self-Biased Current Source

SI – Strong Inversion

SPICE – Simulation Program with Integrated Circuit Emphasis

UCCM – Unified Charge-Control Model

UICM – Unified Current-Control Model

ULV – Ultra-Low Voltage

VHDL – Very high-speed integrated circuit HDL

VTC – Voltage Transfer Characteristic

WI – Weak Inversion

LIST OF SYMBOLS

α	Channel linearity factor
μ_n	electron mobility
μ_p	Hole mobility
σ	DIBL factor
ϕ_t	Thermal voltage
ω	Radian frequency
A_{eff}	Effective junction area
A_V	Voltage gain
$A_{V,CS}$	Common source intrinsic gain
C_{bd}	Bulk-drain intrinsic capacitance
C_{bde}	Bulk-drain extrinsic capacitance
C_{bs}	Bulk-source intrinsic capacitance
C_{bse}	Bulk-source extrinsic capacitance
C_f	Fringing capacitance
C_{gb}	Gate-bulk intrinsic capacitance
C_{gd}	Gate-drain intrinsic capacitance
C_{gde}	Gate-drain extrinsic capacitance
$C_{go(gl)}$	Overlap capacitances in BSIM
C_{gs}	Gate-source intrinsic capacitance
C_{gse}	Gate-source intrinsic capacitance
C_{jb}	Unit-area bottom junction capacitance
C_{jbsw}	Unit-length junction sidewall capacitance along the isolation edge
C_{jbswg}	Unit-length junction sidewall capacitance along the gate edge
C_L	Load capacitance

C_{ox}	Oxide capacitance
C'_{ox}	Oxide capacitance per unit area
C_{sde}	Source-drain extrinsic capacitance
f_{ACM}	Oscillation frequency by ACM model
f_{BSIM}	Oscillation frequency by BSIM
f_0	Center frequency
f_t	Transition frequency
f_u	Unity-gain frequency
g_m	Gate transconductance
g_{mb}	Bulk transconductance
g_{md}	Drain transconductance
g_{ms}	Source transconductance
g_o	Output transconductance
I_D	Drain current
I_F	Forward current
i_f	Normalized forward current or forward inversion level
I_R	Reverse current
i_r	Normalized reverse current or reverse inversion level
I_S	Specific current
I_{SH}	Sheet normalization current
L	Transistor channel length
n	Slope factor
P_{eff}	Effective junction perimeter
q'_{ID}	Normalized reverse charge density
q'_{IS}	Normalized forward charge density

Q'_F	Forward charge density
Q_I	Total inversion channel charge
Q'_R	Reverse charge density
S	Transistor aspect ratio
V_B	Bulk voltage
V_D	Drain voltage
V_{DB}	Drain to bulk voltage
V_{DD}	Power supply voltage
V_{DS}	Drain to source voltage
V_G	Gate voltage
V_{GB}	Gate to bulk voltage
V_P	Pinch-off voltage
V_S	Source voltage
V_{SB}	Source to bulk voltage
V_{T0}	Threshold voltage
v_i	Small-signal input voltage
v_b	Small-signal bulk voltage
v_d	Small-signal drain voltage
v_g	Small-signal gate voltage
v_o	Small-signal output voltage
v_s	Small-signal source voltage
W	Transistor channel width

CONTENTS

1 INTRODUCTION

It all started as a course project named “Implementation of the ACM model in Cadence”. It was the last course I would take during my masters and as I dove deeper into the subject, not only did I learn more about the ACM model and how to use it, but also, I discovered that it is a lifetime worth of work.

1.1 WHEN IT ALL STARTED?

It was the beginning of the 1960’s when the first silicon Integrated Circuits (IC) were developed. At the time, unlike discrete component circuits, which could be verified and corrected by trial and error, the out-of-specification integrated circuit had to go through many processes to be corrected, resulting in waste of resources, materials, and the increase of the IC’s time-to-market. The need for a new and better design approach, along with the availability of powerful scientific computers, led to efforts in research laboratories around the world, targeting at the development of computer circuit simulation programs and compact transistor models to describe the circuits’ electrical behavior. Intended for circuit simulation, compact models comprise mathematical equations that “describe the current and charge behavior of semiconductor devices as a function of voltage, process, electrical, environment and geometry parameters” [1].

The accuracy of a circuit simulation depends not only on the algorithm but also on the representation of the devices; thus, the reliability of a simulation result is dependent of the correctness of the device model used. Since the late 60’s, several models appeared throughout the years following different approaches. One of them, the threshold voltage approach for MOSFET modeling, describes two operating regions, namely, weak inversion and strong inversion. Mathematical smoothing functions are employed to bridge these two regions. SPICE (Simulation Program with Integrated Circuit Emphasis) models adopted this approach from its very beginning. BSIM4, which is a modern version of the threshold voltage-based model, was developed in Berkeley. BSIM, which consists of a very complex model to describe the MOSFETs, has been used in state-of-the-art EDA tools since the 1980’s to run MOS circuit simulations. [1]

The surface potential and inversion charge-based models are part of the charge control models introduced in the 1980’s. Models SP, MOS model 11 and HiSIM are examples of

surface potential-based models, while ACM, EKV and BSIM5 are examples of inversion charge-based models. [2]

1.2 WHY ACM?

Compact MOSFET models are essential for design and simulation of integrated circuits. And while BSIM is widely used in EDA tools to run MOS circuit simulations, its complexity, however, opens a gap between circuit simulation and the hands-on design, making it hard to understand how the main MOSFET parameters relate to the final results. Thus, it becomes interesting to implement inversion charge-based models in simulators as they are strongly based on physics.

Therefore, this work proposes a 4-parameter model based on the Advanced Compact MOSFET (ACM) model, which can be applied for design in all regions of operation. The authors in [3] explain the ACM model and how to design various analog MOS circuits based on the model.

To bridge the gap between design and simulation, the 4-parameter model was implemented in the available simulator to simulate different circuits designed based on the ACM model.

1.3 HOW TO IMPLEMENT THE ACM MODEL IN SIMULATOR?

There are at least four different methods to implement compact models in simulators. Table 1.1, extracted from [4], summarizes these different methods alongside their advantages and drawbacks.

In [5] and [6], there was limited access to the inner workings of the available simulators, thus the ACM model was implemented through macro models. In [5], the simulator presented a tool to facilitate the implementation of the model which made the use restricted to that simulator.

The goal in this work is to easily implement the ACM model in the commercial Cadence® Virtuoso® simulator, which implements BSIM4 through the propriety interface method, consequently, not public.

Table 1.1. Methods to implement compact models in simulators, extracted from [4]

Type	Advantage	Disadvantage
Macro model	Simple Portable	Limited to available primitives
Propriety interface	Powerful Fast	Need access to simulator Not portable
Public interface	Reasonably powerful	Usually missing some capability Not portable Unique complexity Slow
AHDLs (Verilog-A)	Simple Powerful Portable	Language has some restrictions

Behavioral models, which are described through hardware description languages (HDLs) such as Verilog and VHDL, present the advantage of interchangeability with different simulators. They were developed to provide various levels of behavioral modeling abstractions to designers [4]. Verilog-A is simple, powerful, and targeted at analog hardware modeling due to its compact language, unlike VHDL that requires more lines of code.

Therefore, in this work, the 4-parameter model was implemented using the Verilog-A description language to easily simulate circuits using the ACM model in the Cadence® Virtuoso® simulator.

1.4 WHY 4 PARAMETERS?

Since the universe can be defined by just six numbers [7], 4 parameters could be enough to describe a transistor.

In the 1960's, MOS models were developed for the long channel transistors existent at that period. Through the scaling of semiconductor technologies, short-channel effects started to play a more important role in the performance of the designed circuits; consequently, short-channel effects were included in the existing models. The drain-induced barrier lowering (DIBL), velocity saturation and channel length modulation are examples of short-channel effects.

The DIBL factor completes the 4-parameter model (4PM) presented herein, alongside the specific current, threshold voltage and slope factor to describe MOS transistors using the ACM model.

The 4-parameter model is a minimalist yet more realistic model than the one with only 3 parameters; however, the suppressed secondary effects still affect the model's accuracy. The proposed model is mostly intended for low-voltage (LV) and ultra-low voltage (ULV) modeling because the suppressed secondary short-channel effects are not so accentuated on these domains.

In this work, voltages from 200 mV to 1/3 of the technology nominal voltage of operation (in this case 600 mV) corresponds to the LV domain, while sub-200 mV corresponds to the ULV domain.

Why?

In 1972, Swanson and Meindl [8] pointed out that the lowest supply voltage for proper operation of the CMOS inverter was, approximately, $8\phi_t = 200\,mV$ at room temperature (ϕ_t is the thermal voltage). However, in the 2000's, sub-200 mV circuits [9] began to emerge, introducing the ultra-low voltage (ULV) domain.

Energy harvesting sources are a solution to power batteryless devices. Solar cells [10] are popular energy harvesters and provide voltages around 300 mV up to 700 mV under low-intensity ambient light, which corresponds to the designated LV domain herein.

To this day, LV and ULV circuits fascinate the research community [11] from energy harvesting applications [12], to sensor nodes for the Internet of Things (IoT) [13], and always-on circuits [14].

1.5 HOW TO DETERMINE THE 4 PARAMETERS?

Besides the model implementation, determining the correct MOSFET parameters is fundamental for the analysis, design, and simulation of a MOS circuit. Besides a good model, the accuracy of the transistor characteristics is highly dependent on the values of its main parameters. Therefore, extraction methods are introduced to determine the four parameters. These methods, which are automated in the simulator for faster and easier extraction, can be transposed to different simulators.

1.6 SUMMING UP…

This dissertation is organized as follows: Chapter 2 presents the methodology and resources used throughout the work. Chapter 3 briefly introduces the ACM model, the small-signal transconductances and the transistor dynamic model. Chapter 4 describes the parameter extraction methods and how they were automated in the simulator. Chapter 5 presents the steps taken throughout the process of implementing the ACM models in Verilog-A and the resulting current-to-voltage (I-V) characteristics for single transistors. Chapter 6 consists of circuit level simulations, including a CMOS inverter, a ring oscillator, a self-biased current source (SBCS) and a low-noise amplifier (LNA).

By the end of this work, we hope to have finally bridged the gap between design and simulation.

2 METHODOLOGY

This chapter introduces the 4-parameter model and addresses how to extract each parameter through automated simulation setups on the Cadence® Virtuoso® simulator. To bridge the gap between design and simulation, the 4-parameter model was implemented in Verilog-A to simulate different circuits designed with basis on the ACM model. For each different transistor employed, the four parameters had to be extracted before running the simulation. Four circuits were simulated: a CMOS inverter, a ring oscillator, a self-biased current source (SBCS) and a low-noise amplifier (LNA). The simulation results were evaluated and compared with those obtained using the BSIM model.

2.1 RESOURCES

The main resources required for the development of this work were:

a. Books, dissertation theses and scientific papers which can be found in the References Section.

b. MATLAB®, licensed version provided by the university, employed for calculations and most of the images in this work.

c. CMOS 0.18 μm technology from TSMC.

d. Cadence® Virtuoso® EDA tool, also licensed to the university, with the BSIM4 model therein. Some of its features used in this work are the Schematic Editor, where the circuits were implemented and the ADE-L launched from the Schematic editor to configure simulations, which enabled to automate the extraction methods. The Visualization and Analysis XL displays the output signals and expressions, allowing for evaluation of the results without requiring switching programs. The Calculator was crucial for the automation part, since it is a tool with plenty of mathematical expressions and useful functions that can be used both in Visualization and Analysis as well as in ADE-L.

3 THE 4-PARAMETER MODEL

The Advanced Compact MOSFET (ACM) model, briefly introduced in this chapter, describes the electrical behavior of MOS transistors in all regions of operation.

The three main parameters of a MOSFET are the specific current I_S, the threshold voltage V_{T0} and the slope factor n, ideally equal to 1. Though these three parameters are enough to design circuits using the ACM model [3], to obtain more realistic results from simulations, the secondary effect called drain-induced barrier lowering (DIBL) completes the 4-parameter model.

The drain-induced barrier lowering effect occurs when "an increase in the drain voltage produces an increase in the surface potential in the channel and, consequently, it produces a reduction in the potential barrier seen by the electrons at the source" [3].

It has a stronger effect on short channel devices, however, to implement the ACM model for circuit simulations, DIBL cannot be ignored even for long channel transistors.

3.1 A DESIGN-ORIENTED MOSFET MODEL

Figure 3.1 presents the symbol of an n-channel MOSFET and its four terminals: gate (G), source (S), drain (D) and bulk (B). Appendix A presents the ACM model for a PMOS transistor.

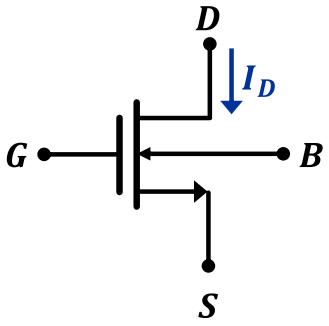

Figure 3.1. Symbol of the NMOS transistor

In the Advanced Compact MOSFET (ACM) model [3], the drain current I_D that flows through a long channel NMOS transistor, illustrated in Figure 3.1, has two components: the forward current I_F and the reverse current I_R, both dependent on the voltage V_{GB} between the gate and bulk terminals. In addition, I_F depends on the voltage V_{SB} between source and bulk,

whereas I_R depends on the voltage V_{DB} between drain and bulk. This source-drain symmetry is depicted in (3.1).

$$I_D = I_F - I_R = I(V_{GB}, V_{SB}) - I(V_{GB}, V_{DB}) = I_S\left(i_f - i_r\right) \tag{3.1}$$

The specific (or normalization) current I_S is dependent on geometry an technological parameters as given by (3.2), where μ_n is the NMOS carrier mobility, C'_{ox} is the oxide capacitance per unit area, ϕ_t is the thermal voltage and n is the slope factor. The aspect ratio S is the ratio of the width W to the length L of the transistor channel.

In a first order approximation, the technological parameters can be comprised in one factor denominated the sheet normalization current I_{SH}, which is slightly dependent on V_G through μ_n and n.

$$I_S = \mu_n C'_{ox} n \frac{\phi_t^2}{2} \frac{W}{L} = I_{SH} \frac{W}{L} = I_{SH} S \tag{3.2}$$

The normalized form of the unified charge-control model (UCCM), expressed in (3.3), establishes the relationship between the voltages at the device terminals and the normalized inversion charge density at the source (drain) $q'_{IS(D)}$.

$$\frac{V_P - V_{S(D)B}}{\phi_t} = q'_{IS(D)} - 1 + \ln q'_{IS(D)} \tag{3.3}$$

$$q'_{IS(D)} = \sqrt{1 + i_{f(r)}} - 1 \tag{3.4}$$

Using equation (3.4) in (3.3) gives the unified current-control model (UICM), expressed in (3.5), which establishes the relationship between the voltages at the device terminals and the forward (reverse) inversion levels $i_{f(r)}$. As a rule of thumb [3], the transistor operates in weak inversion (WI) up to $i_f = 1$ and in strong inversion (SI) for $i_f > 100$. The intermediate values of i_f, from 1 to 100, characterize moderate inversion (MI).

The pinch-off voltage V_P can be approximated by (3.6), where V_{T0} is the equilibrium threshold voltage that corresponds to the gate voltage for which $V_P = 0$, and σ is the magnitude of the DIBL factor.

$$\frac{V_P - V_{S(D)B}}{\phi_t} = \sqrt{1 + i_{f(r)}} - 2 + \ln\left(\sqrt{1 + i_{f(r)}} - 1\right) \tag{3.5}$$

$$V_P = \frac{V_{GB} - V_{T0} + \sigma V_{DB} + \sigma V_{SB}}{n} \tag{3.6}$$

Once familiarized with the model, the four transistor parameters can be extracted using the UICM and its derivatives.

3.1.1 Small-signal transconductances

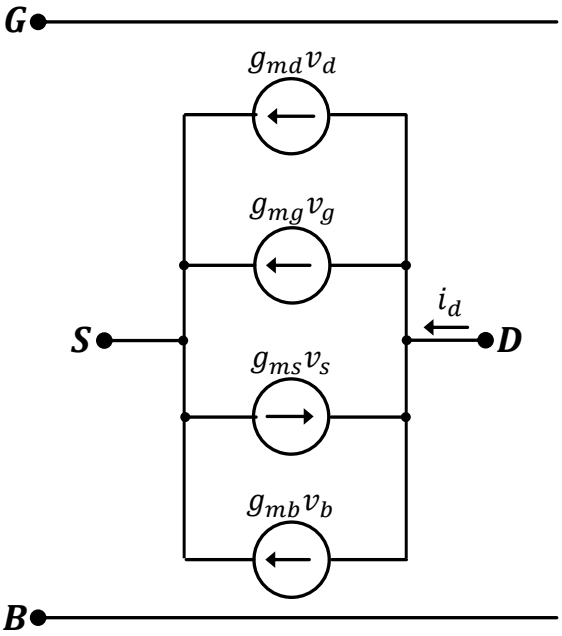

Figure 3.2. Low-frequency small-signal model of the MOSFET

Figure 3.2 presents the low-frequency small-signal model for MOSFET transistors, in which the variation of the drain current is expressed by (3.7), where g_{mg}, g_{ms}, g_{md} and g_{mb} are, respectively, the gate, source, drain and bulk small-signal transconductances given by (3.8);v_g, v_s, v_d and v_b represent the small variations in the gate, source, drain and bulk voltages.

$$i_d = g_{mg}v_g - g_{ms}v_s + g_{md}v_d + g_{mb}v_b \tag{3.7}$$

$$g_{mg} = \frac{\partial I_D}{\partial V_G}, \qquad g_{ms} = -\frac{\partial I_D}{\partial V_S}, \qquad g_{md} = \frac{\partial I_D}{\partial V_D}, \qquad g_{mb} = \frac{\partial I_D}{\partial V_B} \tag{3.8}$$

The relationship between the transconductances and the inversion levels are obtained by applying the partial derivatives of (3.8) to the UICM along with (3.1). Appendix B presents the transconductances in all regions of operation.

Based on Appendix B, the transconductance-to-current ratio in terms of the inversion level are given by expressions (3.9), (3.10) and (3.11), in which $I_{D,sat}$ stands for the approximation of the drain current in the saturation region, where $i_r \ll i_f$ [3].

$$\phi_t \frac{g_{ms}}{I_{D,sat}} = \left(1 - \frac{\sigma}{n}\right) \frac{2}{\left(\sqrt{1 + i_f} + 1\right)} \tag{3.9}$$

$$\phi_t \frac{g_{md}}{I_{D,sat}} = \frac{\sigma}{n} \frac{2}{\left(\sqrt{1 + i_f} + 1\right)} \tag{3.10}$$

$$\phi_t \frac{g_m}{I_{D,sat}} = \frac{1}{n} \frac{2}{\left(\sqrt{1 + i_f} + \sqrt{1 + i_r}\right)} \tag{3.11}$$

The main and most used transconductance of the MOSFET is the gate transconductance g_{mg}, which, from now on, will be referred to as g_m as in (3.11). In addition, differently from (3.9) and (3.10), $g_m/I_{D,sat}$ in (3.11) does not depend on the DIBL factor σ. The small-signal transconductances are essential for the design of integrated circuits and will be constantly referred to.

3.2 DYNAMIC MODEL

The dynamic model of MOS transistors includes intrinsic and extrinsic capacitances. Figure 3.3 shows the idealized MOS transistor with its intrinsic (in red) and extrinsic parts. The overlap capacitances due to the unavoidable overlap between the gate, source and drain diffusions (in yellow), along with the fringing capacitances (C_F) compose the extrinsic capacitance $C_{gse(de)}$, as shown in Figure 3.4(a). The substrate-source and substrate-drain junctions modeled by (nonlinear) diode capacitances correspond to $C_{bse(de)}$. A more complete model for the extrinsic part should include parasitic resistances as well [15].

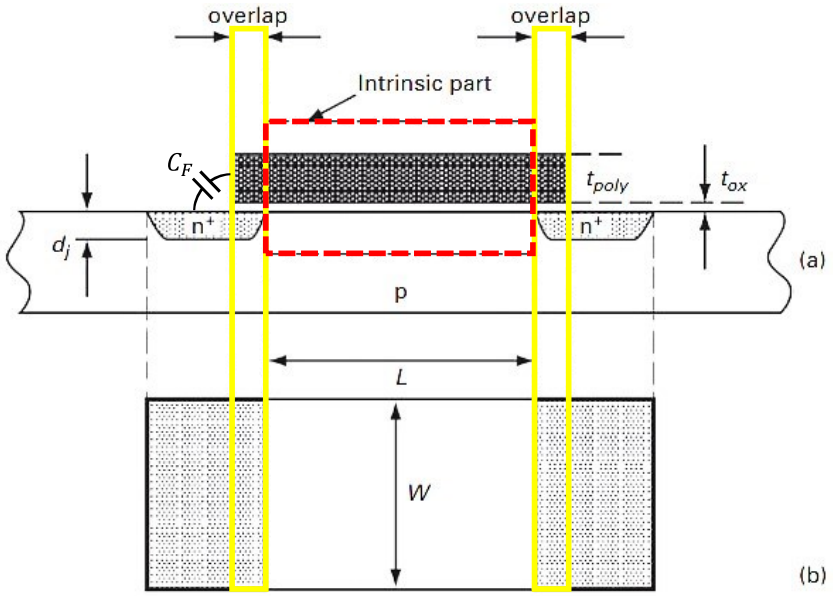

Figure 3.3 Idealized MOS transistor showing the intrinsic and extrinsic parts. (a) cross-section, (b) top view. Adapted from [15].

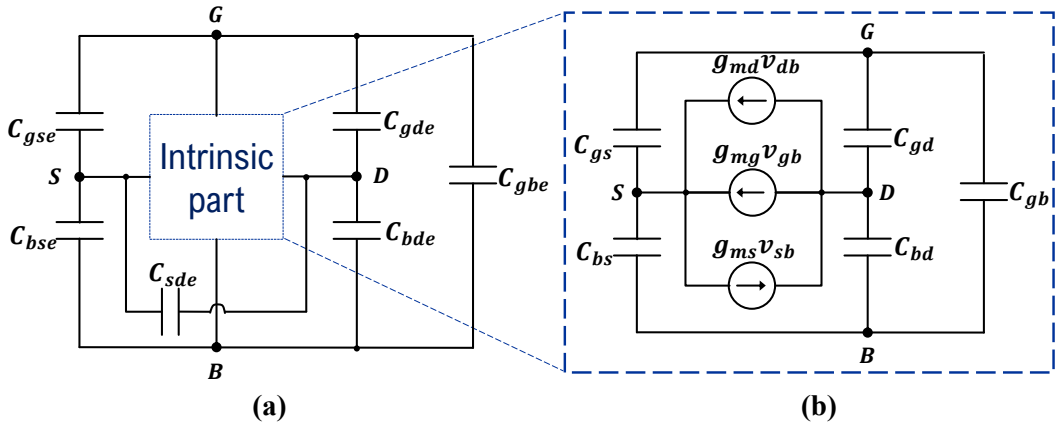

Figure 3.4. MOSFET dynamic model with (a) extrinsic and (b) intrinsic parts [2]

The field effect of MOS transistors occurs in the intrinsic part, between the source and drain (enclosed by a red line in Figure 3.3(a)). The classical MOSFET model in Figure 3.4 contains five capacitances and the small-signal transconductances of Figure 3.2 with the bulk as reference. The five intrinsic capacitances expressed by (3.12) – (3.16) [2], with channel linearity factor $\alpha = \frac{1+q'_{ID}}{1+q'_{IS}}$, do not include the DIBL effect, however, they were implemented in Verilog-A to describe the transistors' dynamic model. The inclusion of the DIBL effect in these five intrinsic capacitances is shown in Appendix C.

$$C_{gs} = \frac{2}{3} WLC'_{ox} \frac{(1+2\alpha)}{(1+\alpha)^2} \frac{q'_{IS}}{(1+q'_{IS})} \tag{3.12}$$

$$C_{gd} = \frac{2}{3} WLC'_{ox} \frac{\alpha^2+2\alpha}{(1+\alpha)^2} \frac{q'_{ID}}{(1+q'_{ID})} \tag{3.13}$$

$$C_{gb} = \frac{n-1}{n} (WLC'_{ox} - C_{gs} - C_{gd}) \tag{3.14}$$

$$C_{bs} = (n-1)C_{gs} \tag{3.15}$$

$$C_{bd} = (n-1)C_{gd} \tag{3.16}$$

4 PARAMETER EXTRACTIONS

Before introducing the implementation of the ACM model in Verilog-A, it is appropriate to learn how to determine the four parameters introduced in Chapter 3, since the accuracy of the transistor characteristics depends not only on a good model, but also on the values of its main parameters.

Parameter extraction methods are commonly used in laboratory experiments to characterize electronic devices. Reproducing these methods via simulation setups makes the automation of the extraction procedure simple and enables the extraction of MOSFET parameters when a test chip is not available for characterization.

For some designers it might seem a trivial task to recreate the methodology of a parameter extraction on a simulator, but the automation part can be time consuming if not familiarized with the simulator at hand. This chapter focuses on showing how the four-parameter extraction methods, described in literature by [16] – [17], were automated for simulations in Cadence® Virtuoso®. The g_m/I_D and $3I_S$ methods were used to extract I_{SH}, V_{T0} and n, while the delta and transconductance methods were used to extract the DIBL factor σ.

4.1 EXTRACTION OF I_{SH}, V_{T0} AND n

The objective of this section is to describe how the threshold voltage V_{T0}, specific current I_S and the slope factor n were extracted using the g_m/I_D characteristic and the $3I_S$ method in Cadence® Virtuoso® Simulator.

4.1.1The g_m/I_D method

Based on [16] and on Appendix B, the values of the threshold voltage and specific current are determined through the g_m/I_D characteristic written in (4.1), which is valid for all regions of operation.

$$\frac{g_m}{I_D} = \frac{1}{I_D}\frac{dI_D}{dV_G} = \frac{d(\ln I_D)}{dV_G} = \frac{2}{n\phi_t(\sqrt{1+i_f}+\sqrt{1+i_r})} \tag{4.1}$$

$$\frac{V_{DS}}{\phi_t} = \sqrt{1+i_f} - \sqrt{1+i_r} + \ln\left(\frac{\sqrt{1+i_f}-1}{\sqrt{1+i_r}-1}\right) \tag{4.2}$$

Expression (4.2) was obtained applying the UICM, expression (3.5), to the drain and to the source terminals The variation of the slope factor with the gate voltage is neglected, thus, for the channel under the threshold condition $i_f = 3$ and in the linear region with $V_{DS} = \frac{\phi_t}{2}$, expression (4.2) results in $i_r = 2.12$, for which V_{T0} corresponds to the gate voltage at which $\frac{g_m}{I_D} = 0.531\left(\frac{g_m}{I_D}\right)_{max}$, while I_S corresponds to $\frac{I_D}{0.88}$, where I_D is the drain current at $V_{GB} = V_{T0}$. The values used to determine V_{T0} and I_S are illustrated in Figure 4.1(b).

The DIBL factor σ does not appear in (4.2) because, in the linear region, short channel effects as DIBL, velocity saturation and CLM are not relevant. Thus, the model for long channel transistors is almost rigorously valid even for short-channel transistors, which highlights the greatest advantage of characterization in the linear region.

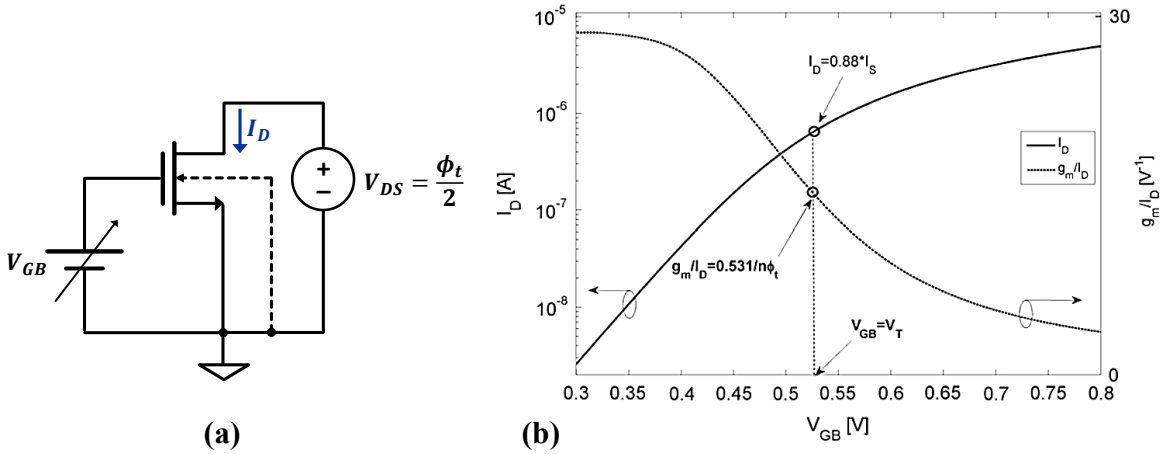

Figure 4.1. (a) Circuit to measure the g_m/I_D characteristic in the linear region; (b) experimental measurement of g_m/I_D and I_D as a function of V_{GB} with the annotated points to determine V_{T0} and I_S. Source: [16]

The circuit configuration to obtain the g_m/I_D characteristic is shown in Figure 4.1(a) and it was implemented in Virtuoso® Schematic Editor. Design variables *w_par* and *l_par* are assigned to the transistor's width and length parameters, respectively, to easily access and change their values directly in ADE-L. V_{GB} is the DC value of the voltage source connected to the transistor gate.

To implement the g_m/I_D method in ADE-L, the gate voltage V_{GB} was swept from 0.3 V to 0.8 V, which is a range wide enough to extract the 3 parameters of interest. The drain current is the main element to add from the Schematic Editor into the outputs in ADE-L.

For the NMOS transistor in common source configuration $V_S = V_B = 0$, whereas for a PMOS $V_S = V_B = 1\ V$, enough to turn on the transistor but not too high as to expand the sweep to a voltage higher than 1.8 V, the nominal supply voltage for 0.18 µm technology. As mentioned earlier in this section, to operate in the linear region, we have chosen $V_{DS} = \frac{\phi_t}{2}$, which is around 13 mV at 27°C.

The voltage V_{GB} (via design variable *vgb*) is varied from –0.3 to 1.8 V to ensure the maximum g_m/I_D is retrieved. The step size was set to 1 mV, since it must be small enough to avoid missing relevant points for the derivative calculation that follows, but not too small or the simulation can take a long time to complete.

To automate the g_m/I_D extraction method in ADE-L, the expressions listed in Table 4.1 were included in the outputs. These expressions were written with the help of the built-in Calculator tool in Virtuoso®. The method without any automation, *i. e*. without the Calculator tool, consists of exporting the $I_D\ vs. V_{GB}$ data to another mathematics software to calculate the $\frac{g_m}{I_D} = \frac{d(\ln I_D)}{dV_G}$ from (4.1) and determine V_{T0} and I_S graphically as in Figure 4.1(b).

Besides the output expressions, Table 4.1 also breaks down the g_m/I_D method into five steps associated with each output expression.

Table 4.1. Steps of the g_m/I_D extraction method and respective output expressions to automate the extraction of parameters V_{T0}, I_S and n in Virtuoso® ADE-L.

Step	Description	Output name in simulator	Expression written for output
I	Calculate g_m/I_D from I_D curve	*gmid*	*deriv(ln(i("/M0/D" ?result "dc")))*
II	Determine V_{T0}	*VT0*	*cross(gmid (0.531 * ymax(gmid)) 1 "falling" nil nil)*
III	Determine I_S	*IS*	*value(i("/M0/D" ?result "dc") VT0)* 1.136*
IV	Determine I_{SH}	*ISH*	*IS/S*, in which *S = (VAR("w_par") / VAR("l_par"))*
V	Determine the slope factor	*n*	*ymax(gmid)/phit*

In Table 4.1, *i("/M0/D" ?result "dc")* corresponds to the DC analysis result of the current at terminal *D*, the drain current I_D, of the transistor *M0* instanced on the Schematic Editor.

The *deriv()* function calculates the derivative of its argument in relation to the sweep variable, while the *ln()* function calculates the natural logarithm, both functions are used to calculate the $\frac{g_m}{I_D} = \frac{d(\ln I_D)}{dV_G}$ from (4.1). The *ymax()* function locates the maximum value in the y-axis, which is $\left(\frac{g_m}{I_D}\right)_{max}$.

The *cross()* function searches for a given value at the specified curve, finds its index, then outputs the value from the x-axis that matches to the same index. For this case, it determines the voltage V_{GB} at which $\frac{g_m}{I_D} = 0.531\left(\frac{g_m}{I_D}\right)_{max}$. When the maximum value is multiplied by a constant lower than 1, there will be the same value twice in a single curve, the "falling" option is meant to tell the Calculator which of the two values should be taken as the desired result..

The *value()* function works similarly to the cross function, but it finds the value in the y-axis, whereas the *cross()* function finds the value in the x-axis. The *value()* function returns the value of the specific current I_S for the determination of the normalization sheet current $I_{SH} = \frac{I_S}{S}$. The aspect ratio $S = \frac{W}{L}$ takes the values set for *w_par* and *l_par*; the *VAR()* function enables the use of design variables in the ADE-L outputs by writing them as arguments in quotes.

At last, the slope factor n can be extracted as $\left(\frac{g_m}{I_D}\right)_{max} \cong \frac{1}{n\phi_t}$, thus $n = \frac{1}{\max\left(\frac{g_m}{I_D}\right)\phi_t}$, as presented in Table 4.1.

4.1.2 The $3I_S$ method

Described in [18], the $3I_S$ method is a direct procedure which enables the extraction of V_{T0} and the slope factor n. For a long-channel transistor in saturation the reverse current is much lower than the forward current; thus, from the UICM in (3.5), for $i_f = 3$, the pinch-off voltage $V_P = V_{SB}$ and the drain current $I_D = 3I_S$.

Employed in this extraction method, the circuit configuration in Figure 4.2 enables to determine the dependence of V_P on the gate voltage V_{GB}. The specific I_S corresponds to the value extracted by the g_m/I_D method.

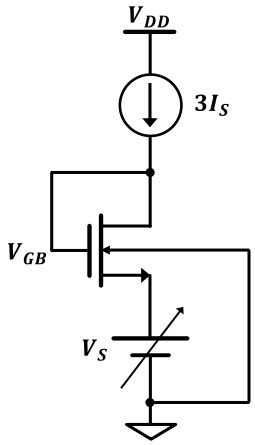

Figure 4.2. Circuit to measure the pinch-off voltage and extract the slope factor n as a function of V_{GB}

$$V_P = \frac{V_{GB} - V_{T0}}{n} \tag{4.3}$$

Expression (4.3) directly establishes that $V_{GB} = V_{T0}$ for $V_P = 0$. Since $V_P = V_{SB}$, then $V_P = 0$ for $V_S = V_B$. The slope factor as a function of V_{GB} is given by (4.4).

$$n = \left[\frac{dV_P}{dV_G}\right]^{-1} \tag{4.4}$$

To implement the $3I_S$ method in ADE-L, a DC analysis and sweep of the source voltage V_S must be run. The gate voltage is added from the Schematic Editor to the outputs in ADE-L. The voltage V_S is varied from –0.3 to 1.8 V with 1 mV step. For the NMOS transistor in diode configuration the bulk voltage $V_B = 0$, whereas for a PMOS $V_B = V_{DD}$.

To automate the $3I_S$ extraction method in ADE-L, the expressions listed in Table 4.2 were included in the outputs. As stated earlier, the threshold voltage obtained through this method corresponds to the gate voltage at which $V_P = V_{SB} = 0$, i.e., $V_S = V_B$. The slope factor is determined for the point at which $V_{GB} = V_{T0}$, since the simulation generates curves in relation to the sweep variable, in this case, V_S, then the slope factor is also found on $V_S = V_B$.

Table 4.2. Output expressions to automate the $3I_S$ extraction method in Virtuoso® ADE-L.

Description	Output	Expression
Threshold voltage	VT0	*value(v("/vgb" ?result "dc") VAR("vb"))*
Slope factor curve	slope_factor	*deriv(v("/vgb" ?result "dc"))*
Slope factor value @ $V_{GB} = V_{T0}$	n	*value(slope_factor VAR("vb"))*

4.1.3 Extraction results

Figure 4.3 and Table 4.3 summarize the results obtained through simulation of the described extraction methods for a long channel NMOS transistor of the 0.18 µm technology available. Figure 4.3(a) presents the g_m/I_D characteristic, consisting of the $I_D\ vs. V_{GB}$ and $\frac{g_m}{I_D} vs. V_{GB}$ curves on the same graph. Figure 4.3(b) presents $V_{SB} = V_P\ vs. V_{GB}$ and the slope factor $n\ vs. V_{GB}$.

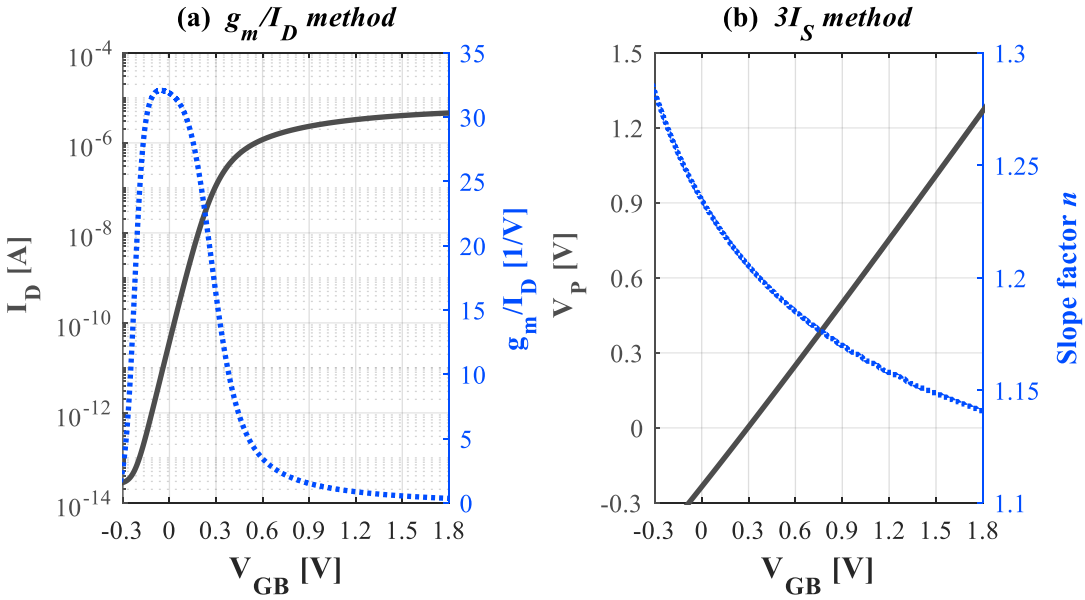

Figure 4.3. Results of (a) the g_m/I_D extraction method; (b) the $3I_S$ extraction method for a transistor with $\frac{W}{L} = \frac{1\ \mu m}{1\ \mu m}$ of the 0.18 µm technology

The results in Table 4.3 show that both methods are consistent and can be used for extraction. The threshold voltage value determined by the $3I_S$ method is coherent with the value determined in the g_m/I_D extraction method, however, with an error of 4 mV only. Short-channel effects affect the value of the threshold voltage determined by the $3I_S$ method since the transistor operates in saturation. For this reason, the value of V_{T0} is usually taken from the g_m/I_D procedure [16].

Table 4.3. Parameters extracted by the g_m/I_D and $3I_S$ methods

Method	Transistor	Long channel		Short channel	
		NMOS	**PMOS**	**NMOS**	**PMOS**
	$\boldsymbol{\frac{W}{L}}$	$\frac{1\ \mu m}{1\ \mu m}$	$\frac{1\ \mu m}{1\ \mu m}$	$\frac{1\ \mu m}{0.3\ \mu m}$	$\frac{1\ \mu m}{0.3\ \mu m}$
$\frac{g_m}{I_D}$	$\boldsymbol{I_{SH}}$ $\boldsymbol{[nA]}$	110	40	126	32
	$\boldsymbol{V_{T0}}$ $\boldsymbol{[mV]}$	291	-211	311	-240
	$\boldsymbol{n}$	1.19	1.17	1.23	1.18
$3I_S$	$\boldsymbol{V_{T0}}$ $\boldsymbol{[mV]}$	295	-212	309	-239
	$\boldsymbol{n}$	1.20	1.17	1.20	1.18

4.2 EXTRACTION OF DIBL FACTOR σ

The drain-induced barrier lowering (DIBL) is a short-channel secondary effect included in the ACM model through parameter σ. Ghibaudo presents in [17] an extraction method for the σ parameter which employs the gate and drain transconductance-to-current ratios; however "elegant", it is not an easy method to automate in simulation. Hence, this section describes two methods automated in Cadence® Virtuoso® Simulator to extract σ, namely the common source intrinsic gain method, and the $g_{md}/I_{D,sat}$ method.

4.2.1 Common Source Intrinsic Gain (CSIG) method

The drain-induced barrier lowering (DIBL) factor σ is a small-signal parameter which directly results in the intrinsic gain of the common source configuration. Figure 4.4 presents the common source topology and its equivalent small-signal model used to calculate the intrinsic gain.

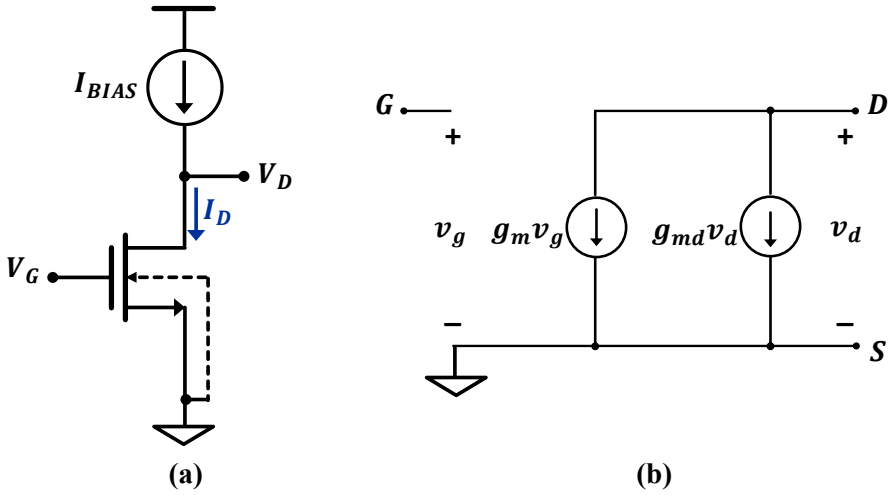

Figure 4.4. (a) Common source configuration and (b) equivalent small-signal model.

In saturation, the use of the transconductance-to-current characteristics (3.10) and (3.11) yields the common source intrinsic gain presented in (4.5) and (4.6).

$$A_{V,CS} = \frac{v_d}{v_g} = -\frac{g_m}{g_{md}} = -\frac{\frac{g_m}{I_{D,sat}}}{\frac{g_{md}}{I_{D,sat}}} = -\frac{\frac{1}{\phi_t}\left(\frac{1}{n}\right)\frac{2}{1+\sqrt{1+i_f}}}{\frac{1}{\phi_t}\left(\frac{\sigma}{n}\right)\frac{2}{1+\sqrt{1+i_f}}} \tag{4.5}$$

$$A_{V,CS} = -\frac{g_m}{g_{md}} = -\frac{1}{\sigma} \tag{4.6}$$

As shown in Figure 4.4, the drain terminal consists of an open circuit in AC to determine the intrinsic gain in the small-signal analysis, which is obtained by employing an ideal current source in DC.

To determine the common source intrinsic gain through simulation, an ideal operational amplifier (op-amp) was included to set the DC operating point required for the small-signal measurement. Figure 4.5 presents the circuit implemented in the Schematic Editor. The ideal op-amp was simulated by a voltage-controlled voltage source (VCVS) with infinite gain (it was used $gain = 10^6$).

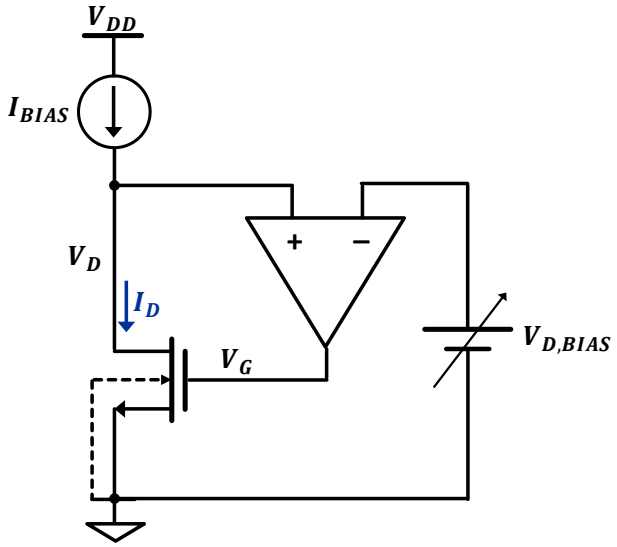

Figure 4.5. Circuit to determine the common source intrinsic gain in simulation.

A DC sweep on the voltage $V_{D,BIAS}$ forces $V_D = V_{D,BIAS}$ and varies V_G to keep $I_D = I_{BIAS}$. The variables *ibias* and *vdbias* were assigned to the constant current I_{BIAS} and the sweep voltage $V_{D,BIAS}$, respectively.

In ADE-L, I_{BIAS} was set to a subthreshold current equal to 10 nA. The saturation range of interest for the voltage sweep is from 0.2 to 1.0 V and the voltage step was set equal to ϕ_t.

The small variations in the gate and drain voltages, v_g and v_d, respectively, correspond to the difference between two operating points ΔV_G and ΔV_D, respectively, which leads to (4.7) and (4.8).

$$A_{V,CS} = \frac{v_d}{v_g} = \frac{\Delta V_D}{\Delta V_G} = -\frac{1}{\sigma} \tag{4.7}$$

$$\therefore \sigma = -\frac{\Delta V_G}{\Delta V_D} \tag{4.8}$$

Hence, the DIBL factor σ is obtained by measuring V_D and V_G and applying the derivative to obtain the small-signal variations (ΔV_G and ΔV_D). Since the step was set equal to ϕ_t, the variation $\Delta V_D = \phi_t$. Once ΔV_G and ΔV_D are calculated, σ is determined by (4.8). Table 4.4 summarizes the steps and output expressions employed for the method automation.

Table 4.4. Output expressions to automate the common source intrinsic gain method

Step	Description	Output in simulator	Expression written for output
I	Calculate ΔV_G	dVG	*deriv(v("/VG" ?result "dc"))*
	Calculate ΔV_D	dVD	*deriv(v("/VD" ?result "dc"))*
II	Calculate $\sigma = -\frac{\Delta V_G}{\Delta V_D}$	sigma	*- (dVD / dVG)*
III	Determine σ @ $V_{D,BIAS}$	sigma_value	*value(sigma VAR("vdbias"))*

In Table 4.4, *v("/VG" ?result "dc")* and *v("/VD" ?result "dc")* correspond to the DC analysis result of V_G and V_D, respectively. Although *vdbias* was employed as the sweep variable, the simulator demands the definition of a constant value to each variable independent of the analysis to be performed. Therefore, *vdbias* was also used to retrieve the value of σ at a specific $V_{D,BIAS}$. A $V_{D,BIAS} = 600\,mV$, which is equal to 1/3 of the technology nominal voltage, was chosen to correspond to a $V_{D,BIAS}$ in the low-voltage domain.

4.2.2 The $g_{md}/I_{D,sat}$ method

Another method to determine σ is to use the drain transconductance-to-current ratio, in saturation, presented in (3.10). As in the g_m/I_D method, the $g_{md}/I_{D,sat}$ relationship can be written as (4.9). For an inversion level $i_f \ll 1$, which corresponds to operation in WI, the parameter σ is determined by (4.10).

$$\frac{g_{md}}{I_{D,sat}} = \frac{1}{I_D}\frac{dI_D}{dV_D} = \frac{d(\ln I_D)}{dV_D} = \frac{\sigma}{n\phi_t}\frac{2}{\left(\sqrt{1+i_f}+1\right)} \tag{4.9}$$

$$\sigma = n\phi_t \frac{g_{md}}{I_{D,sat}} \tag{4.10}$$

The circuit configuration to obtain the $g_{md}/I_{D,sat}$ characteristic is shown in Figure 4.6 it was implemented in Virtuoso® Schematic Editor. The variables *vg* and *vd* were assigned to the DC value of the voltage source connected to the gate and drain, respectively.

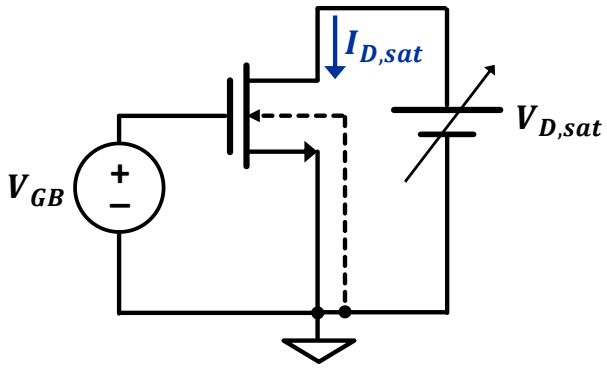

Figure 4.6. Circuit configuration to obtain $g_{md}/I_{D,sat}$ characteristic.

To implement the $g_{md}/I_{D,sat}$ method in ADE-L, a DC analysis and sweep of the drain voltage $V_{D,sat}$ must be run. The drain current is the main element to add from the Schematic Editor into the outputs in ADE-L.

Expression (4.10) is only true for a transistor operating in weak inversion. From the CSIG method, it was observed a gate voltage around 100 mV for a current of 10 nA, which corresponds to a WI current. Hence, $V_{GB} = 100\ mV$ was set.

The voltage $V_{D,sat}$ (via design variable *vd*) is varied from 0.2 to 1 V, selected as the saturation region of interest. As in the g_m/I_D method, the step size of $V_{D,sat}$was set to 1 mV.

Table 4.5 summarizes the steps and output expressions included in the outputs to automate the $g_{md}/I_{D,sat}$ method in ADE-L.

Table 4.5. Output expressions to automate the $g_{md}/I_{D,sat}$ method

Step	Description	Output	Expression
I	Calculate $\frac{g_{md}}{I_{D,sat}}$ from I_D curve	gmd_id	*deriv(ln(i("/M0/D" ?result "dc")))*
II	Calculate $\sigma = n\phi_t \frac{g_{md}}{I_{D,sat}}$	sigma	*gmd_id*n*phit*
III	Determine σ @ $V_{D,sat}$	sigma_value	*value(sigma VAR("vd"))*

In Table 4.5, *i("/M0/D" ?result "dc")* corresponds to the drain current I_D that results from the DC analysis. The slope factor n is a variable that corresponds to the value extracted by the $3I_S$ method. As in the CSIG method, *vd* was also used to determine the value of σ at a specific $V_{D,sat}$, which was chosen to be $V_{D,sat} = 600\ mV$.

4.2.3 Extraction results

Figure 4.7 and Figure 4.8 present the curves obtained through the common source intrinsic gain and $g_{md}/I_{D,sat}$ methods, respectively, for a short channel NMOS transistor with $\frac{W}{L} = \frac{1.0\ \mu m}{0.3\ \mu m}$ from the 0.18 µm technology.

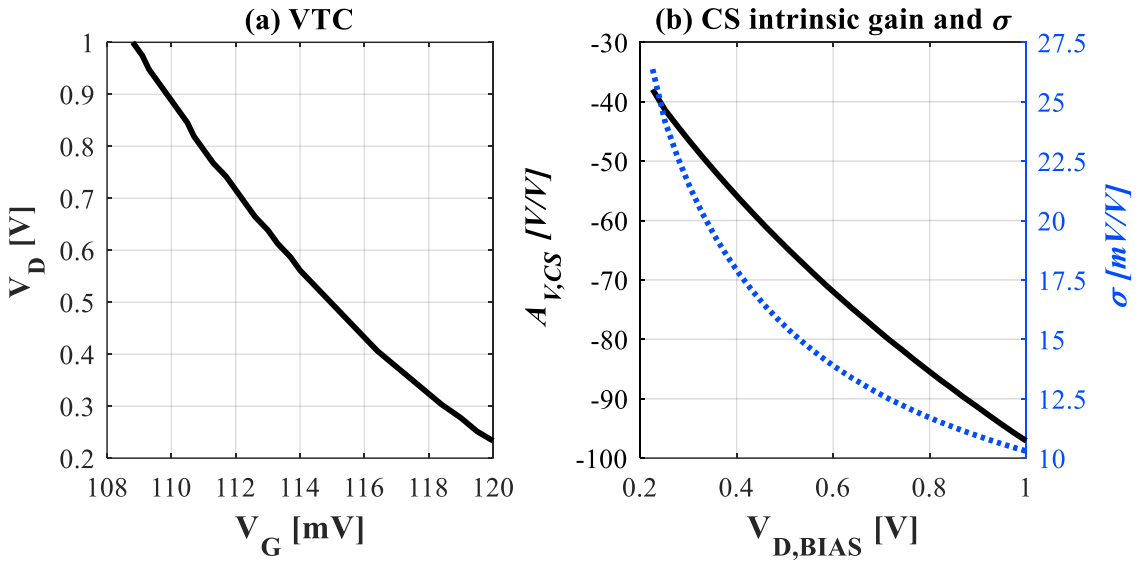

Figure 4.7. (a) Voltage transfer characteristic (VTC) of measured V_G and V_D on CSIG method; (b) intrinsic gain of common source topology in black and σ in blue as versus the sweep voltage $V_{D,BIAS}$.

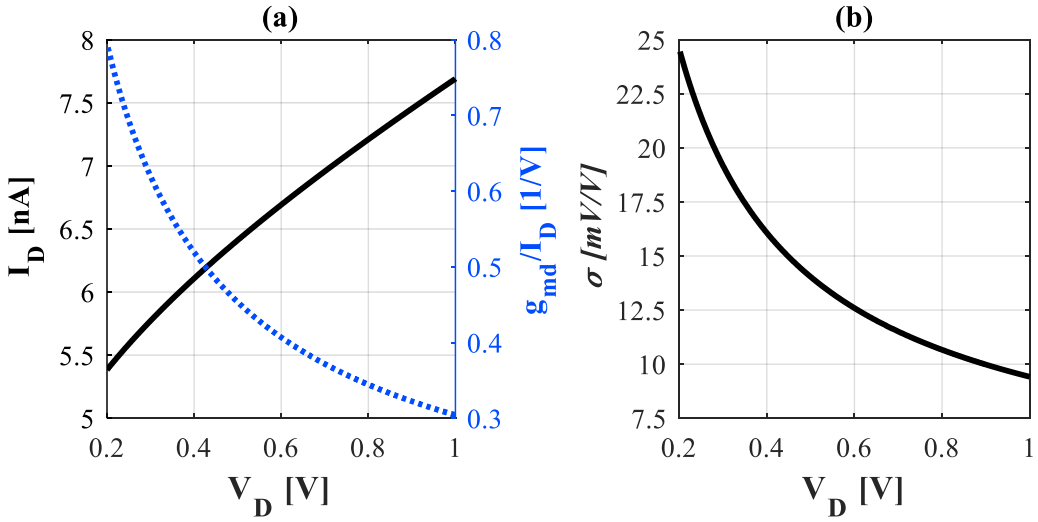

Figure 4.8. (a) Drain current $g_{md}/I_{D,sat}$ characteristic and (b) σ versus V_D

Figure 4.7(b) and Figure 4.8(b) present the σ value for each V_D. Though similar to the CSIG method, the $g_{md}/I_{D,sat}$ method presents higher values of σ for V_D below 400 mV.

Table 4.6 presents the σ values extracted by the common source intrinsic gain and $g_{md}/I_{D,sat}$ methods, for NMOS and PMOS transistors of long- and short-channel lengths at $V_D = 600\ mV$ and $V_G = 100\ mV$.

Table 4.6. Parameter σ extracted by the common source intrinsic gain and $g_{md}/I_{D,sat}$ methods

Method	Transistor	Long channel		Short channel	
		NMOS	**PMOS**	**NMOS**	**PMOS**
	$\boldsymbol{\frac{W}{L}}$	$\frac{1\ \mu m}{1\ \mu m}$	$\frac{1\ \mu m}{1\ \mu m}$	$\frac{1\ \mu m}{0.3\ \mu m}$	$\frac{1\ \mu m}{0.3\ \mu m}$
CSIG	$\boldsymbol{\sigma\ \left[\frac{mV}{V}\right]}$	5.8	18.2	13.7	19.7
$\frac{g_{md}}{I_{D,sat}}$		5.2	16.1	12.6	18.3

As seen in Table 4.6, the common source intrinsic gain and the $g_{md}/I_{D,sat}$ methods give very close values of σ for both short-and long-channel transistors. It should be noted that the DIBL effect is also present in long-channel transistors, even though irrelevant for the computation of the current. However, it plays an important role for the determination of the intrinsic transistor gain. Consequently, σ must be included as the 4th parameter in the ACM model.

5 IMPLEMENTING THE ACM MODEL IN CADENCE

Verilog-A is a procedural language to describe analog behavior, and all necessary interactions between the model and the simulator are handled by the Verilog-A compiler. It supports description of devices and circuits using ordinary differential algebraic equations [4].

Chapter 3 introduced the 4-parameter model using the ACM model. Table 5.1 resumes the main equations implemented in Verilog-A. Chapter 4 introduced the methods employed and automated in Cadence® Virtuoso® for the extraction of the four parameters of the ACM model.

Reference [3] explains and exemplifies how to use the ACM model to design various analog circuits. This chapter focuses on introducing the ACM model in Verilog-A to simulate MOS circuits, thus bridging the gap between design and simulation.

Table 5.1. Recalling the main equations presented in section 3.1

$$I_D = I_F - I_R = I_S\left(i_f - i_r\right)$$	(5.1)
$$I_S = I_{SH}\frac{W}{L}$$	(5.2)
$$\frac{V_P - V_{S(D)B}}{\phi_t} = q'_{IS(D)} - 1 + \ln q'_{IS(D)}$$	(5.3)
$$q'_{IS(D)} = \sqrt{1 + i_{f(r)}} - 1$$	(5.4)
$$\frac{V_P - V_{S(D)B}}{\phi_t} = \sqrt{1 + i_{f(r)}} - 2 + \ln\left(\sqrt{1 + i_{f(r)}} - 1\right)$$	(5.5)
$$V_P = \frac{V_{GB} - V_{T0} + \sigma V_{DB} + \sigma V_{SB}}{n}$$	(5.6)

The ACM model was implemented in three stages:

1. Description of the weak inversion four-parameter model.
2. Description of the all-region four-parameter model.
3. Inclusion of the dynamic model.

5.1 WEAK INVERSION MODEL

Weak inversion (WI) consists in an approximation of the UICM in equation (5.5) for which the inversion levels $i_{f(r)} \ll 1$. Applying this condition to the UICM leads to the straightforward equation (5.7) for the drain current of an NMOS transistor, where the subscript *N* refers to the N-channel MOSFET.

$$I_D = 2I_{SH_N}\frac{W_N}{L_N}e^1 e^{\left(\frac{V_{PN} - V_{SB}}{\phi_t}\right)}\left[1 - e^{\left(-\frac{V_{DS}}{\phi_t}\right)}\right] \tag{5.7}$$

$$V_{PN} = \frac{V_{GB} - |V_{TN}| + \sigma V_{DB} + \sigma V_{SB}}{n_N} \tag{5.8}$$

The previous equations are replicated for a PMOS transistor as (5.9) and (5.10), where the subscripted *P* refers to the P-channel MOSFET.

$$I_D = 2I_{SH_P}\frac{W_P}{L_P}e^1 e^{\left(\frac{V_{PP} - V_{BS}}{\phi_t}\right)}\left[1 - e^{\left(-\frac{V_{SD}}{\phi_t}\right)}\right] \tag{5.9}$$

$$V_{PP} = \frac{V_{BG} - |V_{TP}| + \sigma V_{BD} + \sigma V_{BS}}{n_P} \tag{5.10}$$

Expressions (5.7) – (5.10) were implemented in Verilog-A. The code is shown in Appendix D.1. The WI model in Verilog-A was tested by running simulations on NMOS and PMOS transistors, even though the results for the all-region model were prioritized in this work. One of the results using the WI model is presented in section 6.1.

As a final consideration, it was important to implement the WI model first to get familiarized with Verilog-A syntax and functions.

5.2 ALL-REGION MOSFET MODEL

The UICM in (5.5) is meant to simplify the design of various MOSFET circuits using the inversion levels; however, for a simulator, the terminal voltages are inputs, and the drain current is the output. When solving (5.5) for the drain current, one ends up with a transcendental equation that can be solved numerically. The simulator, however, solves the equation for each point and cannot waste time and processing power in iterative calculations to find the solution of one single point.

Siebel [5] tested some algorithms and ways to implement the ACM model in simulators and concluded that algorithm 443 of Fristsch, Shafer and Crowley [19] is the most accurate to solve ACM model in one single iteration.

Algorithm 443 solves the transcendental equations in the form $x = we^w$. To resemble such form, the UCCM in (5.3) can be easily rewritten as (5.11).

$$e^{\left(\frac{V_P - V_{S(D)B}}{\phi_t} + 1\right)} = q'_{IS(D)} e^{q'_{IS(D)}} \tag{5.11}$$

By comparing (5.11) to $x = we^w$, it yields equations (5.12) and (5.13).

$$x = e^{\left(\frac{V_P - V_{S(D)B}}{\phi_t} + 1\right)} \tag{5.12}$$

$$w = q'_{IS(D)} \tag{5.13}$$

Finally, the algorithm employs expressions from (5.14) to (5.17).

$$w_n = \begin{cases} \dfrac{x + \frac{4}{3}x^2}{1 + \frac{7}{3}x + \frac{5}{6}x^2}\,, \; for \;\; x < 0.7385 \\ ln(x) - \dfrac{24(ln(x)\,ln(x) + 2\,ln(x) - 3)}{7\,ln(x)\,ln(x) + 58\,ln(x) + 127}\,, for \;\; x \geq 0.7385 \end{cases} \tag{5.14}$$

$$e_n = \frac{z_n}{1 + w_n} \frac{2(1 + w_n)\left(1 + w_n + \frac{2}{3}z_n\right) - z_n}{2(1 + w_n)\left(1 + w_n + \frac{2}{3}z_n\right) - 2z_n} \tag{5.15}$$

in which

$$z_n = \ln(x) - w_n - \ln(w_n) \tag{5.16}$$

and, finally

$$w = w_n(1 + e_n) \tag{5.17}$$

From (5.11) and (5.13), the normalized forward and reverse charge densities are determined. Afterward, the definition of normalized charge density in (5.4) is solved for the forward and reverse inversion levels i_f and i_r, which, applied in (5.1) determine the drain current I_D.

The algorithm was implemented in MATLAB® and in Verilog-A. To test the model accuracy and learn if any deviations come from the model or from the simulator, the following steps were taken:

Step 1: calculate V_P for i_f from 0.001 to 1000 using the UICM, equation (5.5). The curve $V_P \; vs. \; i_f$ is presented in Figure 5.1(a).

Step 2: solve ACM for i_f using algorithm 443 [19] and the calculated i_f from Step 1 directly on MATLAB® and by running simulation on Cadence with Verilog-A description.

Figure 5.1(b) shows the ratio between the original i_f used in Step 1 and the one calculated through the algorithm in Step 2. In MATLAB®, the algorithm calculated i_f correctly, but in simulation using Verilog-A it achieved an error of 0.05% for $i_f \geq 6$. There has not been yet a thorough investigation on the cause for such difference when using the Verilog-A in a simulation, because, for the time being, the error was considered acceptable. The important thing to keep in mind is that the algorithm accurately solves the UICM.

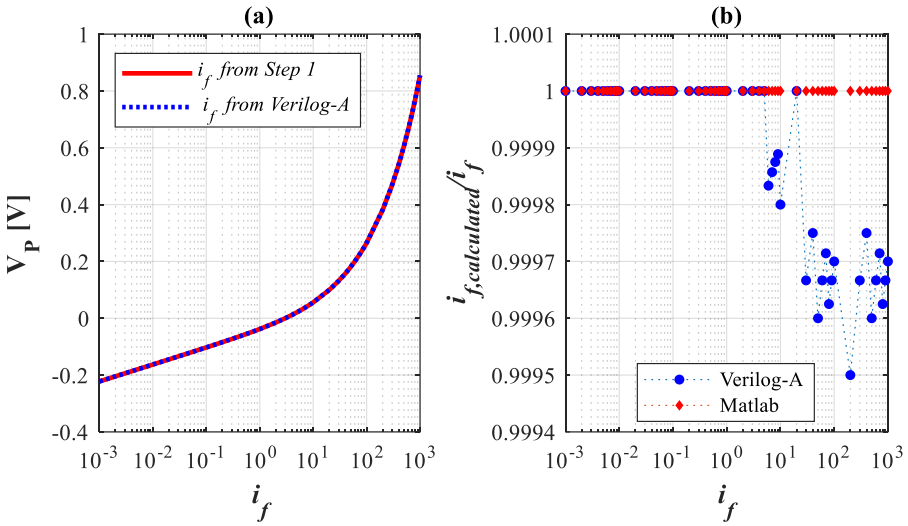

Figure 5.1. Validation of algorithm 443 [19] to solve the UICM: (a) comparison of the curve V_P $vs.$ i_f obtained through Verilog-A to the curve from MATLAB® and (b) result of Step 2 quantifying the error of Verilog-A in relation to MATLAB®

5.3 DYNAMIC MODEL

The dynamic model of the MOS transistor includes intrinsic and extrinsic capacitances, as described in section 3.2. Expressions (3.12) – (3.16) were implemented in Verilog-A just after the drain current calculations, using $\alpha = \frac{1+q_{iD}}{1+q_{iS}}$. The small-signal transconductances are used as design parameters that can easily be derived from the UICM. They appear in the model through the current-voltage relation.

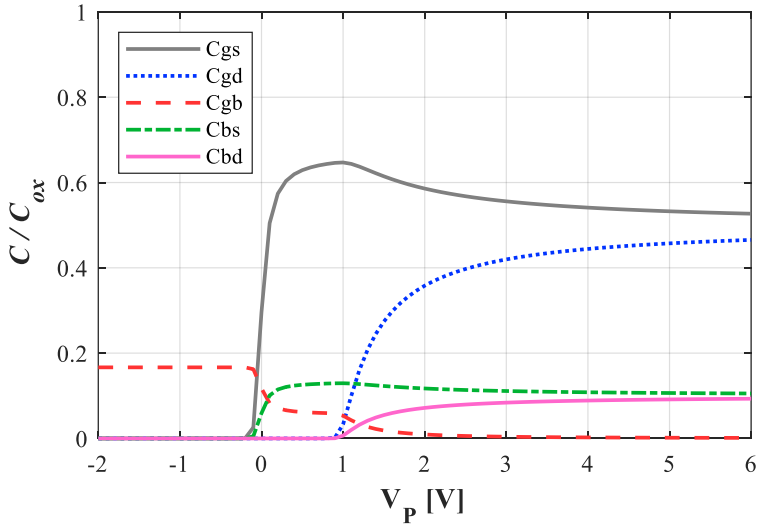

Figure 5.2. Capacitances $C_{gs}, C_{gd}, C_{gb}, C_{bs}$ and C_{bd} normalized by C_{ox} through a range for the pinch-off voltage from $-2\ V$ to $6\ V$, for $V_{DS} = 1\ V$. Results obtained using expressions (3.12) – (3.16).

Using the algorithm that solves the UICM, the capacitances were calculated for V_P from -2 V to 6 V at $V_{DS} = 1\,V$ using the extracted parameters for the long-channel NMOS transistor depicted in Table 5.2.

Figure 5.2 presents the capacitances normalized to C_{ox}. The results shown are consistent with the ones found in [20].

To obtain a closer dynamic result to BSIM's, extrinsic capacitances such as overlap capacitance $C_{go(gl)}$, junction diode capacitances $C_{bse(de)}$ and fringing capacitances were also included in the Verilog-A description in Appendix D.2 through simplified equations (5.18) and (5.19), which were found in the BSIM 4.5 Manual [21]. In (5.18), A_{eff} and P_{eff} are the effective junction area and perimeter.

$$C_{bse} = C_{bde} = A_{eff}C_{jb} + P_{eff}C_{jbsw} + WC_{jbswg} \tag{5.18}$$

$$C_{gse} = C_{gde} = \left(C_{go} + C_{gl} + C_f\right)W \tag{5.19}$$

Since the capacitances were not determined through extraction methods, the values used in (5.18) and (5.19) were searched and retrieved from the technology model; thus, they are not presented in this work due to the foundry's non-disclosure agreement.

An alternative would be to extract these capacitance values, but it would require further study on the subject.

5.4 MODEL RESULTS

The ACM all-region model described in Verilog-A (Appendix D.2) was simulated employing single transistors to compare with BSIM results. Table 5.2 summarizes the values extracted in Chapter 4 of long- and short-channel NMOS and PMOS transistors employed as inputs to the Verilog-A description for upcoming simulations.

Table 5.2. Extracted parameters selected as input to Verilog-A description

Transistor	Long channel		Short channel	
	NMOS	PMOS	NMOS	PMOS
$\frac{W}{L}$	$\frac{1.0\ \mu m}{1.0\ \mu m}$	$\frac{1.0\ \mu m}{1.0\ \mu m}$	$\frac{1.0\ \mu m}{0.3\ \mu m}$	$\frac{1.0\ \mu m}{0.3\ \mu m}$
$I_{SH}\ [nA]$	110	40	126	107
$V_{T0}\ [mV]$	290	-211	309	-240
n	1.19	1.17	1.23	1.18
$\sigma\left[\frac{mV}{V}\right]$	5.2	16.1	12.6	18.3

The first simulations with the Verilog-A description concerned the IV characteristic curves of MOS transistors. Figure 5.3 presents the $I_D vs. V_{GS}$ results at $V_{DS} = 200\ mV$ for the four transistors with the extracted parameters shown in Table 5.2.

The $I_D vs. V_{GS}$ characteristic was also obtained for $V_{DS} = 100\ mV, 500\ mV, 1V$, which are not displayed in this work to reduce the volume of similar results. Figure 5.4 presents the evaluation of these results in the form of $\frac{I_{D,ACM}}{I_{D,BSIM}}$, which provides an insight as to how close the ACM model results are to BSIM's throughout a large range of V_{GS}, which covers the weak, moderate and strong inversion regions. ACM equals BSIM at $V_{DS} = 100\ mV$, for only two V_{GS}values very close to V_{T0} and at $V_{GS} = 1.5\ V$.

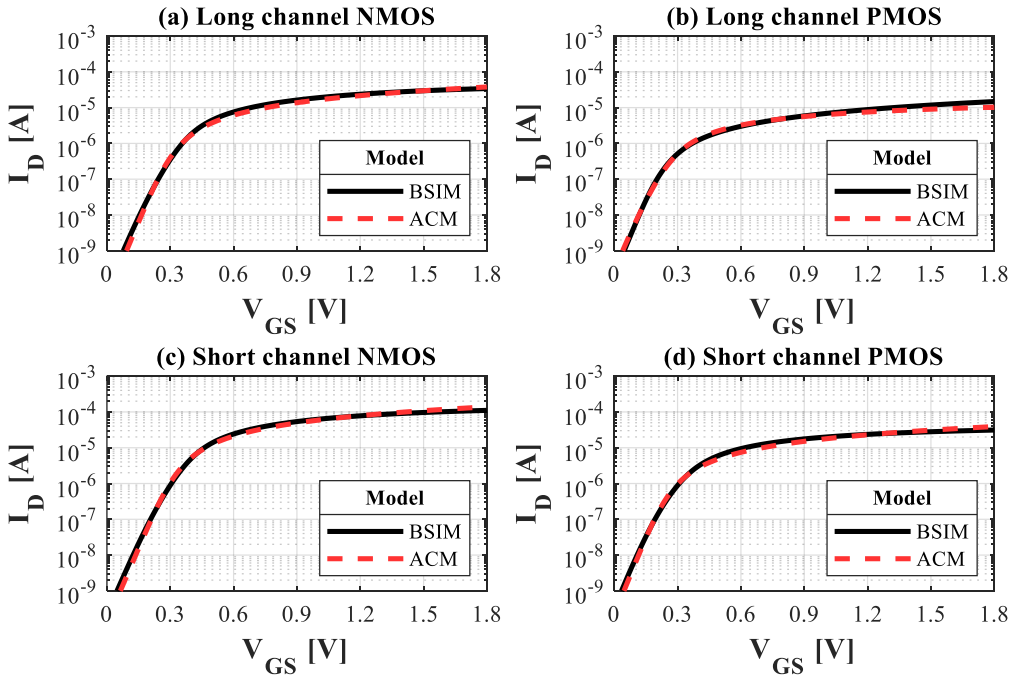

Figure 5.3. $I_D\ vs. V_{GS}$ @ $V_{DS} = 200\ mV$ for (a) long-channel NMOS and (b) PMOS transistors, and (c) short-channel NMOS and (d) PMOS transistors whose extracted parameters are depicted in Table 5.2.

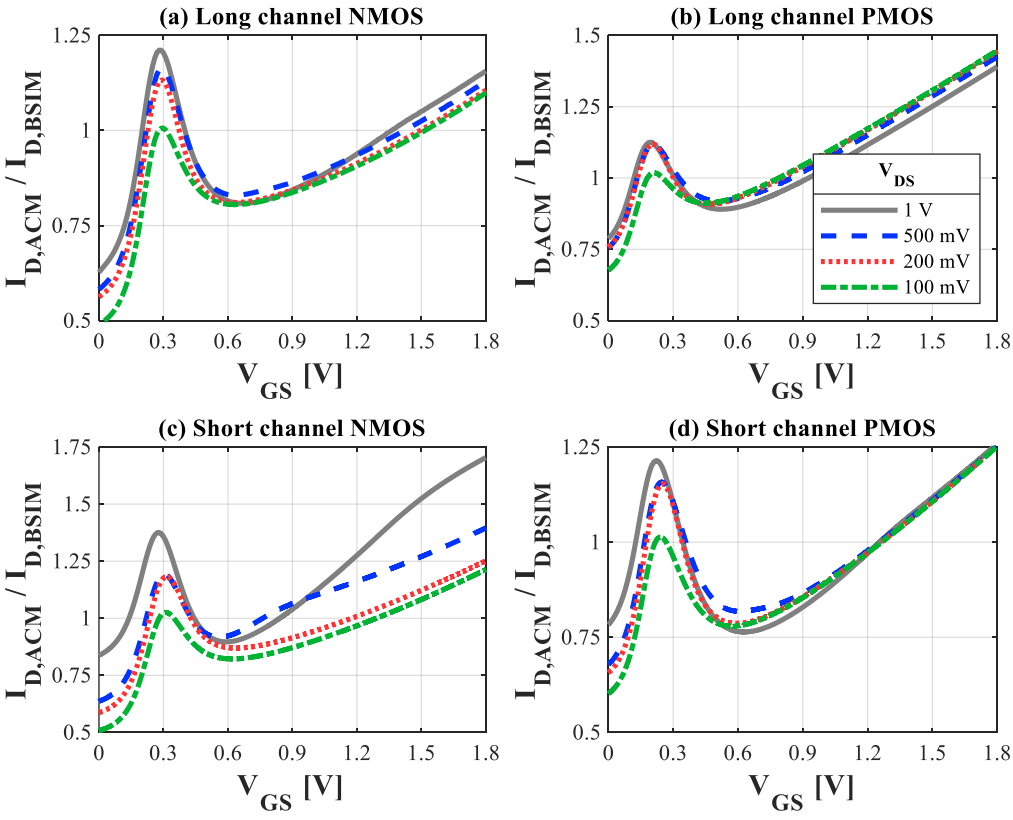

Figure 5.4. Evaluation of ACM with respect to BSIM for $I_D\ vs. V_{GS}$ @ $V_{DS} = 100\ mV, 200\ mV, 500\ mV, 1\ V$ for (a) long channel NMOS and (b) PMOS transistors, and (c) short channel NMOS and (d) PMOS transistors, each transistor whose extracted parameters are depicted in Table 5.2.

Overall, the long-channel transistors resulted in closer values to BSIM's throughout the V_{GS} range, while the short-channel transistors drift further from BSIM's, particularly, for higher values of V_{GS}, since in that region short-channel effects other than the DIBL were not taken into account in the ACM model used.

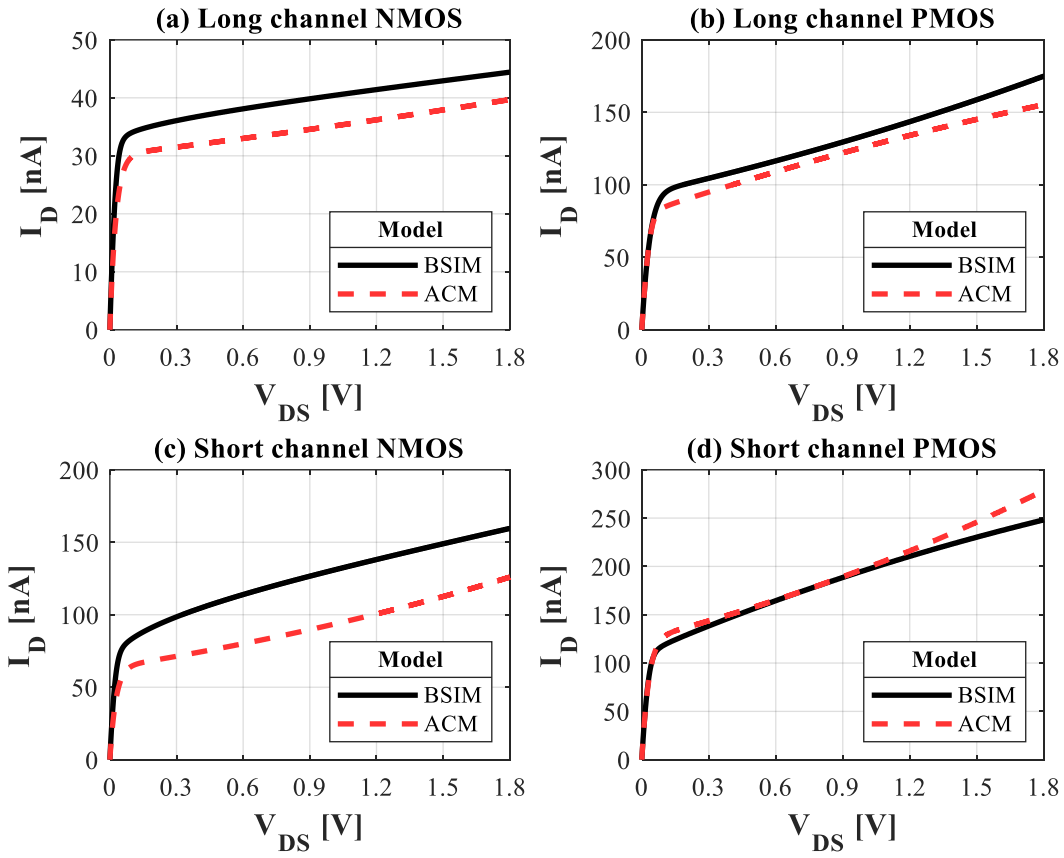

Figure 5.5. $I_D\ vs. V_{DS}$ @ $V_{GS} = 200\ mV$ for (a) long channel NMOS and (b) PMOS transistors, and (c) short channel NMOS and (d) PMOS transistors, each transistor whose extracted parameters are depicted in Table 5.2.

Figure 5.5 presents the $I_D vs. V_{DS}$ results at $V_{GS} = 200\ mV$ for the four transistors whose extracted parameters are depicted in Table 5.2.

The $I_D vs. V_{DS}$ characteristic was also obtained for $V_{GS} = 100\ mV, 500\ mV, 1V$, though, they are not displayed in this work, Figure 5.6 presents the evaluation of these results in the form of $\frac{I_{D,ACM}}{I_{D,BSIM}}$, which provides an insight regarding accuracy of ACM in the linear and saturation regions of the MOS transistors.

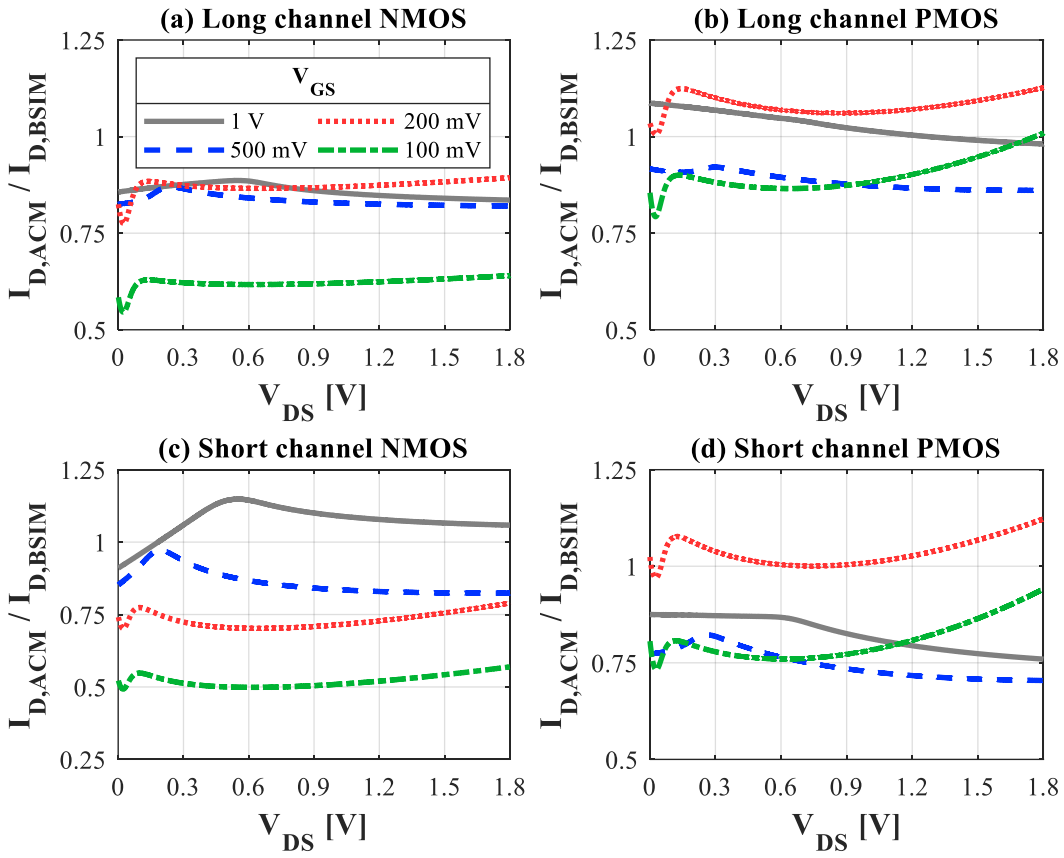

Figure 5.6. Evaluation of ACM with respect to BSIM for $I_D\ vs. V_{DS}$ @ $V_{GS} = 100\ mV, 200\ mV, 500\ mV, 1\ V$ (green, red, blue and grey, respectively) for (a) long-channel NMOS and (b) PMOS transistors, and (c) short-channel NMOS and (d) PMOS transistors, each transistor whose extracted parameters are depicted in Table 5.2.

Once again, the errors of ACM towards BSIM are lower for long channel transistors in comparison with the short channel ones. This occurs mainly because there are secondary short-channel effects not included in the 4-parameter model. The only short-channel effect included is the DIBL, which overall affects the slope of the $I_D vs. V_{DS}$ curve along the saturation region.

The final simulation results in this section are related to the diode configuration in which $V_G = V_D$. Figure 5.7 shows the obtained results while Figure 5.8 presents the same results in the form of $\frac{I_{D,ACM}}{I_{D,BSIM}}$. The error of the ACM in relation to BSIM seems to be higher in deep weak inversion, for voltages lower than 100 mV, and for PMOS transistor the error is higher in strong inversion, but, in any case, . the errors remained within 25%.

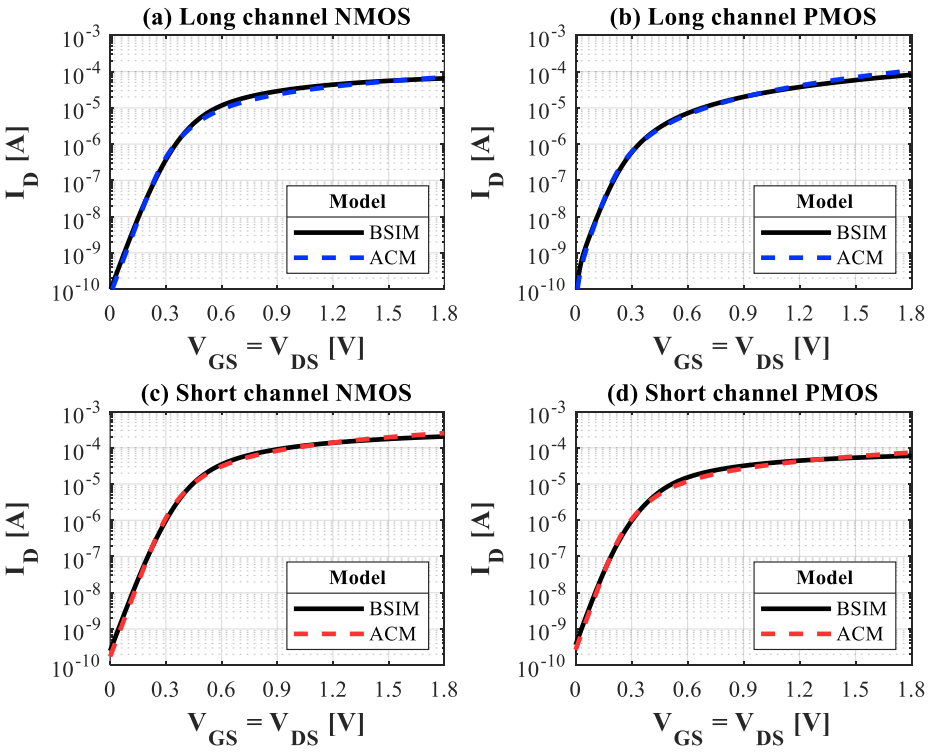

Figure 5.7. $I_D\ vs. V_{GS} = V_{DS}$ for (a) long channel NMOS and (b) PMOS transistors, and (c) short channel NMOS and (d) PMOS transistors, each transistor whose extracted parameters are depicted in Table 5.2.

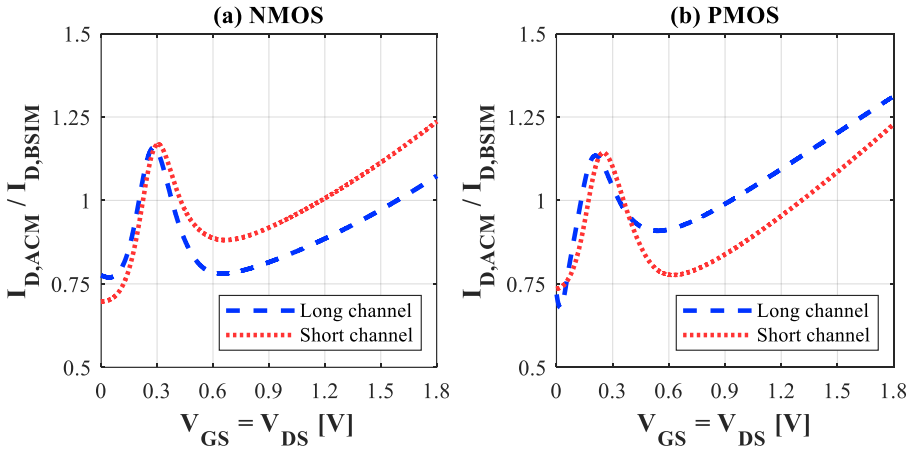

Figure 5.8. Evaluation of ACM with respect to BSIM for $I_D\ vs. V_{GS} = V_{DS}$ for (a) long and short channel NMOS transistors and (b) long and short channel PMOS transistors, each transistor whose extracted parameters are depicted in Table 5.2.

It is important to keep in mind that the low-frequency ACM model is being simulated with only 4 extracted parameters, whereas BSIM requires over 60 parameters for DC simulation and very complicated functions, yet, the ACM and BSIM results are very close when looking at Figure 5.3, Figure 5.5 and Figure 5.7. While the comparison in this work regards BSIM, Silva in [22] shows how accurate ACM is when it comes to actual manufactured transistors.

6 CIRCUIT EXAMPLES

In this Chapter, four different circuits are simulated using the ACM model Verilog-A description and BSIM. The four circuits are the classic CMOS inverter, a ring oscillator employing the CMOS inverter, a self-biased current source (SBCS) and an RF low-noise amplifier (LNA).

6.1 CMOS INVERTER

One of my professors once said that, regardless of how poorly it was designed, the CMOS inverter will work due to its own robustness. It might work poorly but will work.

A versatile and yet simple circuit, the CMOS inverter consists of PMOS and NMOS transistors connected as shown in Figure 6.1, in which I_{SC} is the short circuit current and V_{DD} the supply voltage. Besides its use for digital applications, CMOS inverters are very useful analog building blocks. Amplifiers [23], [24] and oscillators [25], [26] are just a few of the analog applications of CMOS inverters.

Thus, as a favorite of both analog and digital circuit designers, the CMOS inverter is, herein, the first circuit taken to a test drive of the ACM model in the Verilog-A description. The purpose of the test is to check the quality of the 4-parameter model rather than to comply with some specifications. One inverter implemented with long-channel transistors and another with short-channel transistors were simulated. The transistors dimensions along with the extracted parameters are depicted in Table 5.2.

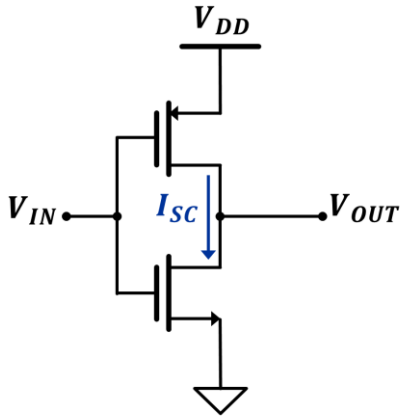

Figure 6.1. The CMOS inverter

6.1.1 Simulation Results

The CMOS inverter was tested using the WI model and the all-region ACM model in Verilog-A. Figure 6.2 presents the simulated Voltage Transfer Characteristic (VTC), short-circuit current and small-signal gain of the CMOS inverter with long channel transistors, determined via DC simulation, are presented in. The results for the CMOS inverter.

The simulated VTC in Figure 6.2 (a) shows that for low values of the supply voltage the WI model is appropriate to model the inverter electrical behavior. For $V_{DD} = 400\,mV$ or higher, the WI model drifts away from BSIM since the transistors start to leave the weak inversion region

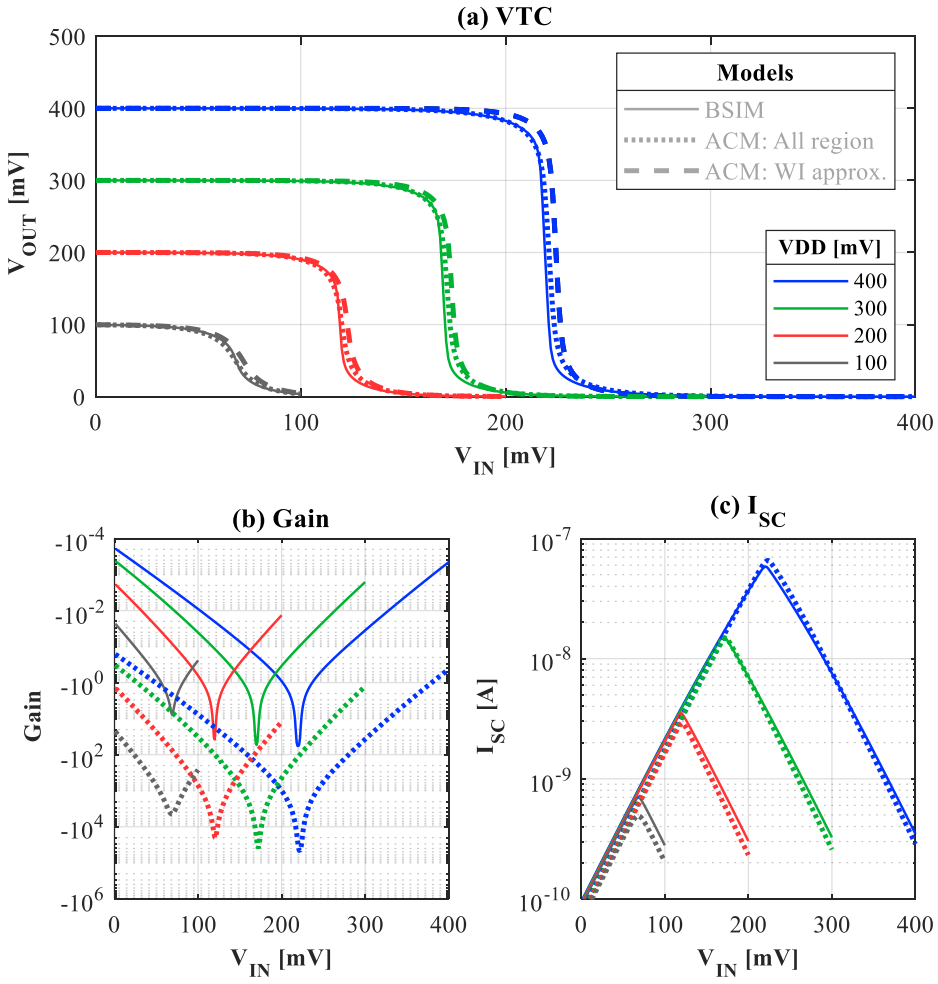

Figure 6.2 (a) Voltage transfer characteristic (VTC) for BSIM, WI and ACM models, (b) small-signal gain and (c) short-circuit current for BSIM and ACM models of CMOS inverter implemented with the long-channel transistors in Table 5.2

The slightly different inclination of ACM in relation to BSIM on Figure 6.2, becomes clearer in Figure 6.2 (b), representing the small-signal gain, the derivative of VTC, in which ACM results are 1000 times higher than BSIM's. On the other hand, the maximum gain in absolute value occurs for the same V_{IN} for both BSIM and ACM.

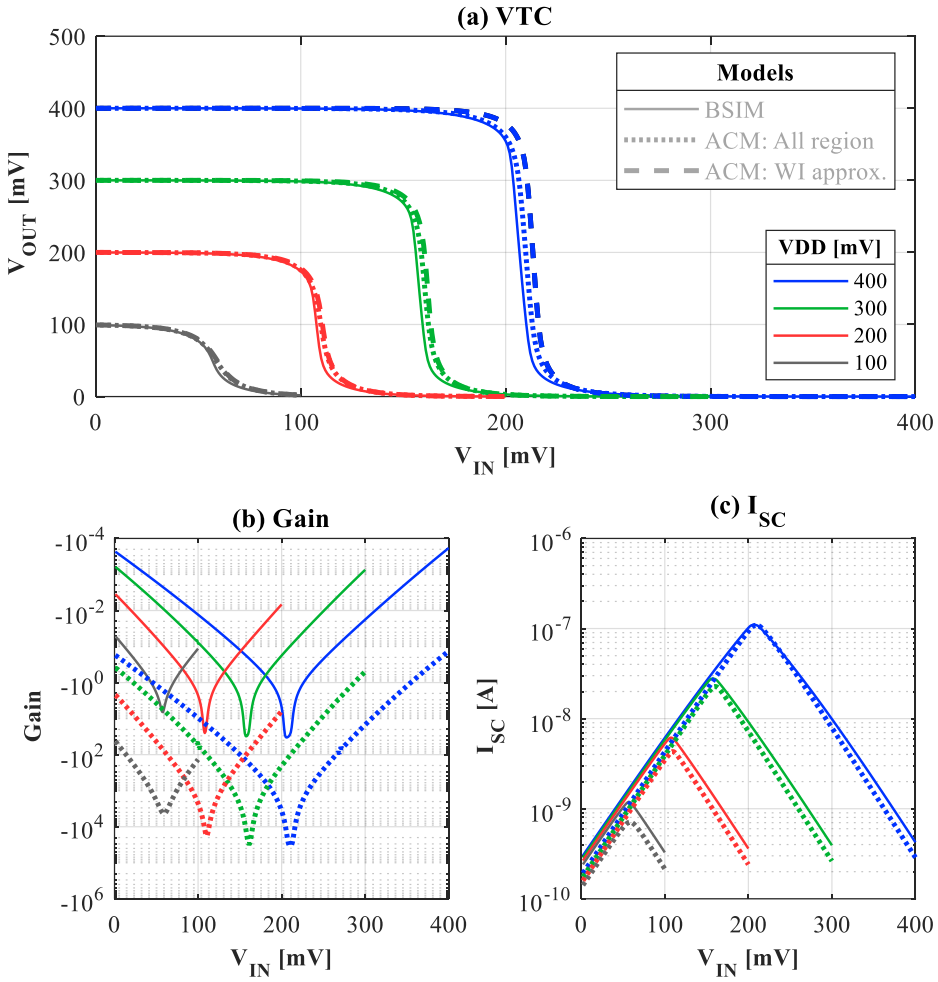

Figure 6.3. (a) Voltage transfer characteristic (VTC) for BSIM, WI and ACM models, (b) small-signal gain and (c) short-circuit current for BSIM and ACM models of CMOS inverter implemented with the short-channel transistors whose extracted values are depicted in Table 5.2

Figure 6.3 provides simulation results of the CMOS inverter with short channel transistors. The conclusions are similar to those presented for Figure 6.2.

6.2 RING OSCILLATOR

Ring oscillators appear in many systems due to their wide tuning range, compact layout, and ability to generate multiple phases [27].

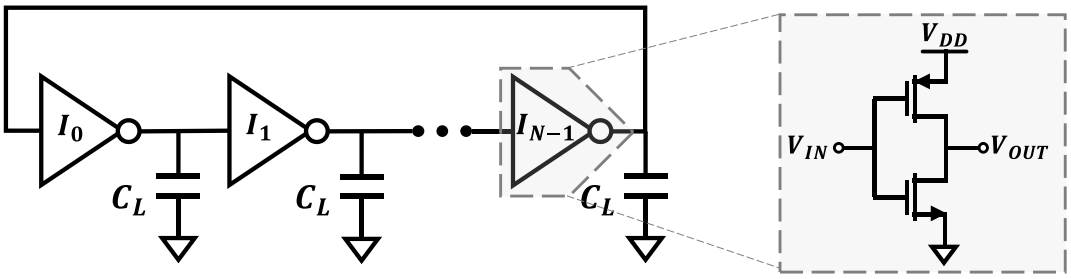

Figure 6.4. N-stage ring oscillator

The ring oscillator, illustrated in Figure 6.4, consists of an odd number N of gain stages in a loop. Each stage is composed of a CMOS inverter with a frequency-dependent voltage gain given by (6.1) [26], in which g_m is the combined PMOS and NMOS gate transconductances, g_o is the output conductance of the inverter, and $\omega = 2\pi f$ is the radian frequency.

$$\frac{v_o}{vi}(j\omega) = -\frac{g_m/g_o}{1 + j\omega\frac{C_L}{g_o}} \tag{6.1}$$

The load capacitance C_L in-between stages is crucial to set the oscillator frequency and critical for successful start-up. It encompasses all capacitances on that node, which includes the intrinsic and extrinsic capacitances of the transistors, interconnect capacitance, and, occasionally, capacitors connected to the node, as well as the combination.

6.2.1 Simulation Results

An 11-stage ring oscillator was implemented to check whether the dynamic model included in the Verilog-A description was working or not. Table 6.1 presents the overall results.

The dynamic model of the first simulation included the 5 intrinsic capacitances expressed by (3.12) – (3.16) and the overlap capacitance introduced in sections 3.2 and 5.3. The waveforms for obtained for $V_{DD} = 100\ mV, 200\ mV, 500\ mV, 1V$ are depicted in Figure 6.5.

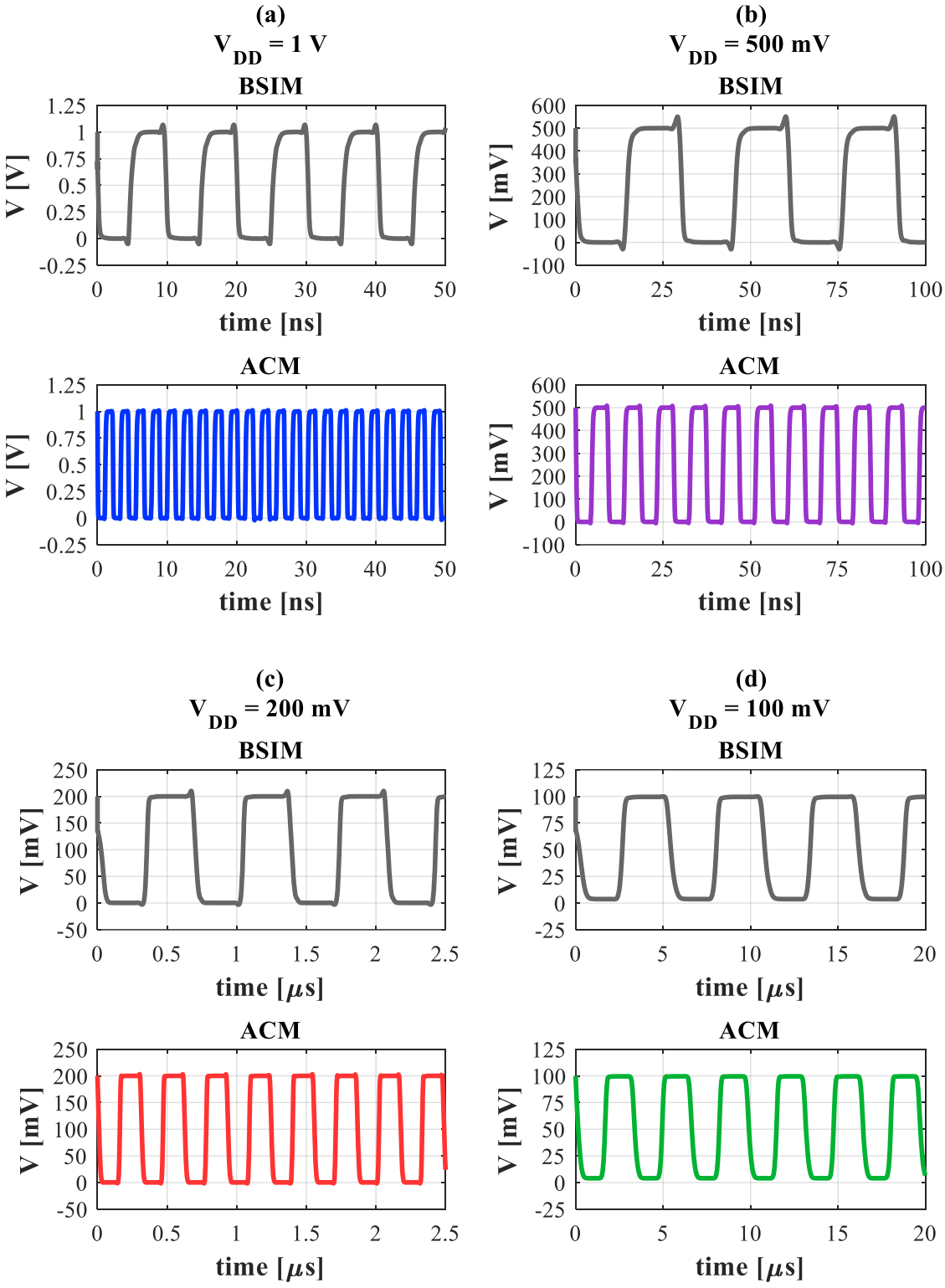

Figure 6.5. Results of time-domain simulations for the ring oscillator at V_{DD} = (a) 1 V, (b) 500 mV, (c) 200 mV and (d) 100 mV. The dynamic model included 5 intrinsic capacitances and the extrinsic overlap capacitances.

As seen in Figure 6.5, the oscillator started; however, the frequency of oscillation using the ACM model differed in over 400% from the BSIM result at V_{DD}=1 V. It meant the dynamic model was working, though it did not match the result of BSIM, since some capacitances, mainly the fringing and junction capacitances, were missing.

On the next step, the fringing capacitance was added in the Verilog-A description, completing the gate extrinsic capacitance $C_{gse(de)}$. Finally, the junction capacitances were also included and completed the bulk extrinsic capacitance $C_{bse(de)}$.

Table 6.1 gives the frequency f obtained for each model after successive successive inclusions of capacitances on the dynamic model. For the sake of comparison between ACM and BSIM, Table 6.2 presents f_{ACM}/f_{BSIM}. Through the modifications on the dynamic model implemented in Verilog-A, the frequency determined with the ACM model became closer to BSIM's.

Table 6.1. Frequency obtained from time-domain simulations for different implementations of the dynamic model.

Models	**BSIM**	**ACM** Dynamic model includes 5 intrinsic capacitances and:		
V_{DD}		**Overlap capacitance**	**Complete $C_{gse(de)}$**	**$C_{gse(de)}$ and $C_{bse(de)}$**
1 V	98 MHz	446 MHz	275 MHz	201 MHz
500 mV	32.3 MHz	106 MHz	65 MHz	48 MHz
200 mV	1.45 MHz	3.2 MHz	1.95 MHz	1.41 MHz
100 mV	187 kHz	306 kHz	186 kHz	136 kHz

Table 6.2 Evaluation of f_{ACM}/f_{BSIM} from the results in Table 6.2

ACM Dynamic model includes 5 intrinsic capacitances and:			
V_{DD}	**Overlap capacitance**	**Complete $C_{gse(de)}$**	**$C_{gse(de)}$ and $C_{bse(de)}$**
1 V	4.55	2.81	2.05
500 mV	3.28	2.01	1.49
200 mV	2.20	1.34	0.97
100 mV	1.64	0.99	0.73

In a final approach, external capacitors $C_L = 1\ pF$ were connected to each stage. The goal of the inclusion of high-valued external capacitors was to attenuate the effect of the capacitances inherent to the ring oscillator on the frequency response and, consequently, to improve the ACM's accuracy in relation to BSIM's. The results in Table 6.3 show that, except for $V_{DD} = 100\ mV$, the highest error was below 10%.

Table 6.3. Frequency results of time-domain simulations of an 11-stage ring oscillator with external $C_L = 1\ pF$

V_{DD}	BSIM	ACM	f_{ACM}/f_{BSIM}
1 V	1.82 MHz	1.71 MHz	0.94
500 mV	448 kHz	405 kHz	0.90
200 mV	12.5 kHz	12.25 kHz	0.98
100 mV	1. 6 kHz	1.2 kHz	0.75

6.3 SELF-BIASED CURRENT SOURCE (SBCS)

This section presents a simple design of a self-biased current source (SBCS) and DC simulation results to visualize how close to BSIM is the ACM model. The design of the SBCS in Figure 6.6 follows the steps presented by Camacho in [28]. The target output current is 100 nA at a supply voltage of 1.8 V.

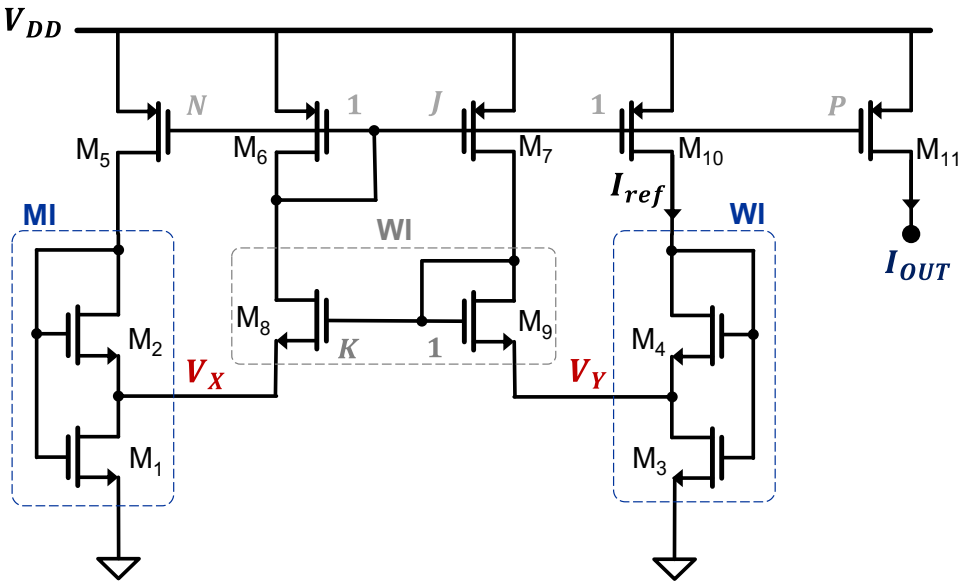

Figure 6.6. Self-biased current source (SBCS) circuit

6.3.1 Design using the ACM model

The core of the SBCS in Figure 6.6 is the self-cascode MOSFET (SCM) composed of transistors M_1 and M_2, which operate in moderate inversion. The second SCM, composed of M_3 and M_4, is biased in weak inversion and generates a proportional to absolute temperature (PTAT) voltage V_Y.

Since $M_{2(4)}$ is in saturation and $M_{1(3)}$ is in triode, $I_{D2} \cong I_{S2} i_{f2}$ and $I_{D1} = I_{S1(i_{f1} - i_{r1})} = I_{ref}(N+1)$. Since $V_{P1} = V_{P2} = V_P$ and $V_{D1} = V_{S2}$, we have $i_{r1} = i_{f2}$; hence, using (3.1) and (3.2) yields relationship (6.2) [28].

The SCM intermediate voltage $V_{X(Y)}$ relates to the inversion level by design equations (6.3) and (6.4), which have already been approximated for this case of study but can be directly derived from the ACM using (3.5) and (6.2).

$$\alpha_{12(34)} = \frac{i_{f1(3)}}{i_{f2(4)}} = 1 + \frac{S_{2(4)}}{S_{1(3)}}\left(1 + \frac{1}{N}\right) \tag{6.2}$$

$$\frac{V_X}{\phi_t} = \sqrt{1 + \alpha_{12} i_{f2}} - \sqrt{1 + i_{f2}} + \ln\left(\frac{\sqrt{1 + \alpha_{12} i_{f2}} - 1}{\sqrt{1 + i_{f2}} - 1}\right) \tag{6.3}$$

$$\frac{V_Y}{\phi_t} = \ln(\alpha_{34}) \tag{6.4}$$

In the SCM design, there are three unknown parameters i_f, α and $V_{X(Y)}$. In this design example, $i_{f2} = 15$ was chosen. To simplify the design further, $S_1 = S_2$ and $J = K = P = N = 1$, which results in $\alpha_{12} = 3$.

For the 0.18 µm technology used in this work, the sheet normalization current of a standard-vt NMOS transistor, with $\frac{W}{L} = \frac{0.5\,\mu m}{2\,\mu m}$, was extracted and found to be $I_{SH2} = 115\,nA$. Applying it in (3.1) for M_2 results in (6.5).

$$I_{SH2} S_2 i_{f2} = I_{OUT} = 100\,nA \rightarrow S_2 = 0.058 \tag{6.5}$$

A series association [29] of 4 transistors, each one with $\frac{W}{L} = \frac{0.5\mu m}{2\mu m}$, was employed to obtain the calculated S_2. The intermediate voltage V_X is found to be 88.7 mV by using the calculated α_{12} and the chosen i_{f2} in (6.3), for $\phi_t = 25.8\,mV$.

As $V_X = V_Y$, expression (6.4) results in $\alpha_{34} = 32$, which, by applying in (6.2) results in $S_3 = 0.0645\ S_4$. Also, for $i_{f4} = 0.01$ then $i_{f3} = \alpha_{34} i_{f4} = 0.32$.

The sheet normalization current extracted from a standard-vt NMOS transistor with dimension $\frac{W}{L} = \frac{4\ \mu m}{2\ \mu m}$ is $I_{SH4} = 126\ nA$. By repeating (6.5) for I_{SH4} results in $S_4 = 79.3$ and $S_3 = 5.1$.

Transistor M_4 was implemented with a parallel association of 40 transistors of $\frac{W}{L} = \frac{4\ \mu m}{2\ \mu m}$, whereas M_3 consists of a parallel association of 20 transistors with $\frac{W}{L} = \frac{0.5\ \mu m}{2\ \mu m}$.

The voltage follower $M_{8\text{-}9}$ was sized with $M_8 = M_9$, both being composed of a parallel association of 35 transistors, each one with dimensions equal to those of $M_{1\text{-}3}$, for achieving the inversion level of $i_{f8} = 0.1$.

The inversion level of the P-mirror composed of $M_{5\text{-}7}$ and $M_{10\text{-}11}$ was set to $i_{fP} = 10$. The sheet normalization current of a standard-vt PMOS transistor, $\frac{W}{L} = \frac{0.5\ \mu m}{2\ \mu m}$, was extracted and determined to be $I_{SHP} = 38\ nA$. Repeating (6.5) for I_{SHP} results in $S_P = 0.26$. Table 6.4 summarizes the sizes and inversion levels used in the design.

Table 6.4 Transistor sizes for the SBCS

Transistor	$M_{1,2}$	M_3	M_4	$M_{8,9}$	$M_{5\text{-}7,10,11}$
$\frac{W}{L} \times \frac{N_{parallel}}{N_{series}}$	$\frac{0.5\ \mu m}{2.0\ \mu m} \times \frac{1}{4}$	$\frac{0.5\ \mu m}{2.0\ \mu m} \times \frac{20}{1}$	$\frac{4.0\ \mu m}{2.0\ \mu m} \times \frac{40}{1}$	$\frac{0.5\ \mu m}{2.0\ \mu m} \times \frac{35}{1}$	$\frac{0.5\ \mu m}{2.0\ \mu m} \times \frac{1}{1}$
i_f	15	0.32	0.01	0.1	10

The transistor parameters were extracted to be used as input parameters in the ACM model described in Verilog-A. These values, shown in Table 6.5, regard one single transistor of W/L, rather than the parameters of the overall association.

The g_m/I_D method was used to extract I_{SH} and V_{T0}, whereas the slope factor n was taken from the $3I_S$ method, because it presented a lower variation with W and, when put to proof in simulation, it provided closer results to BSIM than by using the slope factor from the g_m/I_D characteristic. The DIBL factor σ was extracted using the g_{md}/I_D method.

Table 6.5. Parameter extraction results of transistors used in the SBCS

Transistor	NMOS		PMOS
$\frac{W}{L}$	$\frac{0.5\ \mu m}{2.0\ \mu m}$	$\frac{4.0\ \mu m}{2.0\ \mu m}$	$\frac{0.5\ \mu m}{2.0\ \mu m}$
$I_{SH}\ [nA]$	115	126	38
$V_{T0}\ [mV]$	423	444	– 428
n	1.27	1.27	1.31
$\sigma\left[\frac{mV}{V}\right]$	2.2	2.4	6.5

6.3.2 Simulation Results

Figure 6.7 presents the DC simulation results of BSIM and ACM models obtained for a voltage sweep on V_{DD} from 0 to 1.8 V.

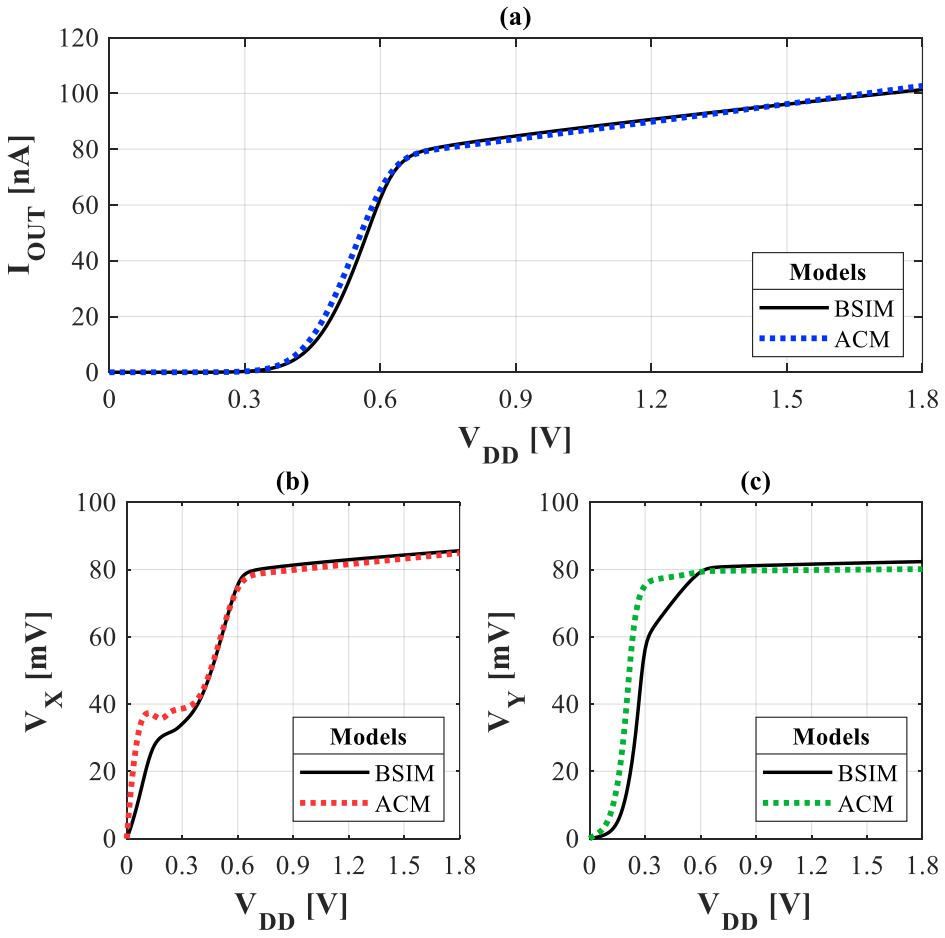

Figure 6.7. Results of DC simulation with sweep on the supply voltage V_{DD}

The output current presents a variation of 20 nA (25%), for V_{DD} from 700 mV to 1.8 V. At $V_{DD} = 1.8\,V$, $I_{OUT} \cong 104\,nA$. The calculated V_X was of 88 mV, while in simulation, the average $V_X \cong 86\,mV$ and $V_Y \cong 81\,mV$, over the range 700 mV to 1.8 V. More details about the design of the SBCS can be optimized found in [28], [30] and [31].

Overall, BSIM and the ACM model in Verilog-A provided consistent results for the output current, although a curious fact was observed while performing the V_{DD} voltage sweep. Figure 6.8 shows the print screen of one of the early SBCS simulation results. The ACM model in blue seemed more realistic than BSIM's in red. At first, we supposed that some startup issue concerning BSIM's calculations was the cause of the misbehavior of the transfer characteristic. However, the problem was not solved by sweeping the voltage V_{DD} from 1.8 V to 0 V. On the other hand, the sweeping of V_{DD} from 0 to 1.8 V provided the BSIM results shown in Figure 6.7 after increasing the number of parallel transistors that compose $M_{8(9)}$, which might suggest that the misbehavior in Figure 6.8 could be related to the output conductance model implemented in BSIM. The matter requires further investigation, whether it is a design problem or a need for better setup to simulate the SBCS with BSIM.

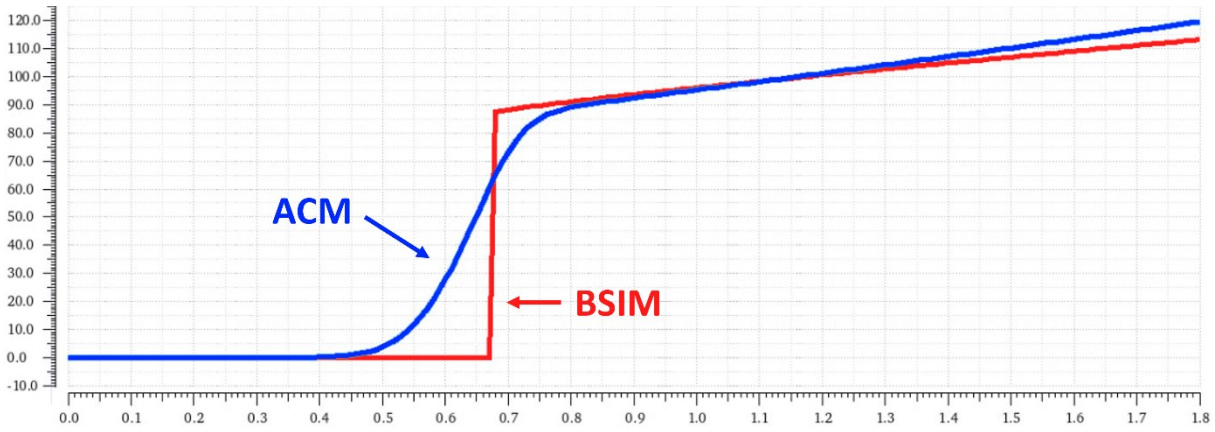

Figure 6.8. Print-screen of simulator with initial results of SBCS

At this point, the ACM model actually served as a reference to check whether the result obtained by BSIM was consistent with the expected one. The use of the ACM model for simulation along with BSIM can be a helpful counterproof for an aspiring designer or even a professional one to verify if the simulation setup was properly configured or if there are issues on the design itself.

6.4 Low Noise Amplifier (LNA)

So far, DC and time-domain simulation results were shown, but the performance of the ACM model in the frequency domain is lacking. In this section a low noise amplifier (LNA) designed using some of the small-signal aspects of the ACM model is presented.

6.4.1 Design using the ACM model

The LNA herein is based on [32], as it presents a methodology to design an LNA using the gm/ID relationship derived from the ACM model. However, it remains a challenging design due to the several analyses one should consider for evaluating the full performance of such circuit. Since the goal in this work is to compare the ACM results versus BSIM's, for the sake of sii88mplicity, the design and specifications will be simplified.

A basic LNA topology and its equivalent small signal model are shown in Figure 6.9.

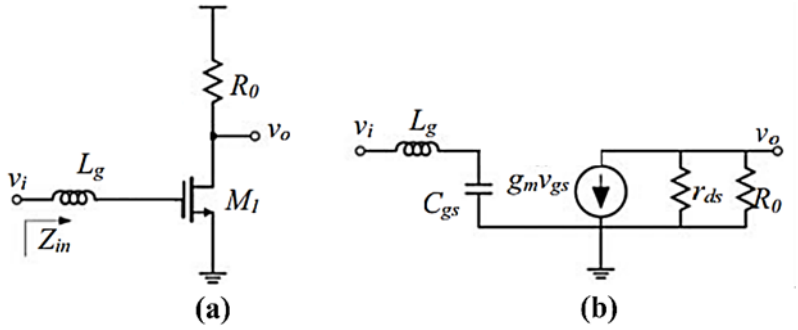

Figure 6.9. (a) LNA structure and (b) its equivalent small-signal model adapted from [32].

As the name indicates, noise is one of the main concerns when it comes to a low noise amplifier. The noise figure NF quantifies the amount of noise added by a device. For the circuit in Figure 6.9, according to [32], the approximate expression given by (6.6) can be used to determine the gate transconductance g_m required to achieve a specified noise figure without any consideration on the size of the transistor.

$$NF = 1 + \frac{\gamma}{g_m R_g} + \frac{1}{g_m^2 R_g R_L} \tag{6.6}$$

This design will focus on achieving a maximum noise figure $NF = 3\ dB$. Assuming a noise excess factor $\gamma = \frac{2}{3}$ [33] (more information concerning noise excess factor can be found

in [34]), a source impedance $R_g = R_L = 50\ \Omega$, where R_L is the output load impedance, then the gate transconductance in (6.6) results in $g_m = 27.6\ mS$.

The gain is another important parameter when it comes to amplifiers. In [32] the voltage gain is given by (6.7) where the input Q-factor Q_{in} is expressed as in (6.8). By setting $Q_{in} = 1$, the center frequency $f_0 = 2.44\ GHz$ and $R_g = 50\ \Omega$, then $L_g = 3.3\ nH$. To obtain a voltage gain of 10 dB, assuming the transistor output resistance $r_{ds} = \frac{1}{g_{ds}} = R_0$, (6.7) results in $R_0 = 156\ \Omega$.

$$G_{lna} = \frac{V_o}{Vi} = g_m(r_{ds}//R_0)\sqrt{1 + Q_{in}^2} \tag{6.7}$$

$$Q_{in} = 2\pi f_0 \frac{L_g}{R_g} \tag{6.8}$$

$$\frac{g_m}{I_{D,sat}} = \frac{2}{n\phi_t(\sqrt{1 + i_f} + 1)} \tag{6.9}$$

Expression (3.11) for a saturated transistor is repeated in (6.9). If $I_D = \frac{g_m}{g_m/I_{D,sat}}$, for a drain current $I_D = 1\ mA$, then $\frac{g_m}{I_{D,sat}} = 27.6$, which corresponds to an inversion level $i_f = 0.8$.

The average I_{SH} extracted from NMOS transistors is around hundreds of nA, which indicates that the aspect ratio will be high for a drain current of 1 mA. A standard-vt transistor of $\frac{W}{L} = \frac{18\ \mu m}{0.18\ \mu m} = 10$, was chosen.

Repeating (6.5) in section 6.3.1, using the extracted $I_{SH} = 204\ nA$ results in an aspect ratio $S = 6128$. To accomplish this S, 61 transistors were associated in parallel. Having sized the transistor, the gate voltage bias V_{GB} can be determined through the UICM expressed as (6.10) for $i_f = 0.8$ and $V_S = V_B = 0$. The extracted parameters are depicted in Table 6.6.

$$\frac{V_{GB} - V_{T0}}{n} - V_{SB} = \phi_t\left[\sqrt{1 + i_f} - 2 + \ln\left(\sqrt{1 + i_f} - 1\right)\right] \tag{6.10}$$

Table 6.6. Extracted parameters of transistor used in LNA

$\frac{W}{L}$	I_{SH}	V_{T0}	n	σ
$\frac{18\ \mu m}{0.18\ \mu m}$	$204\ nA$	$532\ mV$	1.3	$21.8\frac{mV}{V}$

To achieve $i_f = 0.8$ that gives the minimum gate transconductance $g_m = 27.6\,mS$ to obtain a maximum $NF = 3\,dB$, transistor M_1 should be biased with $V_{GB} = 474\,mV$. The g_m/I_D relationship from (6.9) and the UICM in (6.10) are plotted in Figure 6.10 as functions of the inversion level i_f.

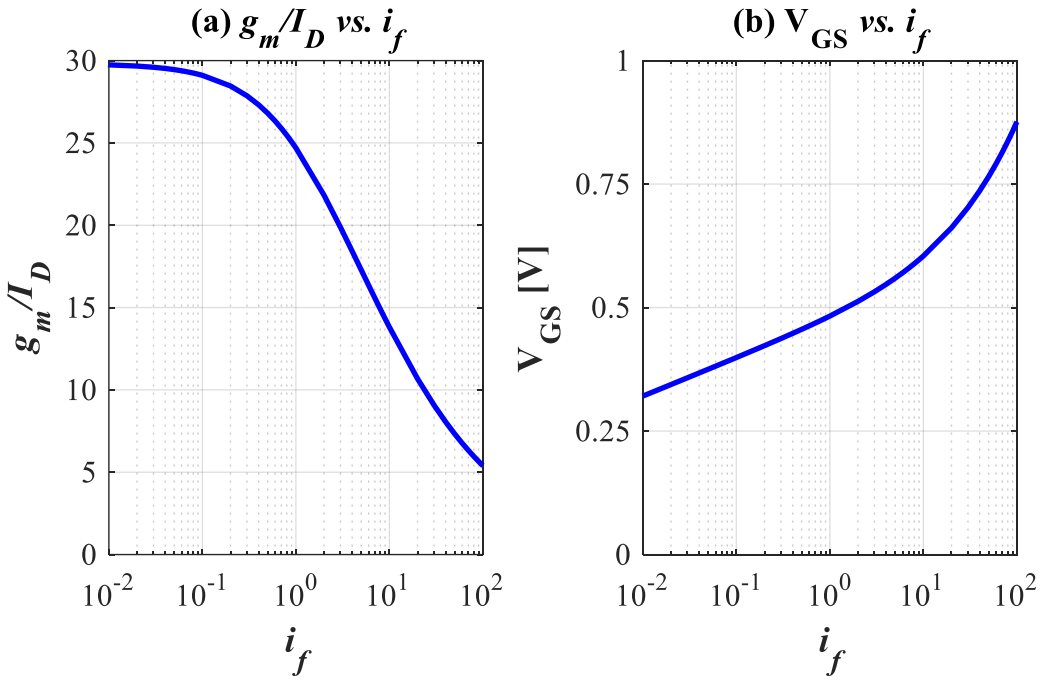

Figure 6.10. (a) g_m/I_D relationship and (b) V_{GS} as functions of the inversion level i_f.

6.4.2 Simulation Results

Figure 6.11 shows the complete circuit with defined component parameters.

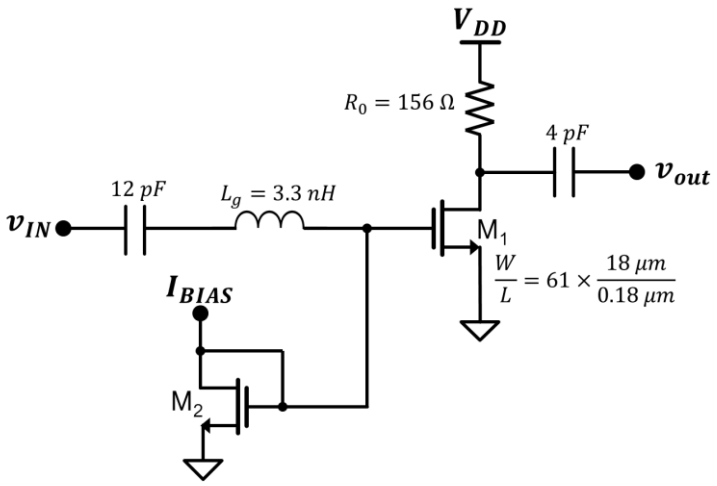

Figure 6.11. Implemented LNA circuit

There are several different analyses in Cadence® Virtuoso® to simulate RF circuits due to the agglomerate of parameters required to evaluate in RF designs. However, due to lack of experience using these different analyses and awareness that the design herein was oversimplified, the results presented in Figure 6.12 show the voltage gain and the noise figure NF.

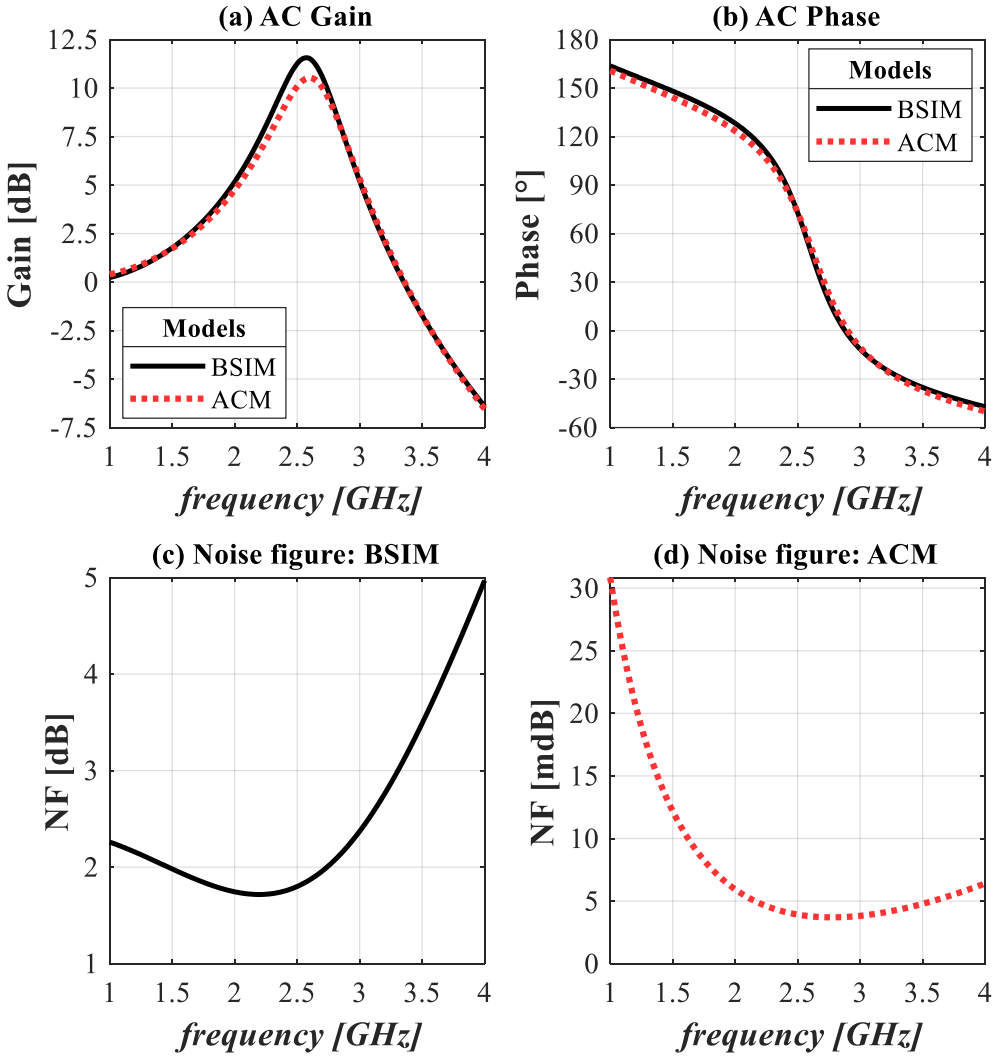

Figure 6.12. Results of frequency-domain simulations for LNA in Figure 6.11: (a) AC gain, (b) AC phase, (c) noise figure obtained for BSIM and for (d) ACM.

In Figure 6.12(a), the center frequency is $f_0 = 2.44\ GHz$ and the AC gain obtained is 10.5 dB for ACM and around 12 dB for BSIM. The phase was not taken into consideration through the design, though it is presented in Figure 6.12(b) to show that ACM managed to calculate the phase very closely to BSIM. It was found a difference of around 6° between ACM and BSIM at the center frequency.

Figure 6.12(c) presents the noise figure for the LNA using the BSIM model. At the center frequency, $NF < 2\ dB$ while $NF > 3\ dB$ starting from unity gain frequency $f_u = 3.25\ GHz$, which was previously calculated by (6.11) as $3.5\ GHz$.

$$f_t = \frac{g_m}{2\pi C_{gs}} \tag{6.11}$$

The noise figure presented in Figure 6.12(d) simply illustrates the lack of a noise model, which is yet to be included in Verilog-A description. Overall, the ACM model provided consistent results in relation to BSIM, even in frequency domain simulations, as demonstrated by the LNA presented in this section.

7 CONCLUSION AND NEXT STEPS

A simulation result is only as good as the model used; however, the transistor characteristics depend not only on a good model, but also on the values of its main parameters.

On circuit level simulations the ACM results were consistent to BSIM's. In fact, the experience of simulating the SBCS illustrated the importance of having more than one model at hand for circuit simulations. The discrepancy of BSIM and ACM on the occasion raised an alert to check what was wrong and to enforce that one should not blindly rely on simulation results.

The ACM model was also implemented on simulator in [5]; however, it was implemented within the simulator ELDO from Mentor Graphics. The code and functions were more complex and still difficult to associate design with simulation. Since a hardware description language was not used, the implementation was tailored for that simulator only.

In [35], on the other hand, the ACM was implemented in VHDL, a hardware description language not as compact as Verilog-A. The authors used the ACM charge density expressions to calculate the currents directly without the need of Algorithm 443 to solve a transcendental equation. However, despite using VHDL to facilitate the widespread of the model for use in other simulators, the charge density equations are not familiar to most of the designers; thus, the gap between design and simulation remained.

Unlike the work herein, authors of [5] and [35] did not extract the MOSFET parameters to use as inputs to the model; instead, they used over 10 parameters available in the simulator that were required to execute the ACM model.

Contrary to [35], the Verilog-A description implemented in this work calculates the current from the UICM, which presents design parameters used by IC designers. Not only the Verilog-A description is interchangeable with other simulators, but also allows a designer to test and play with the transistor parameters to assist on the learning and understanding of how each parameter influences the circuit behavior. In addition, it easily accepts parameter values extracted by chip measurements, a feature which is not available on any of the mentioned papers.

7.1 NEXT STEPS

Throughout this work, some ACM results were greatly different from BSIM's. The oscillator frequency results without inclusion of extrinsic capacitances, and the noise figure on the LNA case are some examples that could deserve some additional work.

Although both σ extraction methods provided similar values, the common source intrinsic gain and the $g_{md}/I_{D,sat}$ methods were proposed, described and implemented only in this work and through simulations. Thus, it would be advisable to validate these σ extraction methods through chip measurements.

Regarding the dynamic model, which expands the range of circuits that can be simulated using the ACM model, an extraction method to determine the transistor capacitances would be extremely useful.

Finally, a noise model could and should be implemented in the Verilog-A description as it would definitely be interesting to evaluate the noise in circuits using the ACM model. Mismatch and process variation could also be incorporated into the model for statistical analysis of corners and Monte Carlo.

There is plenty of room for improvement; however, the proposal of this work was to introduce a minimalist yet realistic model in the simulator. A model that required only 4 parameters was, overall, accomplished.

Besides the mentioned improvements, two main directions to follow from this work forward remain. One direction is to optimize the model for the ULV domain, which presents a large field of applications and room for innovations. The second direction is to include two extra parameters to model the intrinsic gain, namely the velocity saturation and the Early voltage.

This work, on itself, constitutes a collection of years of hard work and research summed up into one single piece, which presents how to go from design to simulation using the ACM model, while also enabling the designer to obtain the required parameters through automated simulation setups. As the title states, this work demonstrates and bridges the gap between design and simulation using the 4-parameter Advanced Compact MOSFET model.

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APPENDIX A – ACM MODEL FOR PMOS TRANSISTOR

Figure A.1 presents the symbol of a p-channel MOSFET transistor and its four terminals: gate (G), source (S), drain (D) and bulk (B).

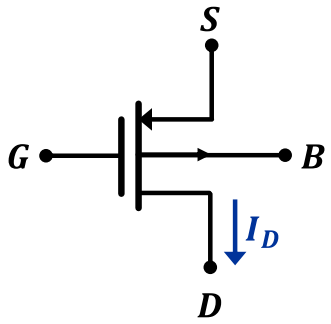

Figure A.1. Symbol of PMOS transistor

The drain current I_D flows through a long channel PMOS transistor from source to drain as illustrated in Figure A.1. As in section 3.1, I_D has two components: the forward current I_F and reverse current I_R, both dependent on the voltage V_{BG} between bulk and gate terminals. In addition, I_F depends on the voltage V_{BS} between bulk and source, whereas I_R depends on the voltage V_{BD} between bulk and drain. This source-drain symmetry is depicted in (A.1).

$$I_D = I_F - I_R = I(V_{BG}, V_{BS}) - I(V_{BG}, V_{BD}) = I_S\left(i_f - i_r\right) \tag{A.1}$$

The specific current I_S is dependent on geometry and technological parameters as given by (A.2) where μ_p is the PMOS carrier mobility, C'_{ox} is the oxide capacitance per unit area, ϕ_t is the thermal voltage and n is the slope factor. The aspect ratio S is the ratio between the width W and length L of the transistor's channel.

In a first order approximation, the technological parameters can be comprised in one factor denominated the sheet normalization current I_{SH}, which slightly depends on V_G through μ_p and n.

$$I_S = \mu_p C_{ox} n \frac{\phi_t^2}{2} \frac{W}{L} = I_{SH} \frac{W}{L} = I_{SH} S \tag{A.2}$$

The normalized form of the unified charge-control model (UCCM), expressed in (A.3), establishes the relationship between the voltages at the device terminals and the normalized inversion charge density at the source (drain) $q'_{IS(D)}$.

$$\frac{V_P - V_{BS(D)}}{\phi_t} = q'_{IS(D)} - 1 + \ln q'_{IS(D)} \tag{A.3}$$

$$q'_{IS(D)} = \sqrt{1 + i_{f(r)}} - 1 \tag{A.4}$$

Using equation (A.4) in (A.3) gives the unified current-control model (UICM), expressed in (A.5), which establishes the relationship between the voltages at the device terminals and the forward (reverse) inversion levels $i_{f(r)}$.

The pinch-off voltage V_P can be approximated by (A.6), where V_{T0} is the equilibrium threshold voltage that corresponds to the gate voltage for which $V_P = 0$, and σ is the magnitude of the DIBL factor.

$$\frac{V_P - V_{BS(D)}}{\phi_t} = \sqrt{1 + i_{f(r)}} - 2 + \ln\left(\sqrt{1 + i_{f(r)}} - 1\right) \tag{A.5}$$

$$V_P = \frac{V_{BG} - |V_{T0}| + \sigma V_{BD} + \sigma V_{BS}}{n} \tag{A.6}$$

APPENDIX B – ALL-REGION SMALL-SIGNAL TRANSCONDUCTANCES

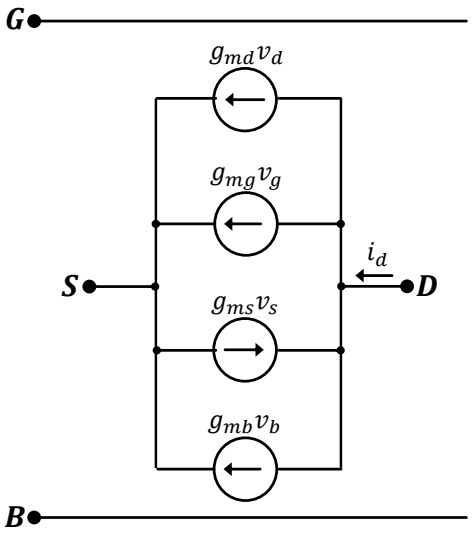

Figure B.1. Low-frequency small-signal model of the MOSFET

As mentioned in section 3.1.1, Figure B.1 presents the low-frequency small-signal model for MOSFET transistors, in which the variation of the drain current is expressed by (B.1), where g_{mg}, g_{ms}, g_{md} and g_{mb} are, respectively, the gate, source, drain and bulk small-signal transconductances given by (B.2) and v_g, v_s, v_d and v_b represent the small variations in the gate, source, drain and bulk voltages.

$$i_d = g_{mg}v_g - g_{ms}v_s + g_{md}v_d + g_{mb}v_b \tag{B.1}$$

$$g_{mg} = \frac{\partial I_D}{\partial V_G}\,, \qquad g_{ms} = -\frac{\partial I_D}{\partial V_S}\,, \qquad g_{md} = \frac{\partial I_D}{\partial V_D}\,, \qquad g_{mb} = \frac{\partial I_D}{\partial V_B} \tag{B.2}$$

$$g_m + g_{md} + g_{mb} = g_{ms} \tag{B.3}$$

The small-signal current variation is zero ($i_d = 0$) when the variation of the gate, source, drain and bulk voltages is the same, hence, (B.1) can be rewritten as (B.3).

The relationship between the transconductances and the inversion levels are obtained for all regions of operation by applying the partial derivatives of (B.2) in the UICM, as expressed from (B.4) to (B.6).

$$g_{ms} = -\frac{\partial I_D}{\partial V_S} = -\frac{\partial (I_F - I_R)}{\partial V_S} = -I_S\frac{\partial \left(i_f - i_r\right)}{\partial V_S} \tag{B.4}$$

$$g_{md} = \frac{\partial I_D}{\partial V_D} = \frac{\partial (I_F - I_R)}{\partial V_D} = I_S \frac{\partial \left(i_f - i_r\right)}{\partial V_D} \tag{B.5}$$

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{\partial (I_F - I_R)}{\partial V_G} = I_S \frac{\partial \left(i_f - i_r\right)}{\partial V_G} \tag{B.6}$$

The resulting transconductances are depicted in expressions from (B.7) to (B.9). Since the short-channel effect of DIBL is accounted for, an extra term of reverse current appears in g_{ms} as the saturation term appears in g_{md}.

$$g_{ms} = \frac{2I_S}{\phi_t}\left[\left(1 - \frac{\sigma}{n}\right)\left(\sqrt{1 + i_f} - 1\right) + \frac{\sigma}{n}\left(\sqrt{1 + i_r} - 1\right)\right] \tag{B.7}$$

$$g_{md} = \frac{2I_S}{\phi_t}\left[\frac{\sigma}{n}\left(\sqrt{1 + i_f} - 1\right) + \left(1 - \frac{\sigma}{n}\right)\left(\sqrt{1 + i_r} - 1\right)\right] \tag{B.8}$$

$$g_m = \frac{2I_S}{\phi_t}\left[\frac{1}{n}\left(\sqrt{1 + i_f} - \sqrt{1 + i_r}\right)\right] \tag{B.9}$$

Equation (B.10) reveals the gate transconductance in terms of the source and drain transconductances including the 4th parameter σ. Applying (B.10) in (B.3) gives the bulk transconductance, also expressed in (B.12).

$$g_m = \frac{g_{ms} - g_{md}}{n - 2\sigma} \tag{B.10}$$

$$g_{mb} = (n - 2\sigma - 1)g_m \tag{B.11}$$

$$g_{mb} = \frac{2I_S}{\phi_t}\left[\frac{n - 2\sigma - 1}{n}\left(\sqrt{1 + i_f} - \sqrt{1 + i_r}\right)\right] \tag{B.12}$$

APPENDIX C – DIBL EFFECT IN INTRINSIC CAPACITANCES

In Chapter 3, expressions (3.12)-(3.16) do not include the DIBL effect. The purpose of this section is to complete the dynamic model for the ACM 4- parameter model by including the DIBL factor in the capacitive coefficients, whose expressions were deduced based on the explanations from [2] and [6].

Expressions (3.12) and (3.13) for C_{gs} and C_{gd}, respectively, from the long channel model are presented again in (C.1) and (C.2) and will be referred to, in this section, as C_{gs0} and C_{gd0}, in which $\alpha = \frac{1+q_{iD}}{1+q_{iS}}$ and $C_{ox} = WLC'_{ox}$.

$$C_{gs0} = \frac{2}{3}C_{ox}\frac{(1+2\alpha)}{(1+\alpha)^2}\frac{q_{iS}}{(1+q_{iS})} \tag{C.1}$$

$$C_{gd0} = \frac{2}{3}C_{ox}\frac{\alpha^2+2\alpha}{(1+\alpha)^2}\frac{q_{iD}}{(1+q_{iD})} \tag{C.2}$$

The calculation of the capacitance coefficients is based on the unified charge-control model (UCCM) and on the quasi-static charge conserving model, which will not be explained herein, since references [2] and [6] already address the subject in depth. Expression (C.3) depicts the total inversion channel charge Q_I as a rational function of the forward and reverse charge densities Q'_F and Q'_R. The normalized inversion charge density at the source (drain) $q'_{IS(D)}$ presented on Chapter 3 relates to $Q'_{F(R)}$ as (C.4), in which $q'_{IS(D)} = -\frac{Q'_{IS(D)}}{nC'_{ox}\phi_t}$.

$$Q_I = WL\left[\frac{2}{3}\left(\frac{Q'^2_F + Q'_F Q'_R + Q'^2_R}{Q'_F + Q'_R}\right) + nC'_{ox}\phi_t\right] \tag{C.3}$$

$$Q'_{F(R)} = Q'_{IS(D)} - nC'_{ox}\phi_t = -nC'_{ox}\phi_t\left(1 + q'_{IS(D)}\right) \tag{C.4}$$

$$\frac{V_P - V_{S(D)B}}{\phi_t} = q'_{IS(D)} - 1 + \ln q'_{IS(D)} \tag{C.5}$$

From (C.3), (C.4) and the UCCM in (C.5), the capacitance coefficients $C_{gs(d)}$ can be calculated by solving the partial derivatives in (C.6). The results of the partial derivatives concerning the UCCM are shown in (C.7) and (C.8).

$$C_{gs(d)} = \frac{1}{n}\frac{\partial Q_I}{\partial V_{S(D)}} = \frac{1}{n}\left(\frac{\partial Q_I}{\partial Q'_F}\frac{\partial Q'_F}{\partial V_{S(D)}} + \frac{\partial Q_I}{\partial Q'_R}\frac{\partial Q'_R}{\partial V_{S(D)}}\right) \quad \text{(C.6)}$$

$$\frac{\partial Q'_{F(R)}}{\partial V_{S(D)}} = nC'_{ox}\left(1 + \frac{nC'_{ox}\phi_t}{Q'_F}\right)\left(1 - \frac{\sigma}{n}\right) \quad \text{(C.7)}$$

$$\frac{\partial Q'_{F(R)}}{\partial V_{D(S)}} = -nC'_{ox}\left(1 + \frac{nC'_{ox}\phi_t}{Q'_F}\right)\left(\frac{\sigma}{n}\right) \quad \text{(C.8)}$$

The gate-to-bulk capacitance C_{gb} is given by (C.9) and the partial derivatives to solve in relation to V_B are expressed in (C.10).

$$C_{gb} = \frac{1}{n}\frac{\partial Q_I}{\partial V_B} - \left(\frac{n-1}{n}\right)C'_{ox}(2\sigma + 1) \quad \text{(C.9)}$$

$$\frac{\partial Q_I}{\partial V_B} = \frac{\partial Q_I}{\partial Q'_F}\frac{\partial Q'_F}{\partial V_B} + \frac{\partial Q_I}{\partial Q'_R}\frac{\partial Q'_R}{\partial V_B} \quad \text{(C.10)}$$

The effect of the DIBL in the five intrinsic capacitances is summarized in expressions (C.11)-(C.15). The source-drain symmetry remained even with the addition of this short-channel effect and the relationship between $C_{bs(d)}$ and $C_{gs(d)}$ is equal to (3.15) and (3.16).

$$C_{gs} = \left(1 - \frac{\sigma}{n}\right)C_{gs0} - \frac{\sigma}{n}C_{gd0} \quad \text{(C.11)}$$

$$C_{gd} = \left(1 - \frac{\sigma}{n}\right)C_{gd0} - \frac{\sigma}{n}C_{gs0} \quad \text{(C.12)}$$

$$C_{gb} = \frac{n-1}{n}\left(C_{ox} - C_{gs0} - C_{gd0}\right) + \frac{2\sigma}{n}\left[(n-1)C_{ox} - C_{gs0} - C_{gd0}\right] \quad \text{(C.13)}$$

$$C_{bs} = (n-1)C_{gs} \quad \text{(C.14)}$$

$$C_{bd} = (n-1)C_{gd} \quad \text{(C.15)}$$

Figure C.1 presents expressions (3.12)-(3.14) in solid lines and expressions (C.11)-(C.13) in dotted lines obtained for a NMOS transistor with $\frac{W}{L} = \frac{18\,\mu m}{0.18\,\mu m}$, which presented $\sigma = 21.8\frac{mV}{V}$. It can be observed the effect of DIBL on the capacitance coefficients, which are consistent with the long channel results, despite the expected difference. For V_P between 0 and 1 V, the inclusion of the DIBL caused C_{gd} to achieve a negative value. Capacitances C_{bs} and

C_{bd} are not presented in Figure C.1 because no significant difference was observed between the results with and without DIBL.

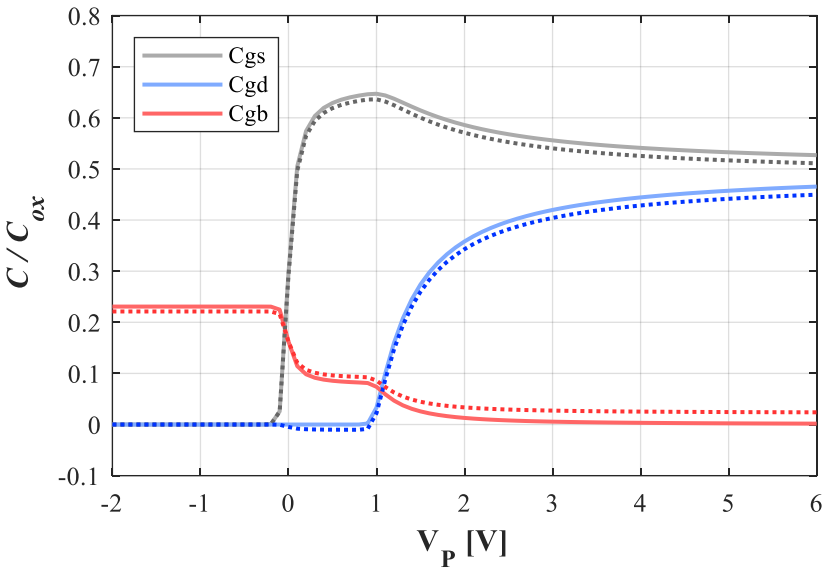

Figure C.1. Capacitances C_{gs}, C_{gd} and C_{gb} normalized by C_{ox} through a range for the pinch-off voltage from $-2\ V$ to $6\ V$, for $V_{DS} = 1\ V$. Results obtained using expressions (3.12)-(3.14) in solid lines and expressions (C.11)-(C.13) in dotted lines, for a transistor with $\frac{W}{L} = \frac{18\ \mu m}{0.18\ \mu m}$.

APPENDIX D – VERILOG-A DESCRIPTION OF ACM MODEL

This appendix presents the transcription of the Verilog-A files that describe the transistor cells used throughout this work. It includes the WI and all-region model versions of the NMOS transistor. Seeing the redundancy of description, the PMOS transistor versions were not included herein. The capacitances' values were taken directly from the foundry's documentation and are omitted due to the foundry's non-disclosure agreement.

D.1 WEAK INVERSION MODEL: NMOS

```
// VerilogA for masters2021_dev, nmos_acm_wi, veriloga
`include "constants.vams"
`include "disciplines.vams"

module nmos_acm_wi(G, D, S, B);
        // pinout definition
        inout B;
        inout D;
        inout G;
        inout S;
        // electrical nodes definition
        electrical B;
        electrical D;
        electrical G;
        electrical S;
        // user parameters
        real parameter ISH = 100e-9;
        real parameter W = 1e-6;
        real parameter L = 1e-6;
        real parameter VTH = 0.7;
        real parameter n =1;
        real parameter sigma = 0.026;
        // auxiliar variables
        real VP;
        real IS;
        analog begin
                PhiT = $vt($temperature);
                VP = (V(G,B) - VTH + sigma*V(D,S) + sigma*V(S,B) )/n;
                IS = ISH*W/L;
                I(D,S) <+ 2*IS*exp(1)*exp((vp-V(S,B))/PhiT)*(1-exp(-V(D,S)/PhiT));
        end
endmodule
```

D.2 ALL-REGION MODEL: NMOS

```
// VerilogA for masters2021_dev, nmos_acm_caps, veriloga
`include "constants.vams"
`include "disciplines.vams"

module nmos_acm_caps(B, D, G, S);
// pinout definition
inout B;
inout D;
inout G;
inout S;
// electrical nodes definition
electrical B;
electrical D;
electrical G;
electrical S;
// user parameters
real parameter ISH = 100e-9;
real parameter W = 1e-6;
real parameter L = 1e-6;
real parameter VTH = 0.7;
real parameter n =1;
real parameter sigma = 0.026;
// auxiliar variables
real VP;
real IS;
real X;
real Y;
real PhiT;
real WnS; // Used to calculate the if
real WnD; // Used to calculate the iR
real numeratorS;
real denominatorS;
real numeratorD;
real denominatorD;
real ZnS;
real ZnD;
real EnS;
real numeratorES;
real denominatorES;
real TermC;
real qiS;
real ifS;
```

```
real EnD;
real numeratorED;
real denominatorED;
real TermD;
real qiD;
real irD;
real ID;
// for dynamic model
real Cox;
real tox;
real e0;
real Cgs;
real Cgb;
real Cbs;
real Cbd;
real Cgd;
real Cgs_int;
real Cgb_int;
real Cbs_int;
real Cbd_int;
real Cgd_int;
real Cg_ext;
real Cb_ext;
real Cgo;
real Cgl;
real Cf;
real Cjb;
real Cjbsw;
real Cjbswg;
real Aeff;
real Peff;
real alpha; //channel linearity factor

        analog begin
                PhiT = $vt($temperature);
                VP = (V(G,B) - VTH + sigma*V(D,S) + sigma*V(S,B) )/n;
                IS = ISH*W/L;
                tox = 4e-9;
                e0 = 8.85e-12;
                Cox = 3.9*e0/tox;
                Cgo = ****;
                Cgl = ****;
                Cf = ****;
                Cjb = ****;
```

```
Cjbsw = ****;
Cjbswg = ****;
Aeff = ****;
Peff = ****.
////////////////////////////////////////////////////////////
//////// Condition to calculate WnS //////////
////////////////////////////////////////////////////////////
X = exp(((VP - V(S,B))/PhiT)+1);
if(X < 0.7385) begin
        numeratorS = X + (4/3)*X*X;
        denominatorS = 1 + (7/3)*X+(5/6)*X*X;
        WnS = numeratorS/denominatorS;
end
else begin
        numeratorS = ln(X)*ln(X)+2*ln(X)-3;
        denominatorS = 7*ln(X)*ln(X) + 58*ln(X) +127;
        WnS = ln(X) - 24*(numeratorS/denominatorS);
end

// Calculating ZnS
ZnS = ln(X) - WnS - ln(WnS);
// Calculating EnS
TermC = ZnS/(1 + WnS);
numeratorES = 2*(1+WnS)*(1+WnS+(2/3)*ZnS)-ZnS;
denominatorES = 2*(1+WnS)*(1+WnS+(2/3)*ZnS)-2*ZnS;
EnS = TermC*(numeratorES/denominatorES);
// Finding the qis and ifS
qiS = WnS*(1+EnS);
ifS = (qiS + 1)*(qiS + 1) - 1; // Equation 2.2.3
////////////////////////////////////////////////////////////
//////// Condition to calculate WnD //////////
////////////////////////////////////////////////////////////
Y = exp(((VP - V(D,B))/PhiT)+1);
if(Y < 0.7385) begin
        numeratorD = Y + (4/3)*Y*Y;
        denominatorD = 1 + (7/3)*Y+(5/6)*Y*Y;
        WnD = numeratorD/denominatorD;
end
else begin
        numeratorD = ln(Y)*ln(Y)+2*ln(Y)-3;
        denominatorD = 7*ln(Y)*ln(Y) + 58*ln(Y) +127;
        WnD = ln(Y) - 24*(numeratorD/denominatorD);
end
```

```
                // Calculating ZnD
                ZnD = ln(Y) - WnD - ln(WnD);
                // Calculating EnD
                TermD = ZnD/(1 + WnD);
                numeratorED = 2*(1+WnD)*(1+WnD+(2/3)*ZnD)-ZnD;
                denominatorED = 2*(1+WnD)*(1+WnD+(2/3)*ZnD)-2*ZnD;
                EnD = TermD*(numeratorED/denominatorED);
                ////////////////////////////////////////////////////////////
                // Finding the qid and irD
                qiD = WnD*(1+EnD);
                irD = (qiD + 1)*(qiD + 1) - 1;
                ////////////////////////////////////////////////////////////
                ////////////// Calculating ID ////////////////////////
                ////////////////////////////////////////////////////////////
                ID = IS*( ifS – irD );
                I(D,S) <+ ID;
                ////////////////////////////////////////////////////////////
                /////////////// Dynamic model ////////////////////
                ////////////////////////////////////////////////////////////
                // Intrinsic caps
                alpha = (1 + qiD)/(1 + qiS);
                Cgs_int = (2/3) * W*L*Cox * ( (1 + 2*alpha) * qiS )/( (1+alpha)*(1+alpha)*(1+qiS) );
                Cgd_int = (2/3) * W*L*Cox * ( (alpha*alpha + 2*alpha) * qiD )/( (1+alpha)*(1+alpha)*(1+qiD) );
                Cgb_int = ( (n-1)/n )*(W*L*Cox - Cgs_int - Cgd_int);
                Cbs_int = (n-1)*Cgs_int;
                Cbd_int = (n-1)*Cgd_int;
                // Extrinsic caps
                Cb_ext = Aeff*Cjb + Peef*Cjbsw + W*Cjbswg;
                Cg_ext = (Cgo+Cgl+Cf)*W;
                // Total caps:
                Cgs = Cgs_int + Cg_ext;
                Cgd = Cgd_int + Cg_ext;
                Cgb = Cgb_int;
                Cbs = Cbs_int + Cb_ext;
                Cbd = Cbd_int + Cb_ext;
                // current through caps: I(p,n) <+ capacitance * ddt(V(p,n))
                I(G,S) <+ Cgs * ddt( V(G,S) );
                I(G,D) <+ Cgd * ddt( V(G,D) );
                I(G,B) <+ Cgb * ddt( V(G,B) );
                I(B,S) <+ Cbs * ddt( V(B,S) );
                I(B,D) <+ Cbd * ddt( V(B,D) );
        end
endmodule
```