Modeling a nanometer FD-SOI transistor with a basic all-region MOSFET model

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***Abstract*—The suitability of a basic, long channel, compact, bulk transistor model coupled with look-up-tables (LUTs) for application to a 28 nm FD-SOI technology is evaluated through simulations. The parameters comprising the LUTs are extracted as a function of the channel length and back-plane voltage, with very simple standard procedures intended for long channel transistors. The resulting model proved to be a simple, but very accurate way to describe the $\mathbf{g_m/I_D}$ curve in the moderate and weak inversion regions, with a straightforward analytical expression, even for minimum length transistors. This approach coupled with a LUT approach for the $\mathbf{I_D/g_{ds}}$ ratio, provides the main small signal model for design. It was also confirmed that reasonably accurate modeling of the intrinsic capacitances require a more complete modeling of the device.**

***Index Terms*—MOSFET model, FD-SOI, gm/ID methodology, weak inversion, moderate inversion**

I. Introduction

The capability to estimate circuit performance and explore the design space in all inversion regions of the MOS transistor is key for gaining insight and optimizing the design of analog and RF circuits. A widespread approach is based on the g_m/I_D method [1], [2]. When aiming at nanometer processes, the transistor characteristics may be captured on look-up-tables (LUTs) [2], [3]. In this way the complexity of second order modeling effects in nanometer processes, and in particular short channel effects, are dealt with by using different LUTs depending on the target transistor length (or range of lengths) and, in some cases, depending also on the bias drain voltage.

A step further from the pure LUT approach would be to have analytical expressions for the transistor model. In this way analytical derivations can be performed providing further insight and understanding in the design process. However, complete analytical models, including all second order effects, are not suitable for analytical circuit design due to their complexity. This work explores, therefore, an intermediate way. Could a basic (long channel) all-inversion-regions, compact model, coupled with a LUT that defines their parameters as a function of the transistor length, be applied to model an advanced nanometer process? Such basic model does not consider effects such as mobility reduction and velocity saturation that will be significant in the strong inversion (SI) region. Nevertheless, considering the very high transition frequency of short channel transistors in a nanometer process, for many analog and RF circuits, even for frequencies up to several GHz, the optimum operating point occurs in the moderate inversion (MI) or even weak inversion (WI) regions [1], [2]. This is the case of ultra low power or ultra low voltage circuits. Therefore, an analytical model that allows to reasonably fit the transistor characteristics in WI and MI would be enough and useful in several cases.

The nanometer process considered is a fully depleted, silicon on insulator (FD-SOI), ultra thin body and buried oxide (UTBB) 28 nm process. This implies, on one hand, an additional challenge, since we will attempt to describe an FD-SOI device with a bulk MOS model. This challenge will be further discussed in Section III. On the other hand, FD-SOI largely reduces short channel effects [4], which helps to make viable the approach discussed in this work. The device performance for extraction of the model parameters and the assessment of model results is based on simulations performed with the foundry provided model in the Spectre simulator.

The paper is organized as follows. Section II presents a brief review of the applied basic compact model (the ACM model) and parameter extraction procedure. Section III describes how this model is applied to the considered process, the results of the parameter extraction and how the parameters vary. In Section IV, the results of the model are compared to simulation results for the small signal parameters, capacitances and transition frequency. Finally, in Section V the main conclusions are summarized.

II. Basic ACM model and parameter extraction

In this section the ACM model [5], which is the basic (long channel) compact model applied, and the procedure for parameter extraction, are briefly reviewed. This model is a bulk MOS transistor model, later it will addressed how it is applied to the FD-SOI transistor. In the ACM model the drain current of a long-channel transistor is expressed as the sum of two currents, namely, the forward and reverse currents [5], as follows

$$I_D = I_F - I_R = I_S(i_f - i_r), \tag{1}$$

where I_S (called specific current) is given by

$$I_S = \mu\, n\, C'_{ox}\, \frac{\phi_t^2}{2}\, \frac{W}{L} \tag{2}$$

and i_f and i_r are the forward and reverse inversion coefficients respectively.

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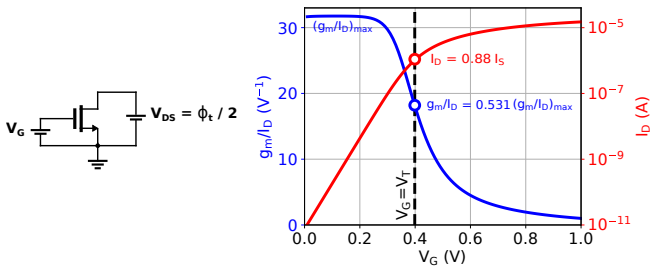


(a) (b)

Fig. 1. (a) Circuit schematic and (b) graphical representation of the g_m/I_D procedure for the extraction of V_T.

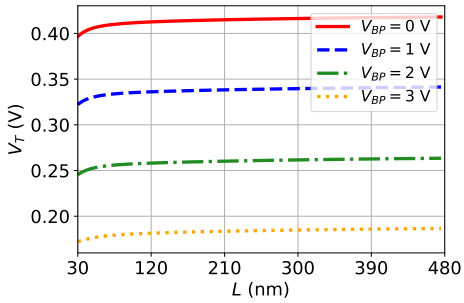


Fig. 2. Results of the extraction of V_T, according to the g_m/I_D procedure, as a function of the channel length L of an nMOS transistor with a channel width $W = 500$ nm, for several values of the back-plane voltage V_{BP}.

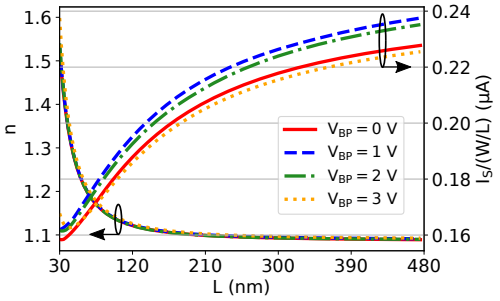


Fig. 3. Results of the extraction of the normalized I_S and the slope factor n, according to the g_m/I_D procedure, as a function of the channel length L of an nMOS transistor with a channel width $W = 500$ nm, for several values of the back-plane voltage V_{BP}.

In (2), μ is the mobility, n is the slope factor, C'_{ox} is the oxide capacitance per unit area, ϕ_t is the thermal voltage and W/L is the aspect ratio.

The relationship between the terminal voltages V_G, V_S, V_D (all referred to the bulk) and the inversion coefficients is [5]

$$\frac{V_P - V_{S(D)}}{\phi_t} = \sqrt{1 + i_{f(r)}} - 2 + \ln\left(\sqrt{1 + i_{f(r)}} - 1\right), \quad (3)$$

where the pinch-off voltage V_P can be approximated by $V_P \cong (V_G - V_T)/n$, being V_T the threshold voltage at $V_S = 0$.

The g_m/I_D ratio can be expressed as

$$\frac{g_m}{I_D} = \frac{1}{I_D}\frac{\partial I_D}{\partial V_G} = \frac{g_{ms} - g_{md}}{nI_D}, \quad (4)$$

leading to

$$\frac{g_m}{I_D} = \frac{2}{n\phi_t\left(\sqrt{1 + i_f} + \sqrt{1 + i_r}\right)}. \quad (5)$$

For parameter extraction, the g_m/I_D based procedure described in [6] is followed, where the authors propose to extract the technology parameters n, V_T and I_S using $V_{SB} = 0$, $V_{DB} = \phi_t/2$, sweeping V_{GB} (as shown in Fig. 1a) and plotting I_D and g_m/I_D with respect to V_{GB} (as shown in Fig. 1b). The extraction of the parameters is then based on the following relationships.

From (5), as $i_f > 0$ and $i_r > 0$, then $(g_m/I_D)_{max}$ is equal to $1/(n\phi_t)$.

For $V_{SB} = 0$ and $V_{GB} = V_T$ (which implies $V_P = 0$), we obtain $i_f = 3$ from (3). For $V_{DS} = \phi_t/2$, $V_{SB} = 0$ and $V_{GB} = V_T$ we obtain $i_r = 2.12$ from (3). For these values of i_f and i_r, we have $g_m/I_D = 0.531/(n\phi_t)$ from (5) and $I_D = 0.88 I_S$ from (1).

So the parameters are extracted as follows. First, $n = 1/(\phi_t (g_m/I_D)_{max})$, then V_T such that $g_m/I_D\,(V_{GB} = V_T) = 0.531/(n\phi_t)$ is determined and, finally, $I_S = I_D\,(V_{GB} = V_T)/0.88$.

III. Parameter Extraction for FD-SOI Nanometer Device

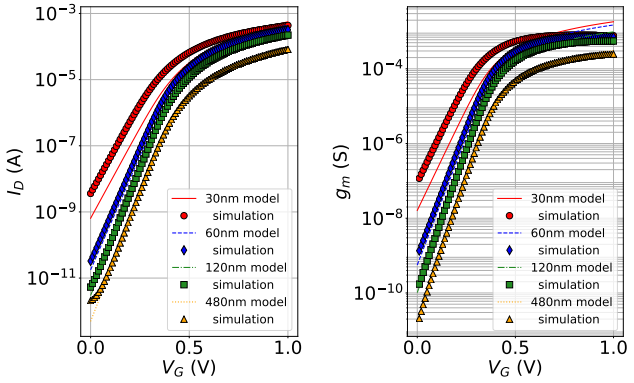
In order to apply the ACM model bulk MOS transistor model to the FD-SOI device, we will consider the ACM model with $V_S = 0$ (i.e. null source to bulk voltage). Equivalently, we are considering the gate and drain voltage of the FD-SOI transistor referred to the source. The slope factor n, the threshold voltage V_T and the specific current I_S are extracted using the procedure depicted in Section II for different channel lengths L and back-plane voltages V_{BP} (also referred to the source). Results, for low V_T transistors, are shown in Figs. 2 and 3.

It can be seen in Fig. 3, that n has little variation with V_{BP}, as has been shown by prior works such as [7], [8], n is very high, up to 1.5, (i.e. the subthreshold slope is degraded) for the minimum channel length but n decreases fast as the channel length increases, reaching typical values of FD-SOI of 1.1. The threshold voltage varies with V_{BP}, as expected [4] and has a slight dependence on the channel length, showing the improved (decreased) short channel effects in FD-SOI. Figure 3 shows the specific current, given in (2), divided by the aspect ratio. There is moderate variation with V_{BP} and a significant dependence on L.

IV. Comparison of the Model Against Simulations

An insightful case with the transistor in saturation, for $V_{DS} = 0.6$ V, was simulated and the results are compared to those obtained with the model.

Figure 4a compares model and simulation for the I_D vs. V_G characteristic for several values of channel length L. Even though the I_D of a minimum channel length transistor (L =30 nm) is not well predicted by the model, it works fine



(a) (b)

Fig. 4. Simulation and model results of (a) I_D and (b) g_m, for several values of L, with $W = 500$ nm, $V_{DS} = 0.6$ V and $V_{BP} = 0$ V.

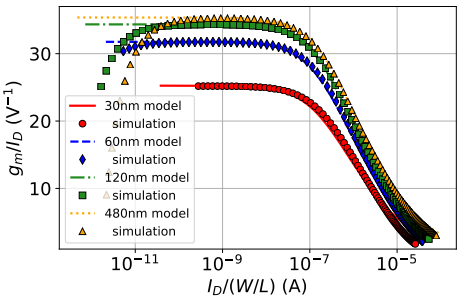


Fig. 5. Simulation and model results of g_m/I_D for several values of L, with $W = 500$ nm, $V_{DS} = 0.6$ V and $V_{BP} = 0$ V.

for $L \geq 60$ nm. The same trend occurs with the transconductance in Fig. 4b.

A. Small signal parameters

Figure 5 shows g_m/I_D as a function of the normalized drain current. The model fits the simulations for all transistor lengths in all inversion regions except for deep weak inversion and deep strong inversion. The former, with $I_D/(W/L) < 10$ pA, where the leakage current dominates, making this region a very unlikely design choice. The latter, with $g_m/I_D < 6$ V^{-1}, exhibits a difference between the model and the simulation due to mobility reduction and velocity saturation.

The relative error in g_m/I_D, between the model and the simulations, is depicted in Fig. 6. It can be seen that the model provides a reasonable approximation (relative error less than 7 %) of the g_m/I_D characteristic of the full simulation model in WI and MI, for $g_m/I_D \geq 6$ V^{-1}.

The ratio g_m/I_D proves to be fairly independent of V_{BP}, as has been shown by prior works such as [7], [8], because of its independence on the threshold voltage. The simulation results depicted in Fig. 7 are consistent with this.

The considered basic ACM model does not include the second order effects that define the output conductance. Therefore, in the proposed approach the output conductance will be considered fully based on a LUT of the I_D/g_{ds} ratio [2],

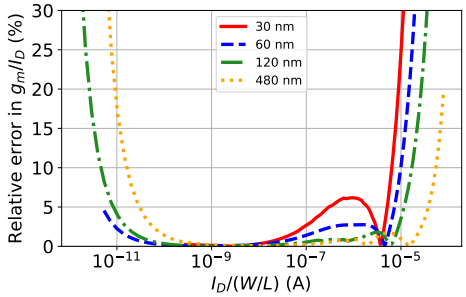


Fig. 6. Relative error in g_m/I_D, between the model and the simulation results, for several values of L with $W = 500$ nm, $V_{DS} = 0.6$ V and $V_{BP} = 0$ V.

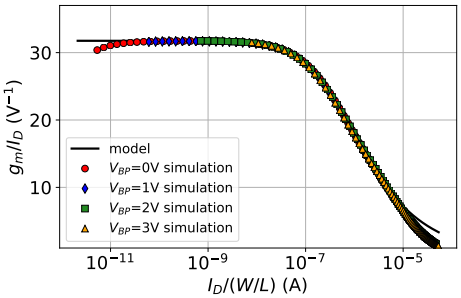


Fig. 7. Simulation and model results of g_m/I_D for several values of V_{BP}, with $W = 500$ nm, $L = 60$ nm and $V_{DS} = 0.6$ V.

[3], which can be interpreted as the Early voltage. This LUT will have as inputs L, V_{BP} and g_m/I_D (or alternatively $I_D/(W/L)$). The evolution of the I_D/g_{ds} ratio with L and V_{DS} is shown in Fig. 8 for an MI operating point. It can be seen that taking a constant Early voltage extracted at a given V_{DS} (e.g. 0.6 V) would be only acceptable if the V_{DS} range is small. Otherwise the LUT should also consider the V_{DS} dependence.

B. Intrinsic small signal capacitances

In order to assess the performance of the modeling approach regarding the intrinsic small signal capacitances, the main

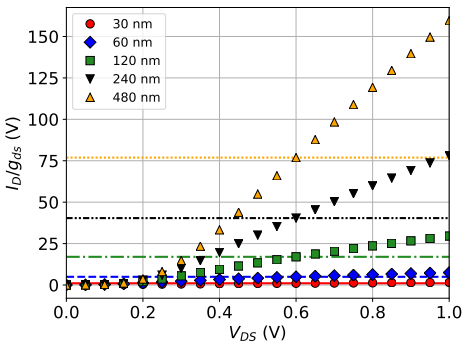


Fig. 8. Simulation results of the Early voltage for several values of L, with $W = 500$ nm, $g_m/I_D = 15$ V^{-1} and $V_{BP} = 0$ V. The horizontal lines are the result of approximating the Early voltage at $V_{DS} = 0.6$ V.

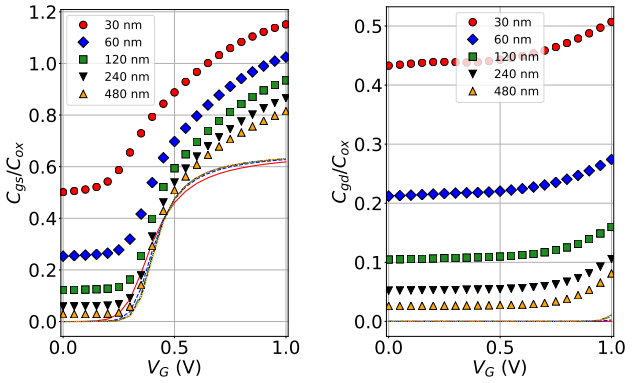


Fig. 9. Simulation (markers) and model (lines) results of the normalized intrinsic capacitances (a) C_{gs} and (b) C_{gd} for several values of L, with $W = 500$ nm, $V_{DS} = 0.6$ V and $V_{BP} = 0$ V.

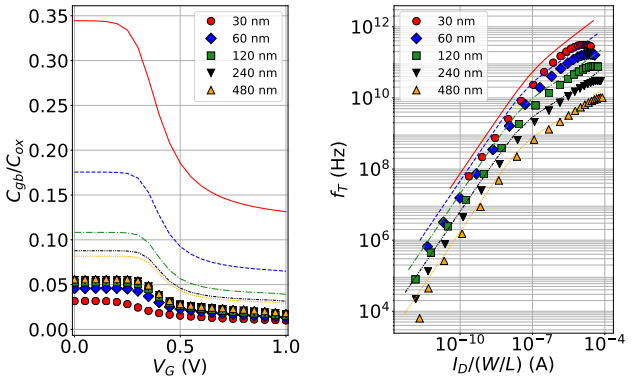


Fig. 10. Simulation (markers) and model (lines) results of (a) the normalized intrinsic capacitance C_{gb} and (b) the transition frequency f_T, for several values of L, with $W = 500$ nm, $V_{DS} = 0.6$ V and $V_{BP} = 0$ V.

components of the total gate capacitance are considered. These are: gate to source, gate to drain and gate to bulk. In the case of the gate to bulk capacitance of the ACM model, it is associated to the gate to back-plane capacitance of the FD-SOI device. The expressions of these capacitances as presented in [5] as a function of i_r and i_f lead to the results shown in Figs. 9a, 9b and 10a.

Note in Fig. 9b that C_{gd} is estimated by the model to be zero in saturation, since the effect of the drain voltage on the transistor charges is neglected in saturation in the basic long channel model. In the simulation results in Fig. 9b, it is noticeable that the effect of the drain voltage in saturation is very significant, particularly for shorter channels. This modeling limitation also impacts the other capacitances. This can be seen, either because the part of the channel charge in saturation controlled by the source changes or considering that the three components of the gate capacitance are related by [5]:

$$C_{gb} = \frac{n-1}{n}(WLC'_{ox} - C_{gs} - C_{gd}). \qquad (6)$$

Furthermore, in this nanometer process, this relationship will be influenced by the change in the inversion charge depth in the Si film with bias voltage [4]. These effects mean a significant intrinsic C_{gd} and modified C_{gs} and C_{gb}. The overall result is that C_{gs} is underestimated and C_{gb} is overestimated.

Figure 10b shows the model predicted and simulated transition frequency.

V. Conclusion

It was presented and assessed a modeling approach which applies a basic, long channel, bulk transistor model coupled with LUTs for the three parameters as a function of the length and back-plane voltage. The parameters were extracted with very simple, standard procedures, intended for long channel transistors. The resulting model proved to be a simple, but very accurate way for describing the g_m/I_D curve in the MI and WI regions, which is the basis for transistor dimensioning. This was achieved even for minimum length transistors in a 28 nm FD-SOI technology. This allows to perform analytical derivations based on the g_m/I_D characteristic in nanometer technologies for low-power and low-voltage applications. This approach coupled with an LUT approach for the output conductance provides the main small signal model for design. It was also confirmed that reasonably accurate modeling of the intrinsic capacitances require a more complete modeling of the device.

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