MOSFET Threshold Voltage: Definition, Extraction, and Applications

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Abstract

This paper develops a procedure for MOS transistor characterization that allows the direct determination of the threshold voltage. The proposed method is insensitive to second order effects since it is based on the measurement of the channel conductance-to-current ratio in the linear region of operation at low current. The new technique is compared with other two 'current-based' extraction procedures and some applications are presented.

Keywords: threshold voltage, MOSFET characterization, parameter extraction

1 INTRODUCTION

The threshold voltage V_T is a fundamental parameter in the characterization of MOS transistors and should be used, whatever the adopted model for the transistor is. The classical definition of threshold, $\phi_s = 2\phi_F + V$, which links the surface, the Fermi, and the channel potentials is indeed 'surface-potential based'.

V_T represents a physical change in the phenomenon that prevails in the current flow through the device as it goes from weak to strong inversion. Since this transition is very gradual, no remarkable point can be directly identified as the threshold voltage in the I_D vs. V_G characteristic. This is one of the reasons why different definitions of threshold voltage have been presented in the literature [1]. Another reason is the sometimes poor modeling, since to extract unambiguously V_T it is essential that the model includes the drift and diffusion transport mechanisms, both important near the threshold condition.

In this study we first recall the current-based threshold voltage definition (equality between the drift and diffusion components of drain current) and compare it to the classical surface potential based definition.

Then we summarize a new procedure for the characterization of MOS transistors, which allows the direct determination of the (current-based) threshold voltage and some other important electrical parameters with minimum influence of second order effects. In the new procedure, the threshold voltage is determined at a constant gate-to-substrate voltage, at a low drain-to-source voltage and with the transistor operating in the weak and moderate inversion regions. The new method will be compared with two other 'current-based' procedures. Finally, we present some applications.

2 CURRENT-BASED THRESHOLD DEFINITION

The weak inversion current in MOSFET is essentially due to the carrier diffusion, whereas the strong inversion current is mostly due to the carrier drift, as shown in Fig. 1.

At some point the drift and diffusion components of the current are equal. Taking this point to define the threshold is very appropriate [2-4].
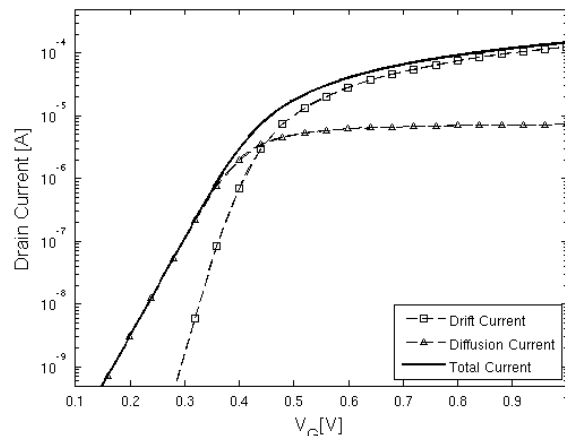

Figure 1: Drain current and its diffusion and drift components vs. gate voltage for a MOSFET operating in the linear region with $V_{DS} = \frac{\phi_t}{2} = 13\text{mV}$.

For planar bulk MOS transistors there is a small difference of the order of the thermal voltage ϕ_t between the classical and the current-based threshold voltages, as shown in Table 1 [5].

3 THE g_{ds}/I_D PROCEDURE

The circuit configuration used to determine the channel conductance-to-current ratio g_{ds}/I_D in the linear region is shown in Fig. 2.

Physical Meaning	Value of ϕ_S at threshold	Value of Q_I' at threshold	Difference in V_T relative to the classical definition
Surface concentration of electrons= bulk concentration of holes	$2\phi_F + V$	$-(n-1)C_{ox}'\phi_t$	0
Drift component = Diffusion component of Drain current	$2\phi_F + V + \phi_t \ln\left(\dfrac{n}{n-1}\right)$	$-nC_{ox}'\phi_t$	$\phi_t\left[1+n\ln\left(\dfrac{n}{n-1}\right)\right]$

Table 1: Classical and current-based threshold definitions [5]. C'_{ox} is the oxide capacitance per unit area, Q'_I is the inversion charge per unit area and n is the slope factor.

The drain current I_D at a constant V_{DS} (= $\phi_t/2$) voltage is measured as a function of source-substrate voltage V_S, as shown in Fig. 2.
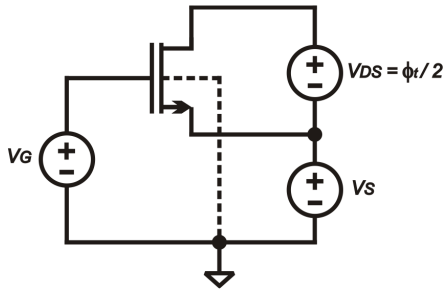

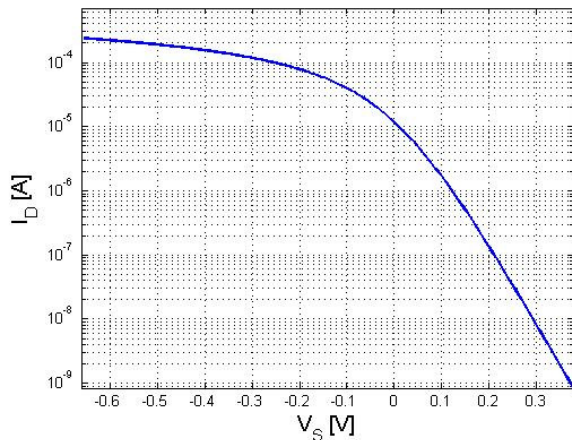Figure 2: Circuit configuration for measuring the common-gate characteristics in the linear region.

Figure 3: Drain current vs. source voltage for V_{DS}=13 mV at room temperature, V_G= 0.42 V, L_m= 0.5 µm (mask channel length), W= 12 µm, TSMC – 0.35 µm technology.

Variable	Expression	
Drain current	$I_D = I_F - I_R = I_S\left(i_f - i_r\right)$	(1)
Specific Current	$I_S = \mu n C_{ox}' \dfrac{\phi_t^2}{2}\dfrac{W}{L}$	(2)
Source (drain) transconductance	$g_{ms(d)} = \dfrac{2I_S}{\phi_t}\left(\sqrt{1+i_{f(r)}}-1\right)$	(3)
Source (drain)-to-bulk voltage	$V_P - V_{S(D)} = \phi_t\left[\sqrt{1+i_{f(r)}} - 2 + \ln\left(\sqrt{1+i_{f(r)}}-1\right)\right]$	(4)
Pinch-off voltage	$V_P \cong \dfrac{V_G - V_T}{n}$	(5)

Table 2: Long-channel MOSFET expressions [3]. μ is the mobility, W is the channel width, L is the channel length.

For the circuit in Fig.2, the variation of the drain current is

$$\Delta I_D = -g_{ms}\Delta V_S + g_{md}\Delta V_D \tag{6}$$

where g_{ms} and g_{md} are the source and drain transconductance, respectively.

Since in our case $\Delta V_D = \Delta V_S$, we can calculate the channel conductance-to-drain current ratio from Eqs. (1) and (3) as

$$\frac{g_{ds}}{I_D} = -\frac{1}{I_D}\frac{dI_D}{dV_S} = \frac{2}{\phi_t\left(\sqrt{1+i_f}+\sqrt{1+i_r}\right)} \tag{7}$$

For V_{DS} much lower than the thermal voltage ϕ_t, $i_f \cong i_r$ and (7) becomes

$$\frac{g_{ds}}{I_D} = \frac{1}{\phi_t\sqrt{1+i_f}} \tag{8}$$

Thus, for i_f=3 the channel conductance-to-current ratio is one-half of the peak value $1/\phi_t$. In order to account for the

error introduced by a non-neglible V_{DS}, we can use Eq. (4) to calculate $i_r = 2.12$ and $g_{ds}/I_D = .531/\phi_t$ for $i_f = 3$. At this point of the g_{ds}/I_D curve $V_S = V_P$ and $I_S = 1.136 * I_D$ as can be easily verified using Eqs. (1) and (5).

Finally, V_T is the gate voltage at which the condition $V_P = 0$ holds (see Eq. (5)).

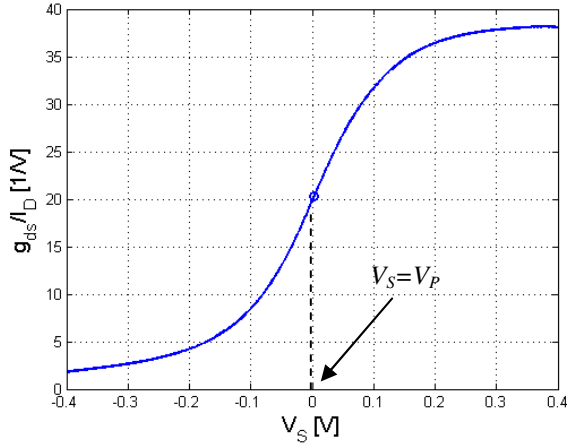Fig. 4 shows the g_{ds}/I_D curve as a function of V_S, with the indication of the point where $V_S = V_P$

Figure 4. g_{ds}/I_D as a function of the V_S, for the same transistor used in the Fig. 3. The circle indicates the point where $V_S = V_P$.

4   COMPARISON OF THE DIFFERENT CURRENT-BASED EXTRACTION METHODS

The g_m/I_D method in [3] uses the transistor in the linear region and exploits the transconductance-to-current ratio characteristic. The advantage of the use of the channel conductance instead of the transconductance is that the extraction is independent of the slope factor (body factor) since V_{GB} is kept constant during the measurement. Figure 5 shows the plot of the g_m/I_D and g_{ds}/I_D characteristics.
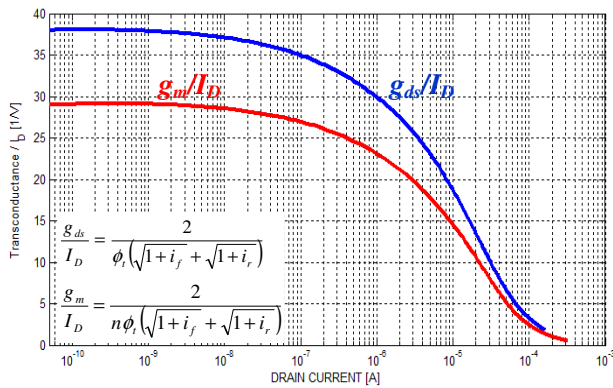

Figure 5: Comparison between g_m/I_D and g_{ds}/I_D as a function of the drain current using the BSIM3V3 model for NMOS transistor with $W/L = 125$ in a TSMC – 0.35 µm.

The constant current (CC) method [3] is the simplest one to extract the threshold voltage. In this method, the MOSFET in the diode connection is biased with a constant drain current ($I_D = 3 * I_S$) (Fig. 6), and, as a consequence, $V_S = V_P$ and $V_G = V_T$ for $V_S = 0$.
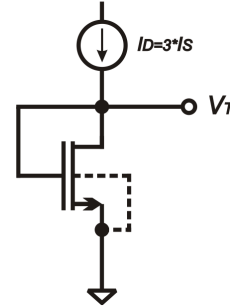

Figure 6: Constant current circuit configuration for measuring the threshold voltage .

The V_T values extracted from the g_m/I_D, g_{ds}/I_D and constant current methods, are shown in Fig. 7. In this figure, we can observe that the V_T values from these methods present similar behaviors, especially for g_m/I_D and g_{ds}/I_D methods.
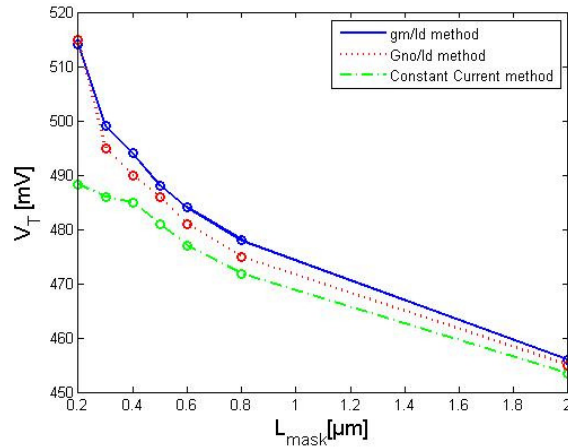

Figure 7: Measured V_T values vs. mask channel length for g_m/I_D, g_{ds}/I_D and constant current methods for NMOS transistors with L_m ranging from 0.2 µm to 2 µm and $W/L = 100$, in a TSMC – 0.18 µm technology.

5   APPLICATIONS

The threshold voltage is a fundamental electrical parameter used in technology characterization, aging evaluation, matching assessment and in temperature and radiation sensors.

As an example of matching assesment, 20 matched NMOS transistors were measured and the V_T was extracted using the g_m/I_D and CC methods.
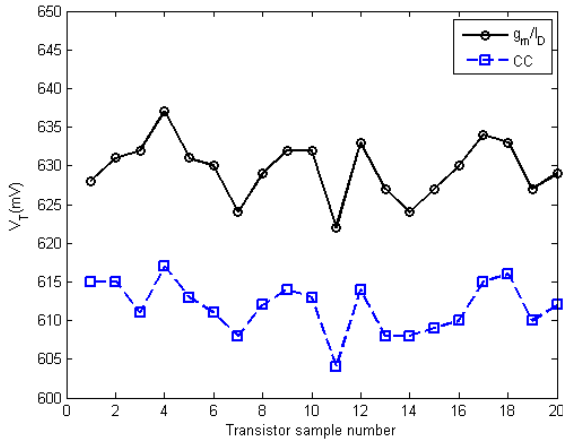

Figure 8: V_T measurements using g_m/I_D and constant current (*CC*) methods for 20 matched NMOS transistors (*W*=12 µm and L_m=0.5 µm – TSMC 0.35 µm) at room temperature. The V_T average values were 629mV (g_m/I_D) and 611.5mV (*CC*) and the relative standard deviation was 0.59%(g_m/I_D) and 0.55% (*CC*).

Fig. 8 shows that both methods present similar behavior and almost the same relative standard deviation. The *CC* method is interesting because it is very simple and rapid. In fact, the *CC* method can be used as a V_T extractor circuit for tracking the V_T variation as a function of a specific parameter, *e.g.* temperature or ionizing radiation.

An example of the usage of *CC* method to study the effect of temperature is presented in Fig. 9. It is important to note that the specific current is dependent on temperature (4). Due to this reason, the biasing current (I_D=3*I_S) was determined, through electrical simulation, for each temperature.
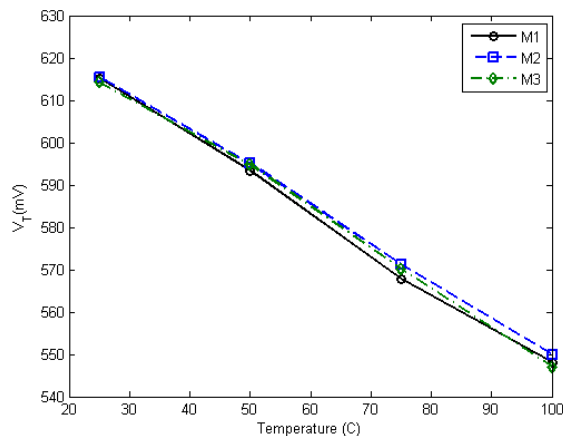

Figure 9: V_T measurements using constant current (*CC*) methods vs. temperature for 3 matched NMOS transistors (M1, M2, M3) with *W*=12 µm and L_m=0.5 µm – TSMC 0.35 µm.

From Fig.9 we can observe that the V_T thermal coefficient is approximately -0.9 mV/°C.

6 CONCLUSION

A new procedure for the direct determination of the threshold voltage with minimum influence of second order effects is introduced.

The threshold voltage is determined at a constant gate-to-substrate voltage, at a low drain-to-source voltage and with transistor operation in the weak and moderate inversion regions. Under these operating conditions the effects of series resistances, mobility and slope factor variations, and channel length modulation are practically negligible, allowing a direct determination of the threshold voltage.

Aditionally, the current-based extraction in weak-moderate inversion allows the design of low power V_T extractor circuits.

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