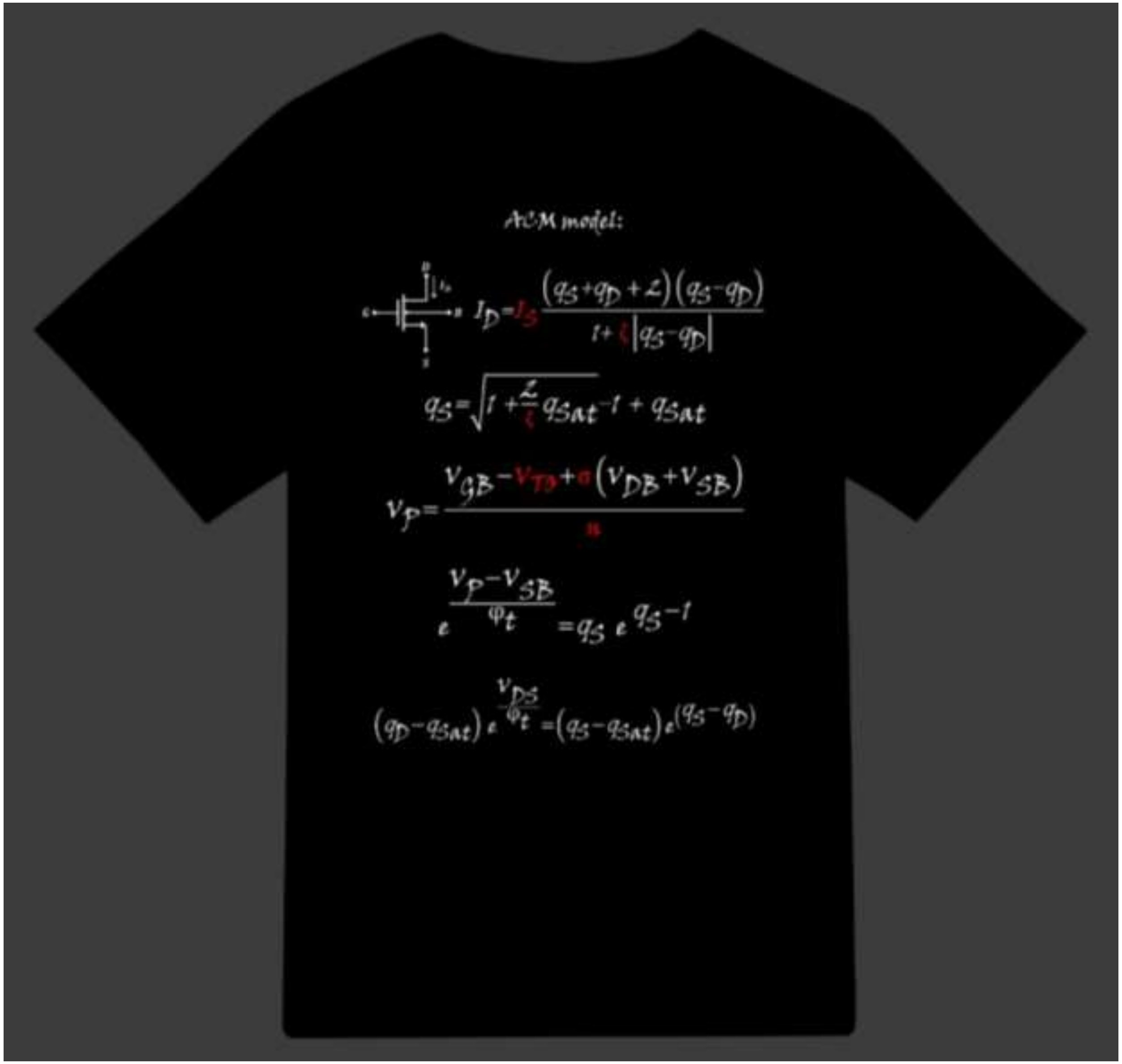
THE ADVANCED COMPACT MOSFET (ACM) MODEL AND ITS APPLICATION TO THE DESIGN AND SIMULATION OF BASIC CIRCUITS

Presentation by Márcio Cherem Schneider

Lima - September 2024

CONTENTS:

0. Introduction



0. Introduction

What is a compact model ?

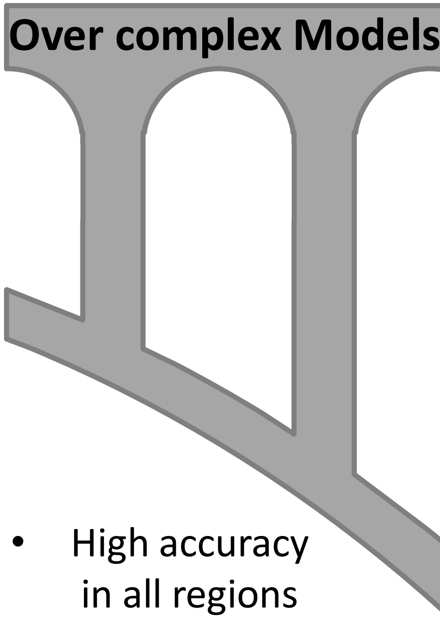
- Compact Model is the medium of information exchange between foundry and designer.
- Provides **detailed information** about device operation & characteristics
- However, needs to be:
  - **Simple** enough to be incorporated in circuit simulators
  - **Accurate** enough to predict behavior of circuits

0. Introduction

Why the need for a design-oriented MOSFET model ?

- Provides a proper bridge between the electrical behavior of the MOSFET and circuit performance though simple analytical equations
- Allows analytical sizing of the transistors
- Avoids excessive dependency of the IC designer in using parametric simulations with complex models to define the operation point!

- Poor accuracy, only in one region
- 2/3 DC parameters



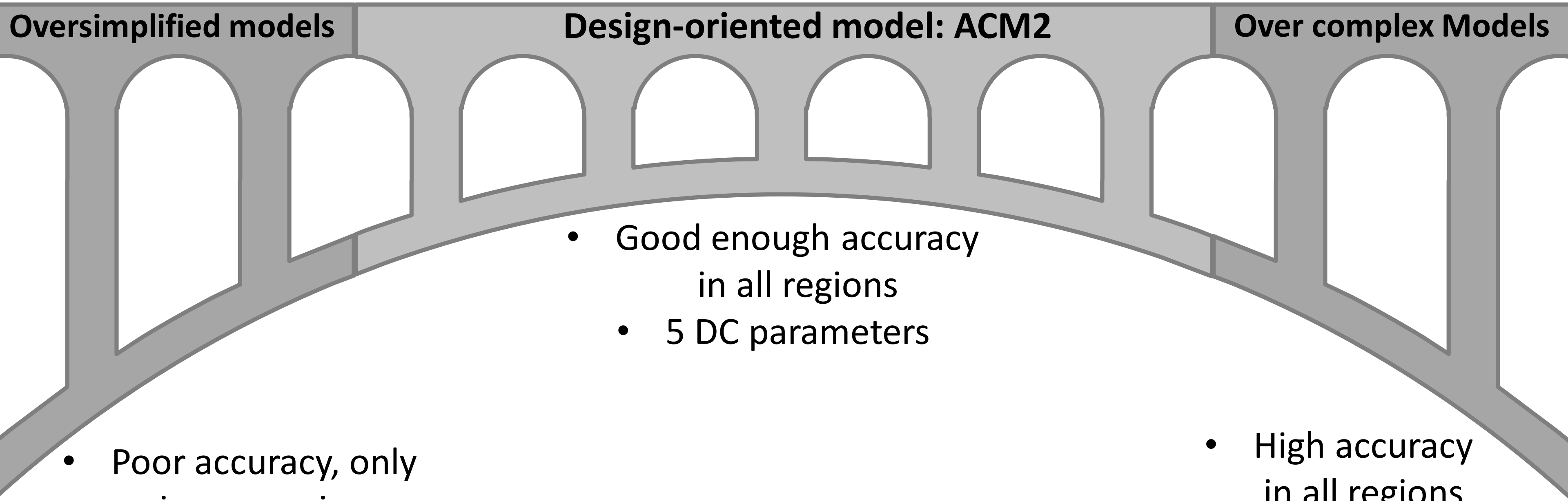
- High accuracy in all regions
- tens of DC parameters

0. Introduction

Why the need for a design-oriented MOSFET model ?

- Provides a proper bridge between the electrical behavior of the MOSFET and circuit performance though simple analytical equations
- Allows analytical sizing of the transistors
- Avoids excessive dependency of the IC designer in using parametric simulations
- **Increase the designer intuition!**

IC designers bridge



Oversimplified models

Design-oriented model: ACM2

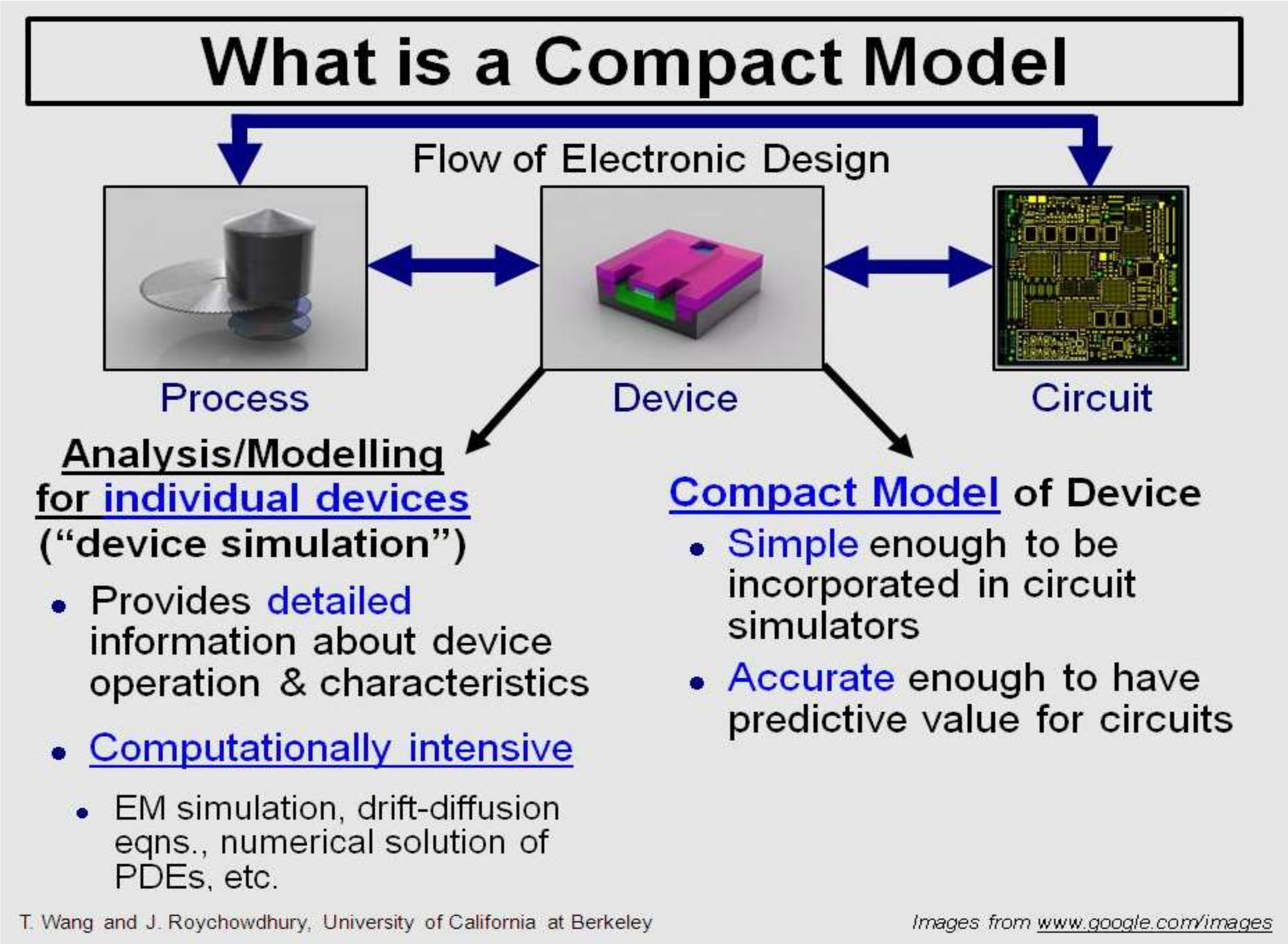
Over complex Models

- Good enough accuracy in all regions
- 5 DC parameters

- Poor accuracy, only in one region
- 2/3 DC parameters

- High accuracy in all regions
- tens of DC parameters

0. Introduction



What is a Compact Model

Flow of Electronic Design

Analysis/Modelling for individual devices (“device simulation”)

- Provides detailed information about device operation & characteristics
- Computationally intensive
  - EM simulation, drift-diffusion eqns., numerical solution of PDEs, etc.

Compact Model of Device

- Simple enough to be incorporated in circuit simulators
- Accurate enough to have predictive value for circuits

T. Wang and J. Roychowdhury, University of California at Berkeley

Images from www.google.com/images

0. Introduction

Family of BSIM models: popular MOSFET models for circuit simulators

BSIM DC models: equations characterized by several tens of parameters.

- Compact models with reduced number of DC parameters make easier the understanding of the MOSFET.
- Understanding of a compact DC model improves designers' skills and abbreviates considerably time spent on simulations.
- The simple 5-PM (5-parameter model) version of the ACM model: successfully simulation of MOS circuits.

This presentation: the 5-PM of the (DC) ACM model, the MOSFET small-signal model, noise and mismatch

0. Introduction

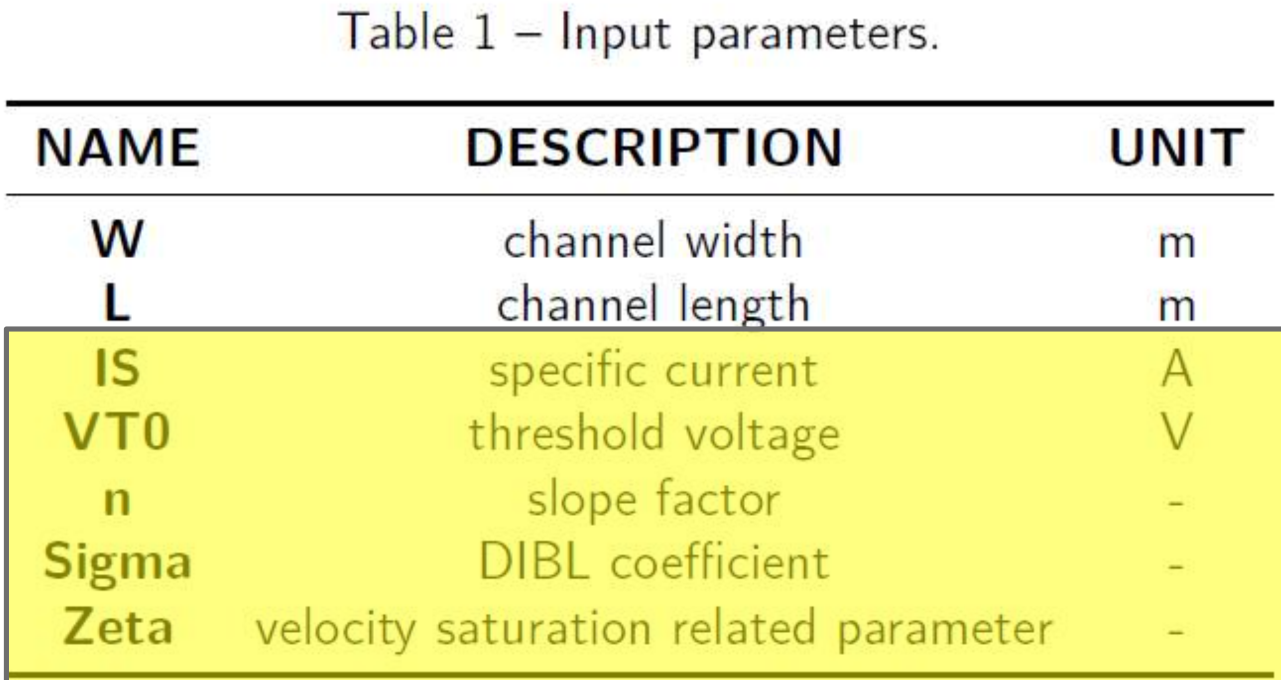
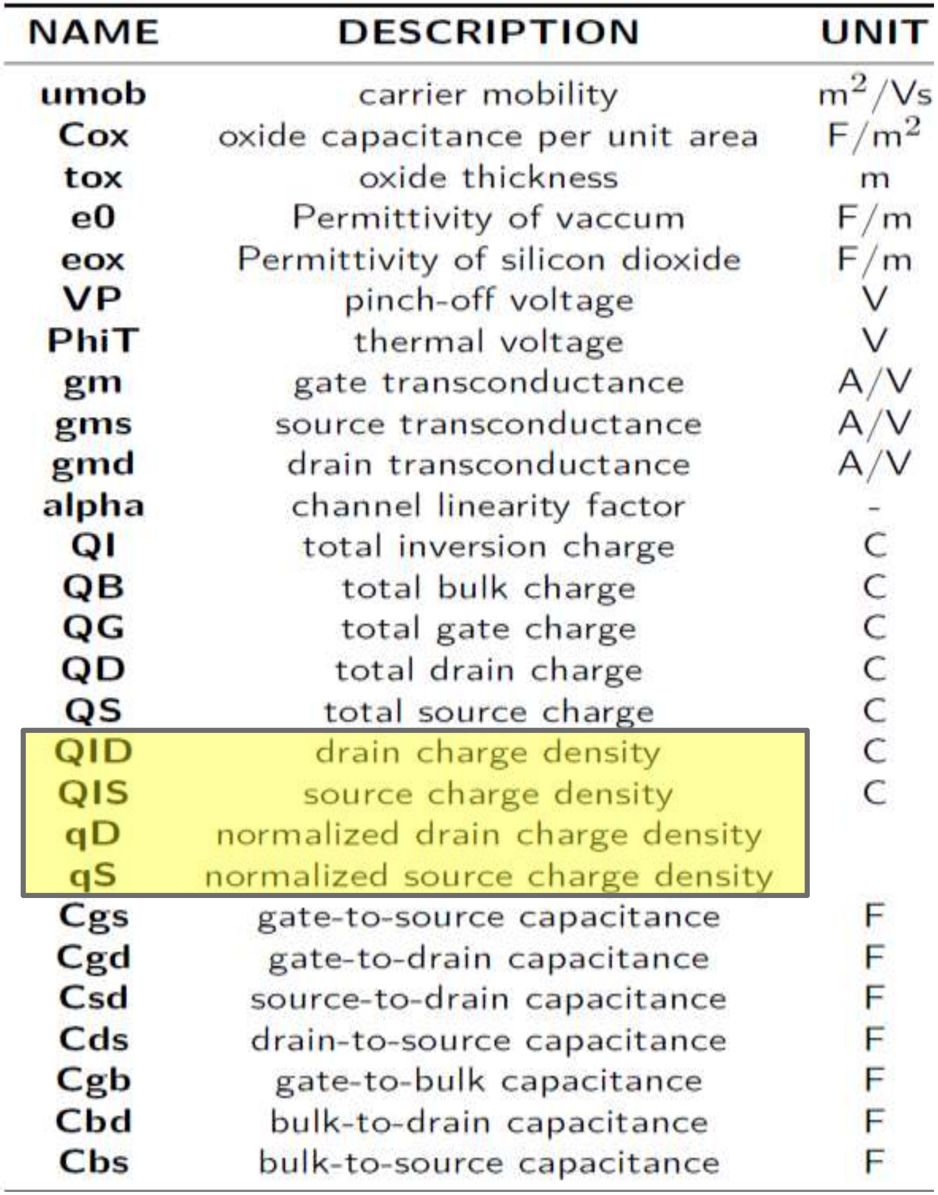


Table 1 – Input parameters.

NAME	DESCRIPTION	UNIT
W	channel width	m
L	channel length	m
IS	specific current	A
VT0	threshold voltage	V
n	slope factor	-
Sigma	DIBL coefficient	-
Zeta	velocity saturation related parameter	-

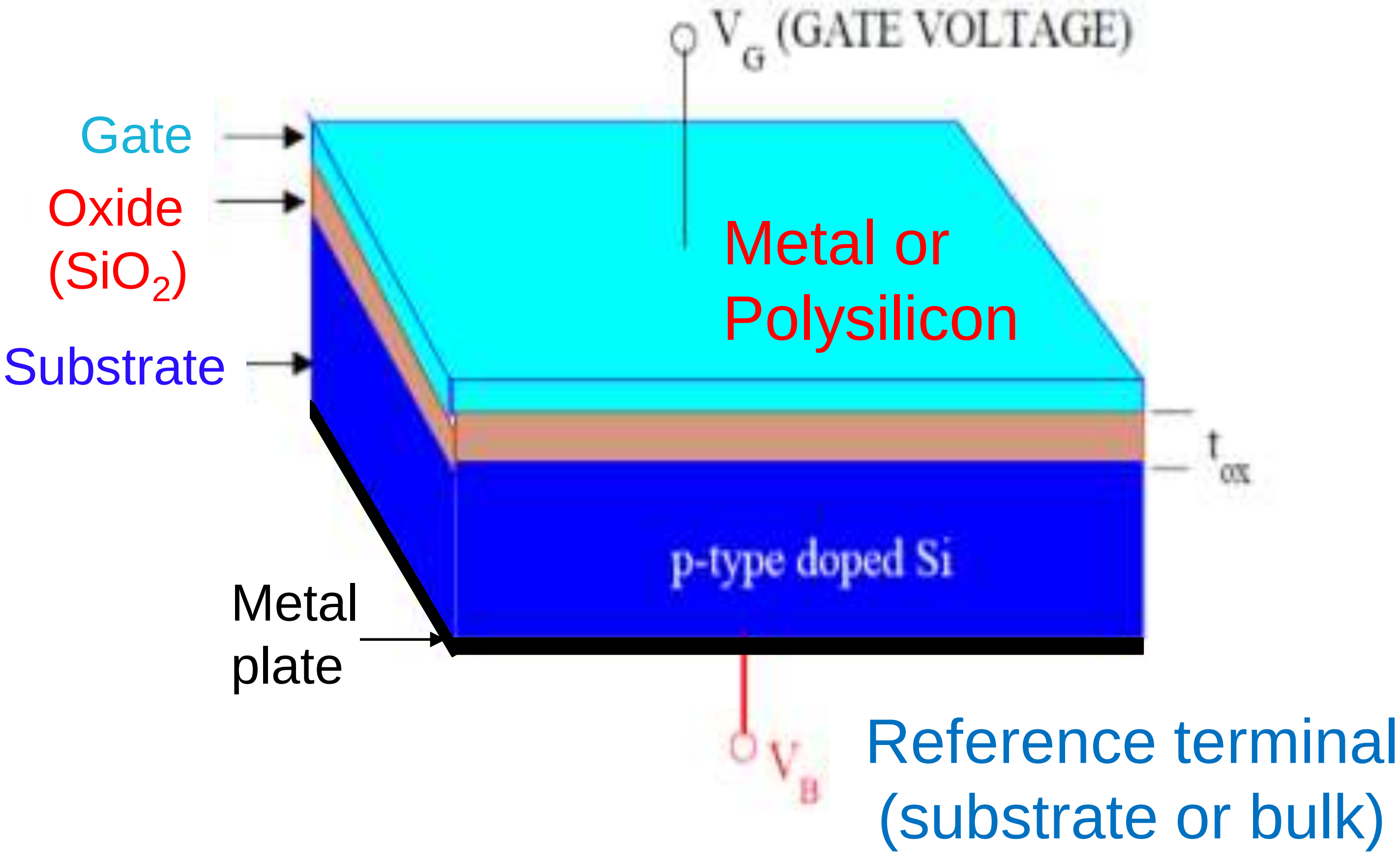
5 DC parameters of the ACM model

0. Introduction



NAME	DESCRIPTION	UNIT
umob	carrier mobility	m^2/Vs
Cox	oxide capacitance per unit area	F/m^2
tox	oxide thickness	m
e0	Permittivity of vaccum	F/m
eox	Permittivity of silicon dioxide	F/m
VP	pinch-off voltage	V
PhiT	thermal voltage	V
gm	gate transconductance	A/V
gms	source transconductance	A/V
gmd	drain transconductance	A/V
alpha	channel linearity factor	-
QI	total inversion charge	C
QB	total bulk charge	C
QG	total gate charge	C
QD	total drain charge	C
QS	total source charge	C
QID	drain charge density	C
QIS	source charge density	C
qD	normalized drain charge density	
qS	normalized source charge density	
Cgs	gate-to-source capacitance	F
Cgd	gate-to-drain capacitance	F
Csd	source-to-drain capacitance	F
Cds	drain-to-source capacitance	F
Cgb	gate-to-bulk capacitance	F
Cbd	bulk-to-drain capacitance	F
Cbs	bulk-to-source capacitance	F

1. The MOS capacitor



Gate

Oxide (SiO_2)

Substrate

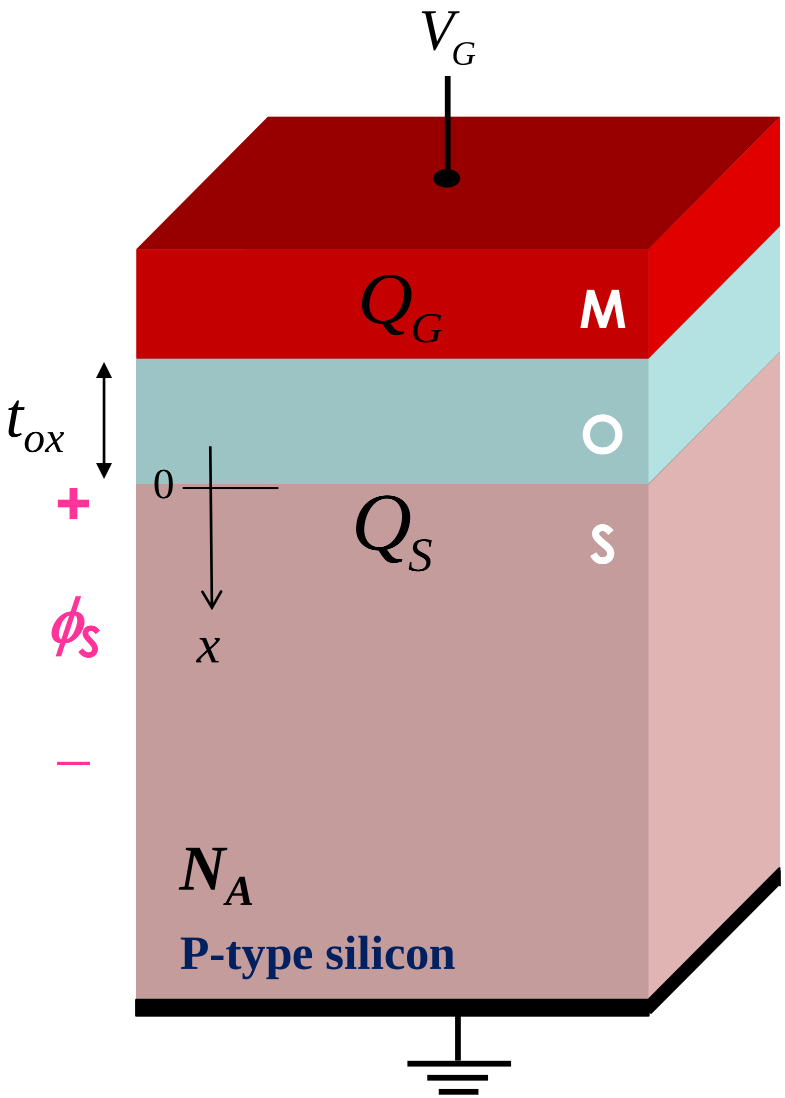
Metal or Polysilicon

Metal plate

Reference terminal (substrate or bulk)

https://www.wisdomjobs.com/userfiles/structure_of_mosfet.jpg

1. The MOS capacitor



The “ideal” two-terminal MOS structure

$$V_G - \phi_s = \frac{Q_G}{C_{ox}} \qquad C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

Charge conservation

$$\boxed{Q_G + Q_S = 0}$$

$$\underbrace{\boxed{V_G = \phi_s - \frac{Q_S}{C_{ox}}}}$$

Potential balance equation

t_{ox} **-** oxide thickness

ε_{ox} **-** permittivity of oxide

ϕ_S - surface potential (at x=0)

C_{ox} - oxide capacitance/unit area

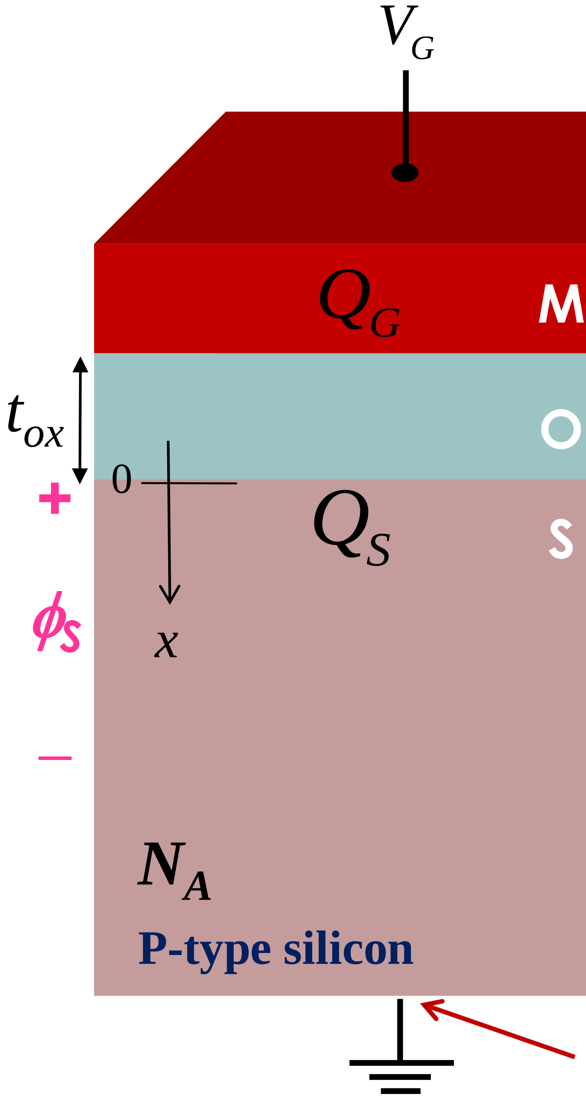
Q_G (Q_S) - gate (semiconductor) charge/ unit area

N_A – acceptor concentration

What´s the electric field E_{ox} inside the oxide?

1. The MOS capacitor

The MOS capacitor



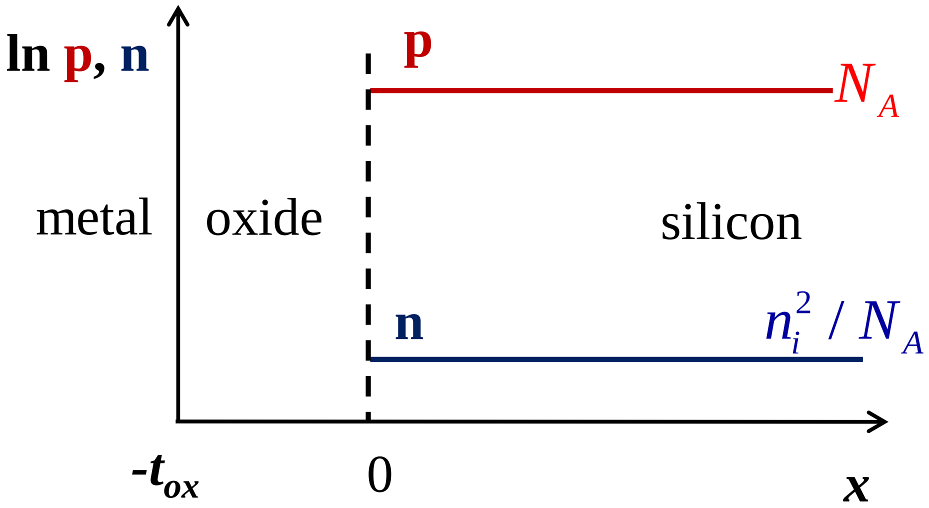
Reference potential (gnd)

The potential balance equation

$$\boxed{V_G - V_{FB} = \phi_s - \frac{Q_S}{C_{ox}}}$$

Flat band

$$V_G = V_{FB}$$



Carrier concentration along ***x*** for $\phi_S = Q_S = 0$

$$\begin{cases} p = N_A \\ n = n_i^2 / N_A \end{cases}$$

Example 1.1 : oxide capacitance

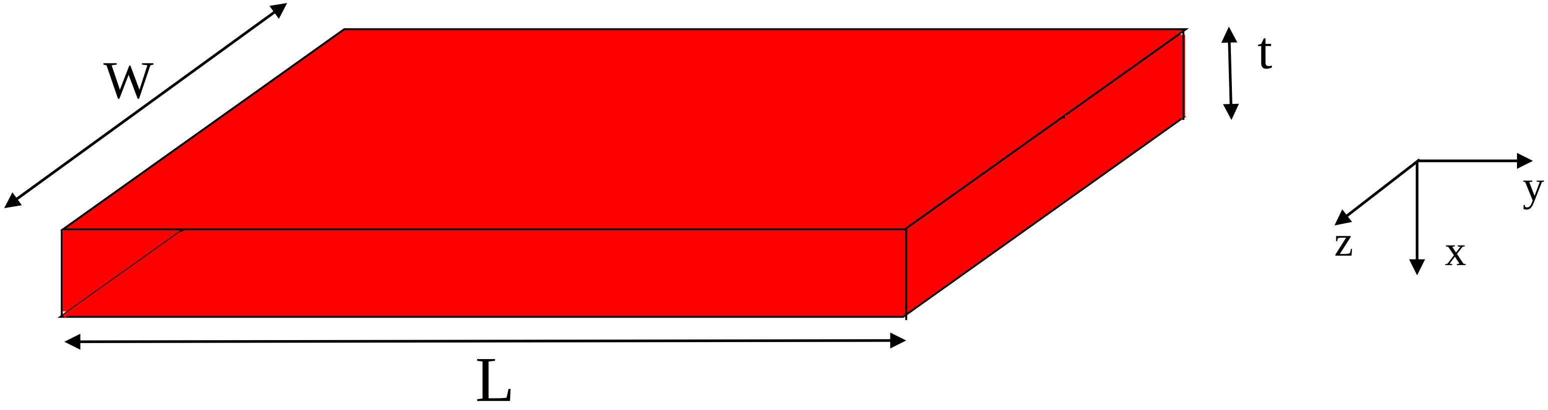
(a) Calculate the oxide capacitance per unit area for t_{ox}= 5 and 20 nm. The permittivity of silicon oxide is $\varepsilon_{ox} = 3.9\varepsilon_0$. $\varepsilon_0 = 8.85 \cdot 10^{-14}$ F/cm is the permittivity of free space.

(b) Determine the area of a 1pF metal-oxide-metal capacitor for the two oxide thicknesses given in (a).

(c) Determine the gate charge/unit area in C/cm^2 and the number of elementary charges/ μm^2 of the 1 pF capacitor for $V_G - \phi_S = 1$ V

Answer: (a) C_{ox} = 690 nF/cm^2 = 6.9 fF/μm^2 for t_{ox}=5 nm and C_{ox} = 172 nF/cm^2= 1.7 fF/μm^2 for t_{ox}= 20 nm. (b)The capacitor areas are 145 and 580 μm^2 for oxide thicknesses of 5 and 20 nm, respectively. (c) $0.69 \cdot 10^{-6}$ C/cm^2 and $0.43 \cdot 10^5$/ μm^2 for capacitor area of 145 μm^2 and $0.17 \cdot 10^{-6}$ C/cm^2 and $0.11 \cdot 10^5$ /μm^2 for capacitor area of 580 μm^2.

Example 1.2: volumetric and areal charge densities



Assume that the electron concentration is n = 10^{16} cm^{-3} , L=W=1 um, t=0.1 um

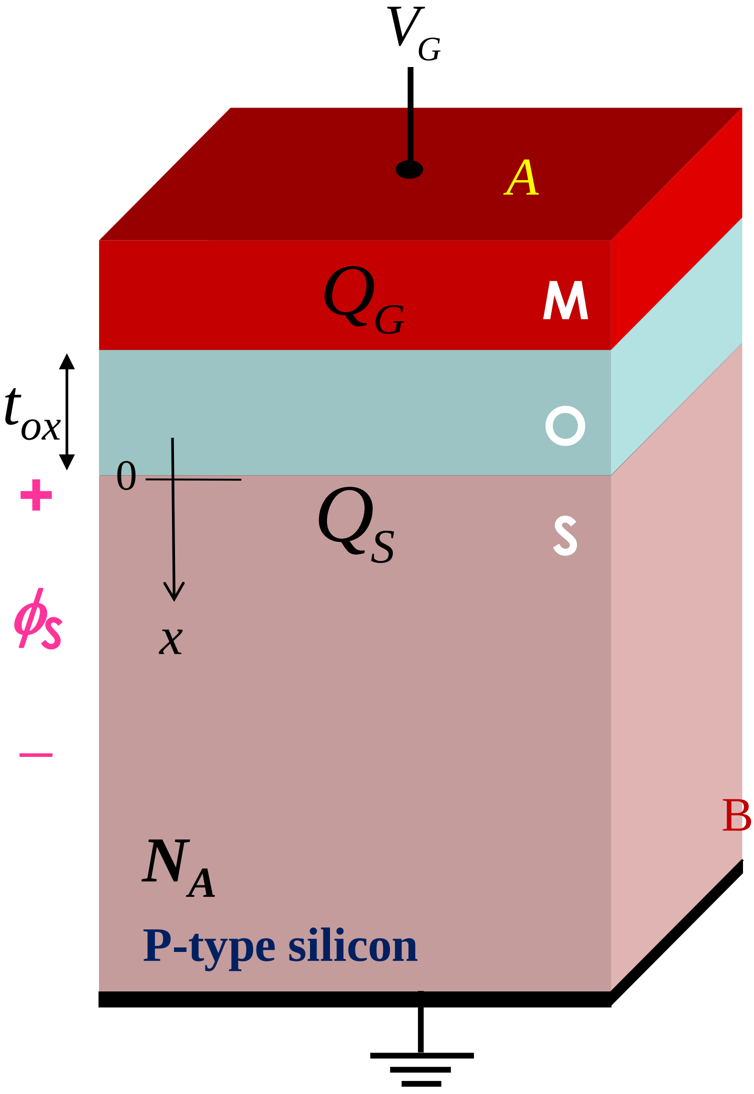
(a) Calculate the volumetric charge density

(b) Calculate the total number of electrons and the corresponding charge inside the volume

(c) Calculate the (areal) charge density seen from the x-direction (seen from above)

Answer: (a) ρ= -1.6 10^{-3} C/cm^3 (b) Number of electrons = 10^3, charge = -1.6 x 10^{-16} C (c) charge density Q_n= -1.6 x 10^{-8} C/cm^2 .

1. The MOS capacitor



What is the semiconductor Q_S composed of?

$$\rho = q(\underbrace{p - n}_{\text{Mobile charges}} + \underbrace{\cancel{N_D} - N_A}_{\text{Fixed charges}})$$

The semiconductor charge density Q_S is

$$Q_S = \int_0^{ohmic\ contact} \rho dx = \int_0^{ohmic\ contact} q(p - N_A - n)dx$$

$$Q_S = Q_B + Q_I$$

Bulk(fixed) charge

Inversion (mobile) charge

$$\boldsymbol{Q_B = \int_0^{ohmic\ contact} q(p - N_A)dx}$$

$$\boldsymbol{Q_I = -\int_0^{ohmic\ contact} qndx}$$

Reference potential (gnd)
Ohmic contact

$$\left\{ \begin{array}{l} \boldsymbol{p = N_A} \\ \boldsymbol{n = n_i^2 / N_A} \end{array} \right.$$

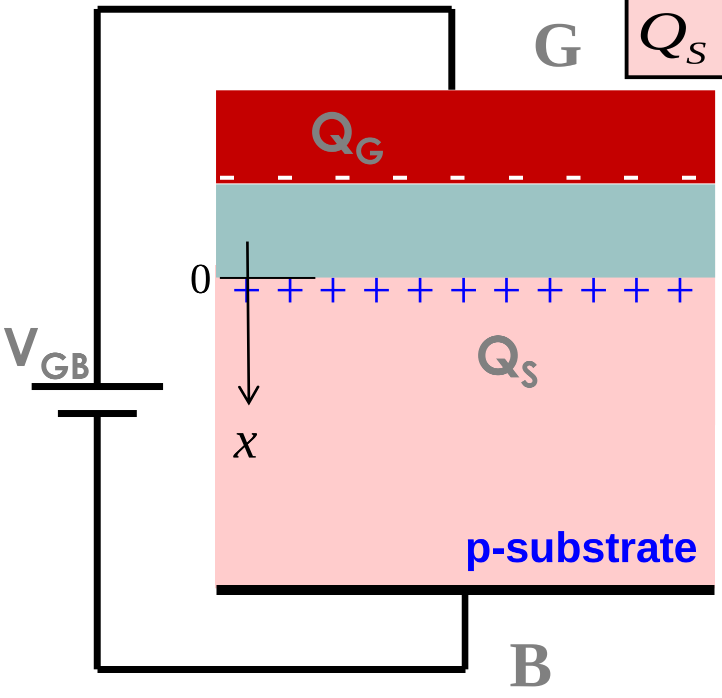
1. The MOS capacitor

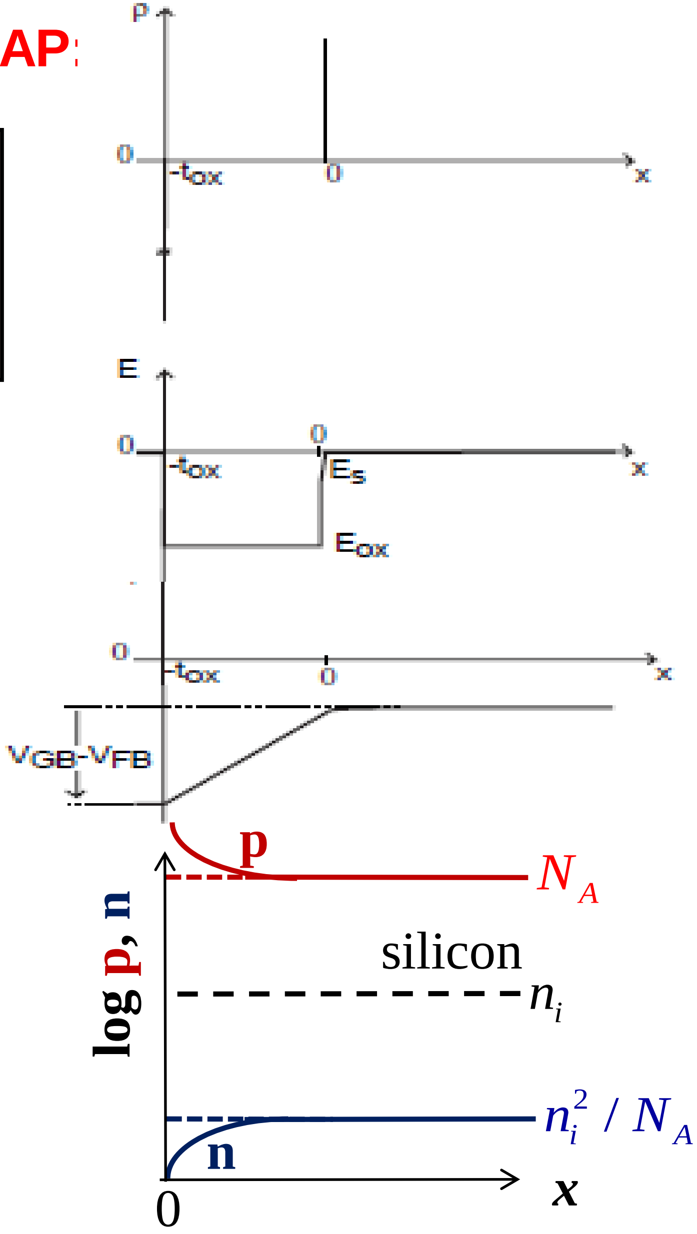
Regions of operation of the MOSCAP:

Accumulation

(p-substrate)

$$V_{GB} < V_{FB}$$
$$\phi_s < 0$$
$$Q_S > 0$$





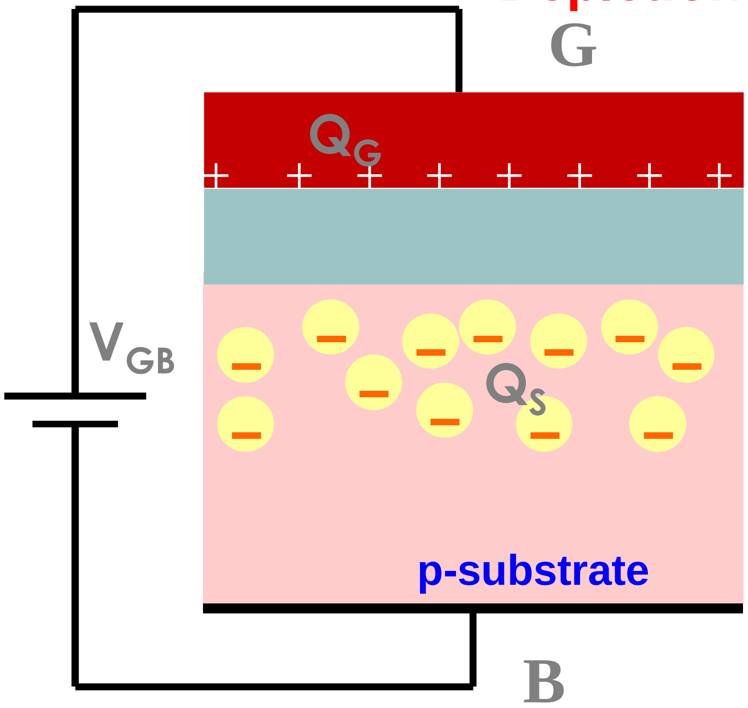
$$p = N_A e^{-\frac{q\phi(x)}{kT}}$$

$$n = \frac{n_i^2}{N_A} e^{\frac{q\phi(x)}{kT}}$$

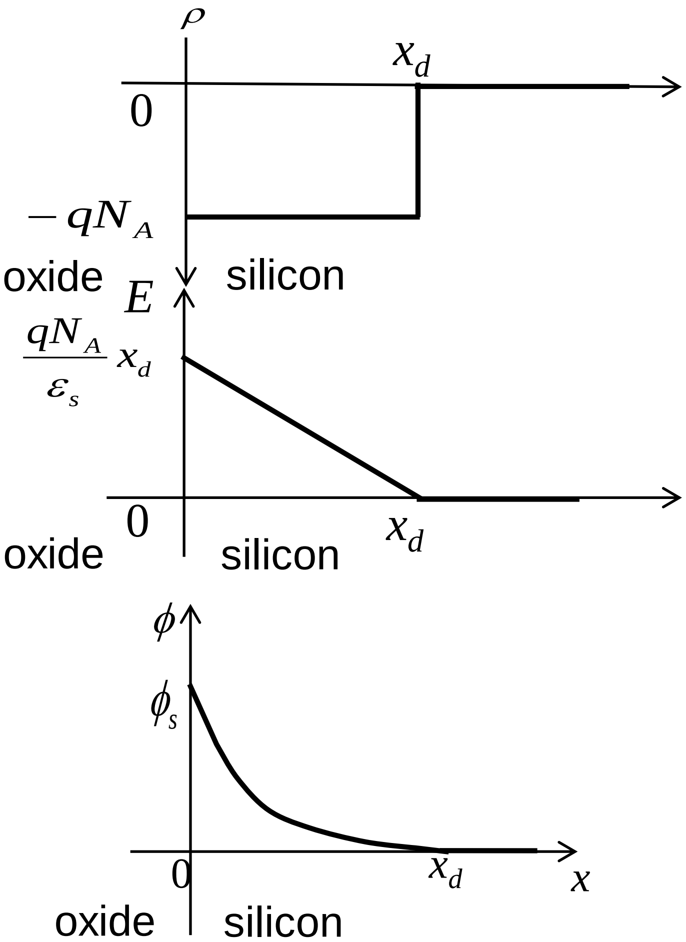
Holes + accumulate in the p-type semiconductor surface

1. The MOS capacitor

Depletion (p-substrate)



$V_{GB} > V_{FB}$
$\phi_F > \phi_s > 0$
$Q_S < 0$

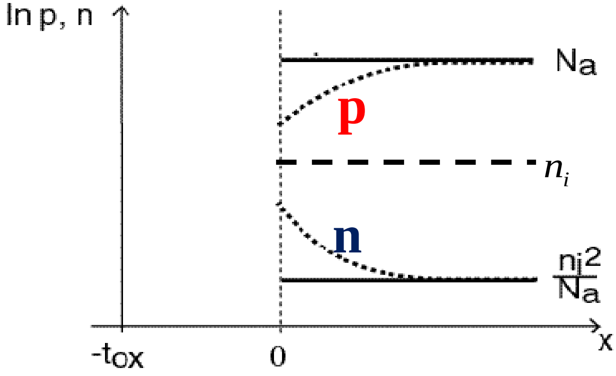


Holes evacuate from the P semiconductor surface and acceptor ion charges ⊖ become uncovered

$\boxed{Q_S \cong Q_D}$

Q_D: depletion charge (ions)

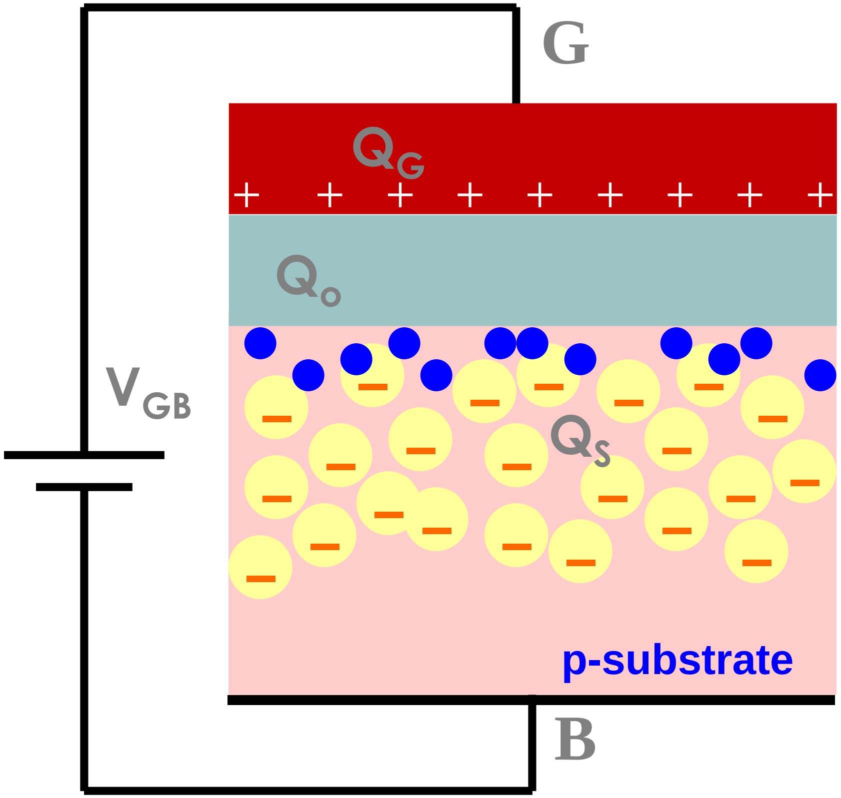
$$n = \frac{n_i^2}{N_a} e^{\frac{q\phi(x)}{kT}} \qquad p = N_a e^{-\frac{q\phi(x)}{kT}}$$



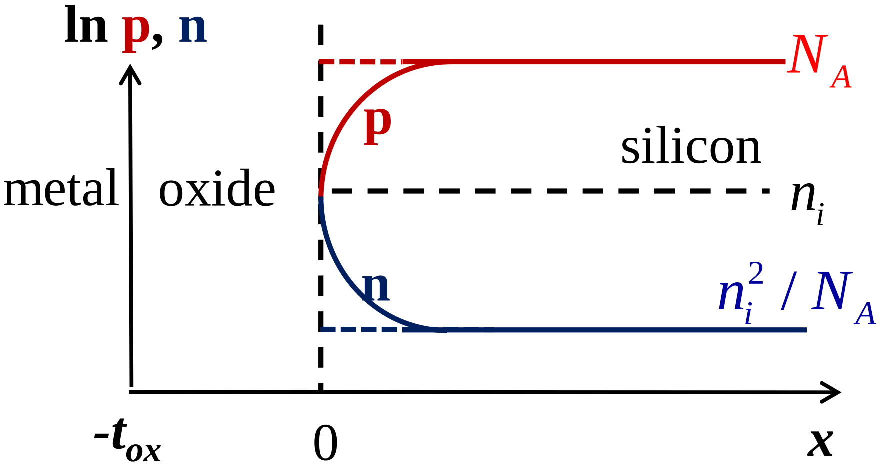
Regions of operation of the MOSCAP: Inversion (p-substrate)

$$\boxed{\begin{array}{l}\phi_s > \phi_F \\ Q_S < 0\end{array}}$$

ϕ_F : Fermi potential



Many electrons ● approach the surface!

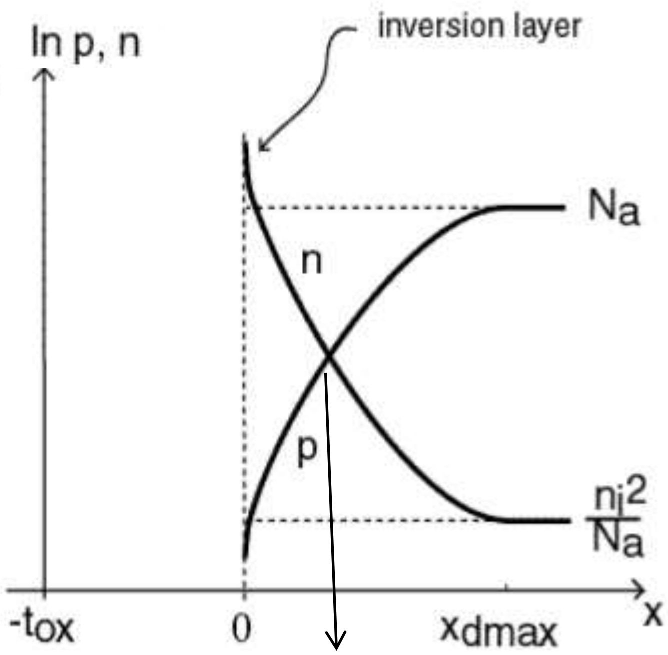


$$\boxed{Q_S = Q_N + Q_D}$$

When $\boxed{\phi_s = \phi_F \rightarrow p(x=0) = n(x=0) = n_i}$

Q_N: electron charge (carriers)

Regions of operation of the MOSCAP - Inversion (p-substrate): $\phi_s > \phi_F$ **Φ_F is the Fermi potential**



$$p = N_a e^{-\frac{q\phi(x)}{kT}}$$

$$n = \frac{n_i^2}{N_a} e^{\frac{q\phi(x)}{kT}}$$

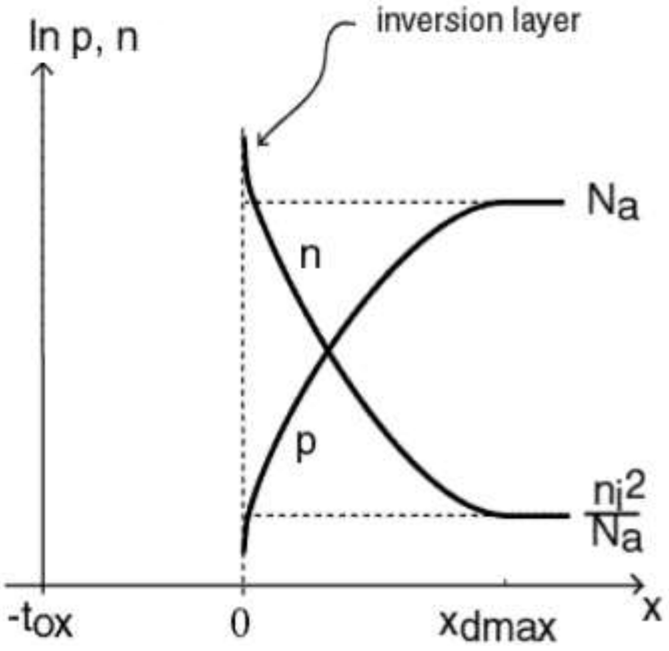
$$n(\phi = \phi_F) = n_i = \frac{n_i^2}{N_a} e^{\frac{q\phi_F}{kT}} \rightarrow \phi_F = \frac{kT}{q} \ln \frac{N_a}{n_i}$$

The semiconductor operates in inversion when $\phi_S > \phi_F$

At this point
$p=n=n_i$ and $\phi=\phi_F$

For $\phi>\phi_F$ the concentration of minority carriers (*n*) at the semiconductor-oxide interface becomes higher than that of majority carriers (*p*); the semiconductor operates in the inversion region

Strong inversion : the concentration of minority carriers (*n*) becomes higher than that of holes (majority carriers) deep in the bulk



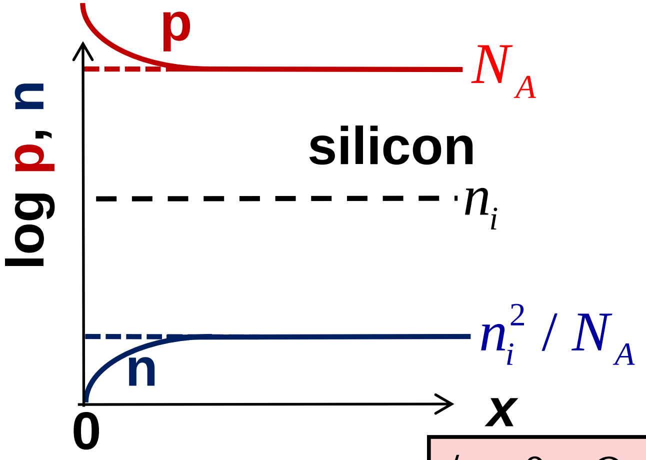
$$p = N_a e^{-\frac{q\phi(x)}{kT}}$$

$$n = \frac{n_i^2}{N_a} e^{\frac{q\phi(x)}{kT}}$$

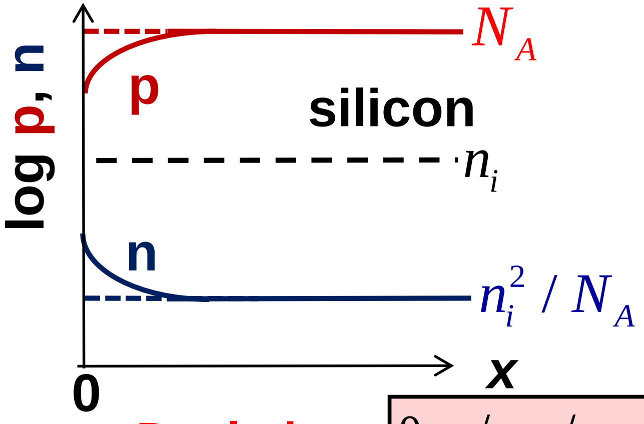
$$n = N_a = \frac{n_i^2}{N_a} e^{\frac{q\phi}{kT}} \rightarrow \phi = 2\frac{kT}{q}\ln\frac{N_a}{n_i} = 2\phi_F$$

The semiconductor operates in strong inversion when $\phi_S > 2\phi_F$

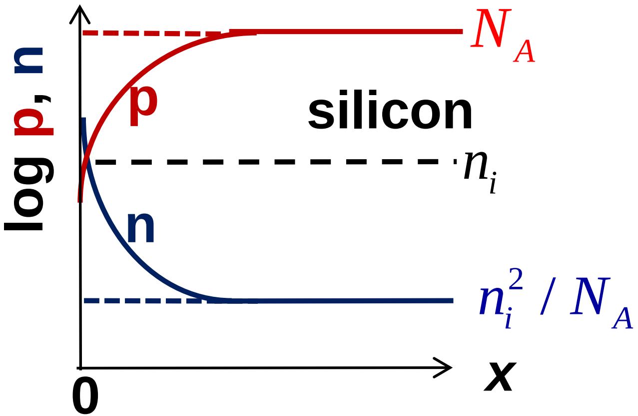
Operating regions of the MOSCAP: Summary (I)



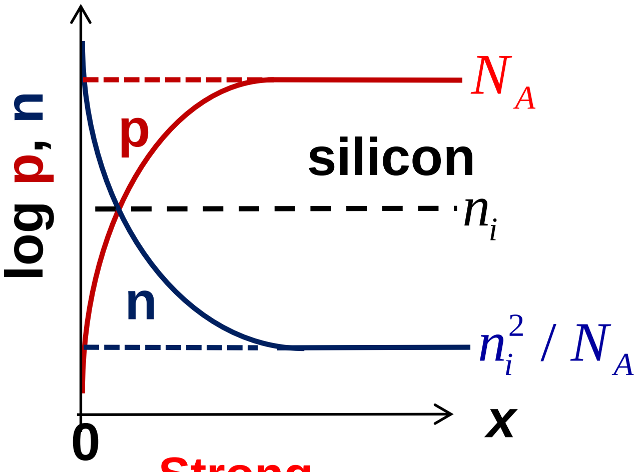
Accumulation $\phi_s < 0; \quad Q_S > 0$



Depletion $0 < \phi_s < \phi_F; \quad Q_S < 0$

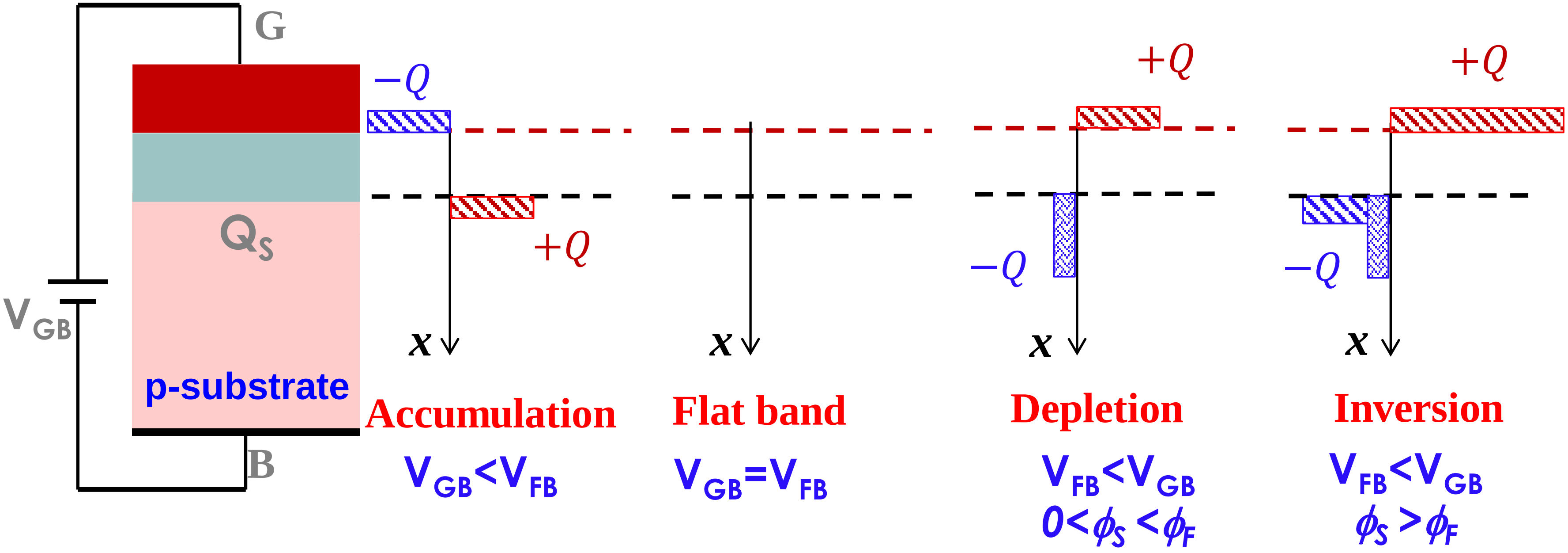


Weak inversion $\phi_F < \phi_s < 2\phi_F; \quad Q_S < 0$



Strong inversion $2\phi_F < \phi_s; \quad Q_S < 0$

Operating regions of the MOSCAP: Summary (II)



Accumulation

$V_{GB}<V_{FB}$

Flat band

$V_{GB}=V_{FB}$

Depletion

$V_{FB}<V_{GB}$
$0<\phi_S<\phi_F$

Inversion

$V_{FB}<V_{GB}$
$\phi_S>\phi_F$

▨ **Positive charge (holes or deficiency of electrons) density**

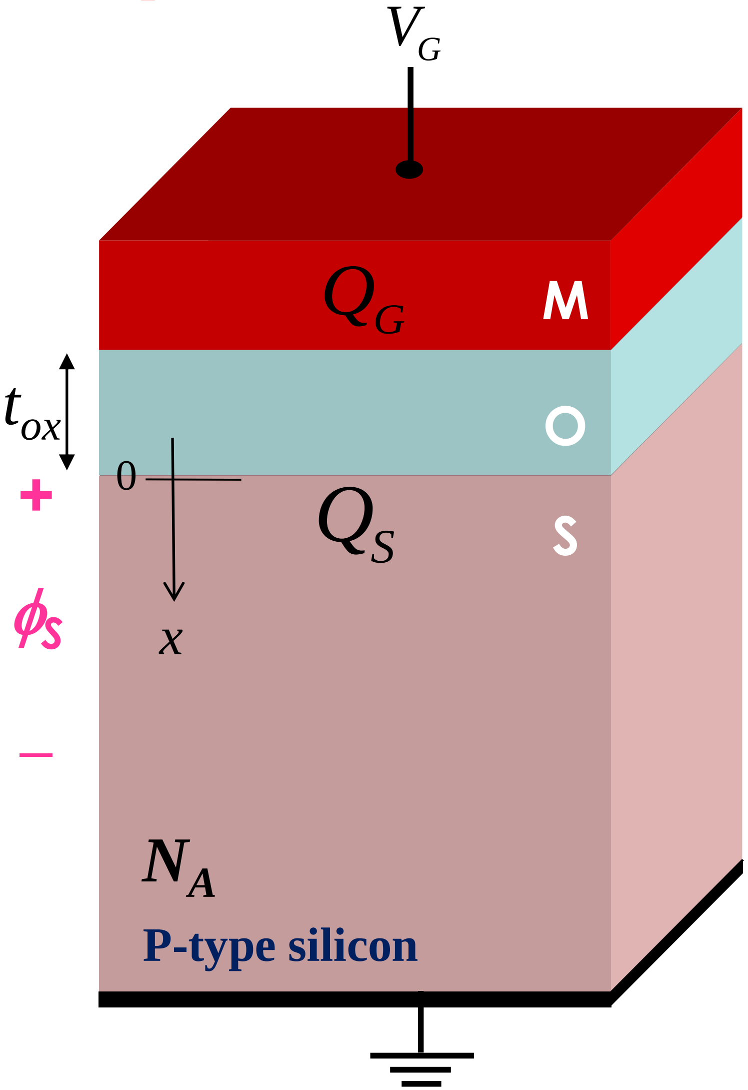
▨ **Carrier (electron) charge density**

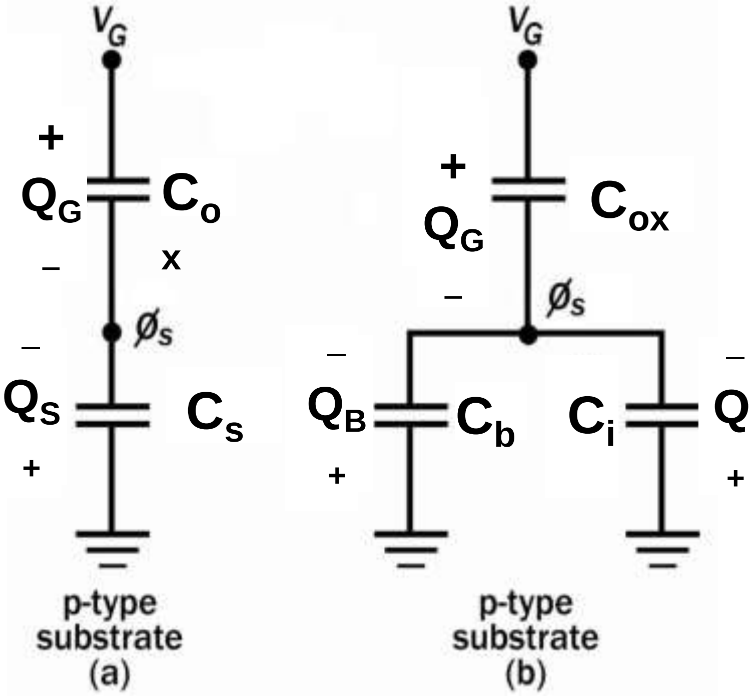
▨ **Depletion (ion) charge density**

1. The MOS capacitor

Capacitive model of the MOSCAP

$$\boxed{V_G - V_{FB} = \phi_s - \frac{Q_S}{C_{ox}}}$$





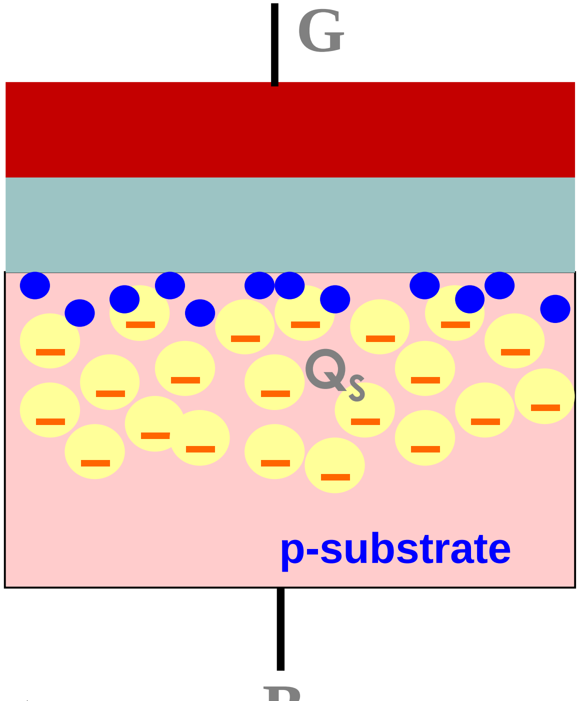
$$Q_B = \int_0^{\substack{ohmic\\contact}} q(\underset{\downarrow}{p - N_A})dx$$

Holes & uncovered ions

$$Q_I = -\int_0^{\substack{ohmic\\contact}} qndx$$

Electrons (N-MOSFET carriers)

The threshold voltage



Q_S (semiconductor charge density) =

Q_I (carrier charge density)+

Q_B (ion charge density)

mobile

fixed

Threshold voltage

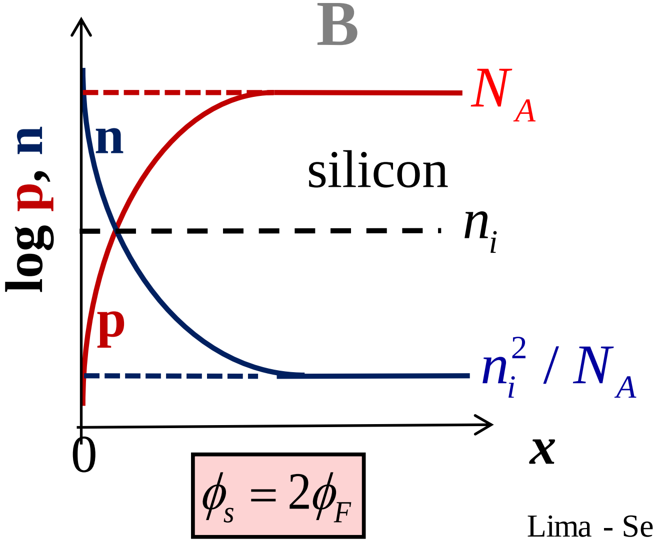
Gate voltage for which
$n(x=0) = N_A \Rightarrow \phi_s = 2\phi_F$

$$\phi_F = \phi_t \ln(\frac{N_A}{n_i})$$

From $$\boxed{V_G - V_{FB} = \phi_s - \frac{Q_S}{C_{ox}}}$$

$$\boxed{V_T = V_{GB}\Big|_{\phi_s = 2\phi_F} \cong V_{FB} + 2\phi_F + \underbrace{\gamma\sqrt{2\phi_F}}_{\text{Term due to } Q_D}}$$

$$\gamma = \sqrt{2q\varepsilon_s N_A} / C_{ox}$$



Example 1.3: threshold voltage

Estimate V_T for an n-channel transistor with N_A=10^{17} atoms/cm^3 and t_{ox}=5 nm. The flat-band voltage is -0.58 V.

$$\phi_F = \phi_t \ln\frac{N_A}{n_i} \cong 26\times\ln\frac{10^{17}}{10^{10}} = 419 \text{ mV};\;\; C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{0.345\times10^{-12}}{5\times10^{-7}} = 690\times10^{-9} \text{ F/cm}^2$$

The body-effect factor is

$$\gamma = \sqrt{2q\varepsilon_s N_A} / C_{ox} = \frac{\sqrt{2\times1.6\times10^{-19}\times1.04\times10^{-12}\times10^{17}}}{690\times10^{-9}} = 0.264\sqrt{\text{V}}$$

The threshold voltage is

$$V_T \cong V_{FB} + 2\phi_F + \gamma\sqrt{2\phi_F} = -0.58 + 0.838 + 0.264\sqrt{0.838} = 0.5\text{V}$$

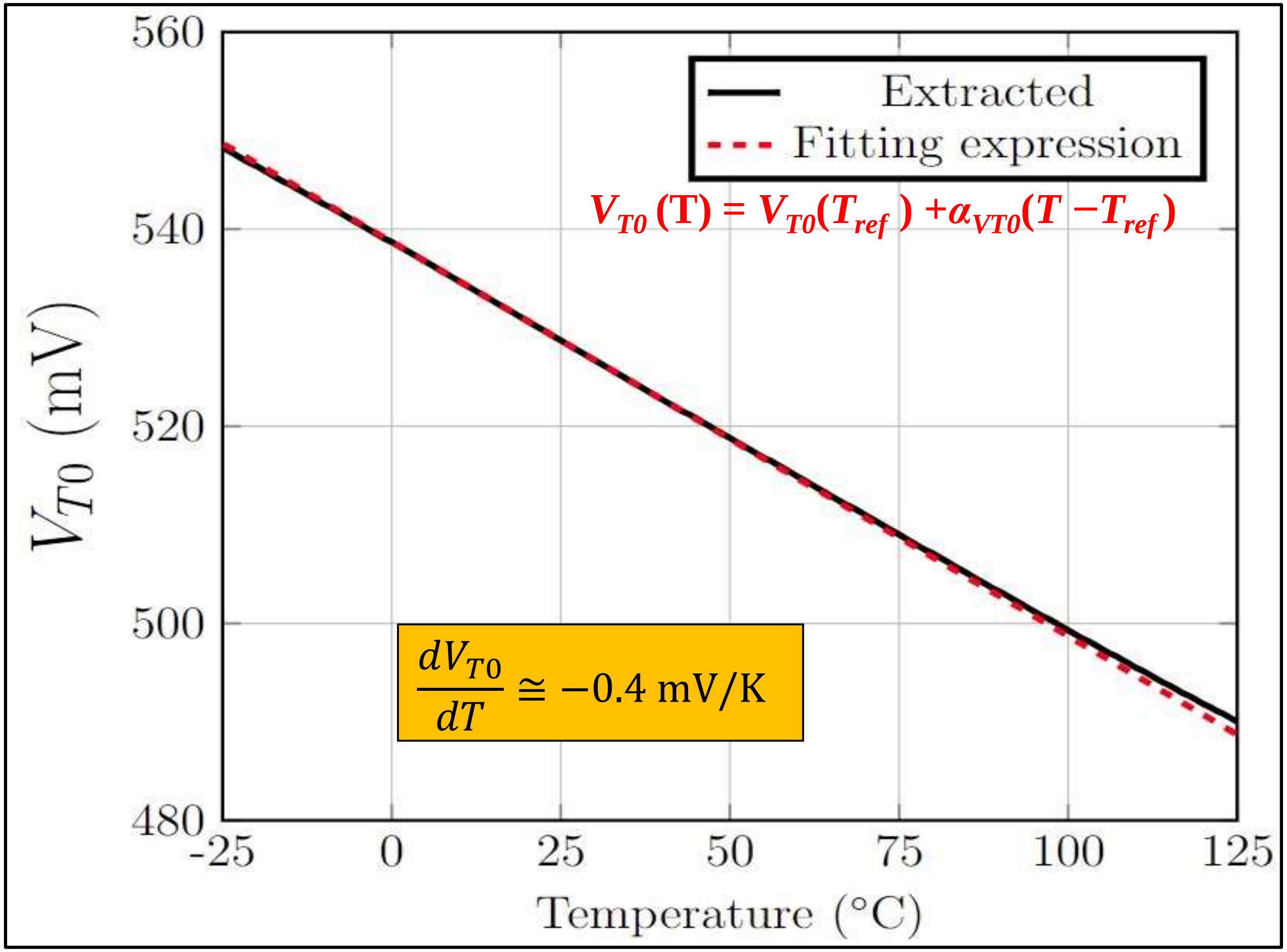
NOTE: In some technologies there are transistors with V_T close to zero, which are called native or zero-VT transistors

1. The MOS capacitor

$$V_T = V_{GB}\Big|_{\phi_s=2\phi_F} \cong V_{FB} + 2\phi_F + \gamma\sqrt{2\phi_F}$$

$$\frac{dV_{T0}}{dT} \cong -\frac{n}{T}\left(\frac{V_{gap}}{2} - \emptyset_F\right)$$

Standard VT
180 nm CMOS
W= 5 um
L= 180 nm



$$V_{T0}\,(\mathrm{T}) = V_{T0}(T_{ref}) + \alpha_{VT0}(T - T_{ref})$$

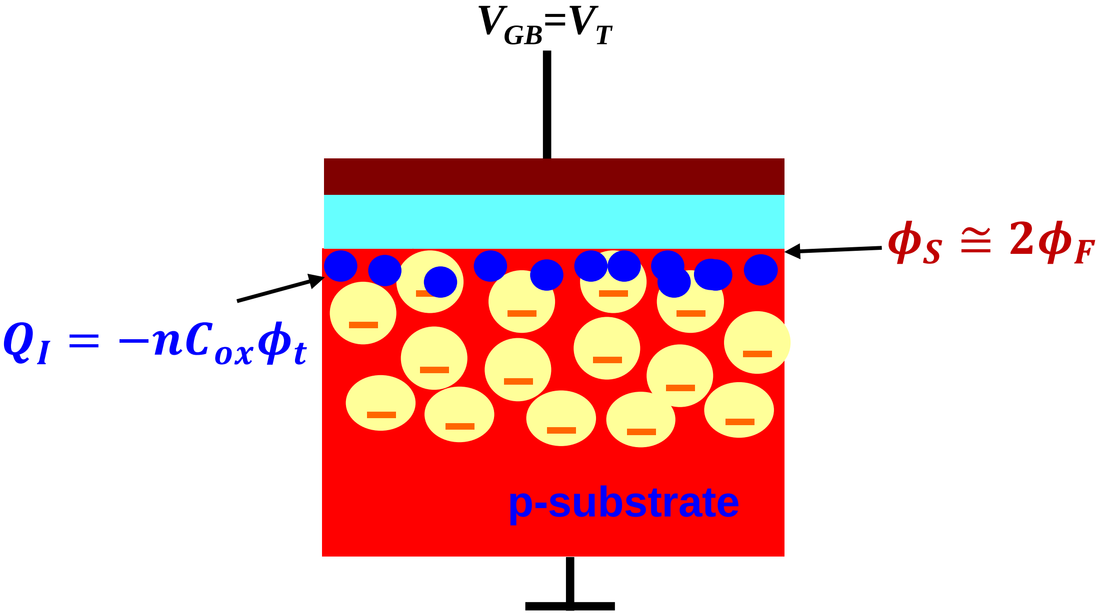
$$\frac{dV_{T0}}{dT} \cong -0.4\ \mathrm{mV/K}$$

Temperature dependence of the threshold voltage (~ CTAT)

1. The MOS capacitor

Since ACM is charge-based model, the threshold voltage is modified to

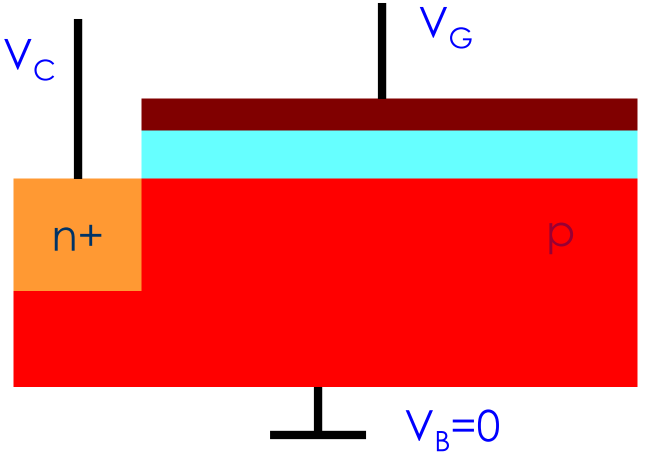
$$V_T = V_{GB}|_{Q_I=Q_{IP}=-nC_{ox}\phi_t} \cong V_{GB}|_{\phi_S=2\phi_F} = V_{FB} + 2\phi_F + \gamma\sqrt{2\phi_F}$$



Example 1.3

$n = 1 + \frac{\gamma}{2\sqrt{2\phi_F}} = 1.144$, $C_{ox} = 690\ nF/\text{cm}^2$, ϕ_t= 25.9 mV ⇨ Q_I = -20.4 pC/cm^2

2. The three-terminal MOS structure



Carrier concentrations in Si substrate follow Boltzmann's law:

n, p ∝ exp(-Energy/kT)

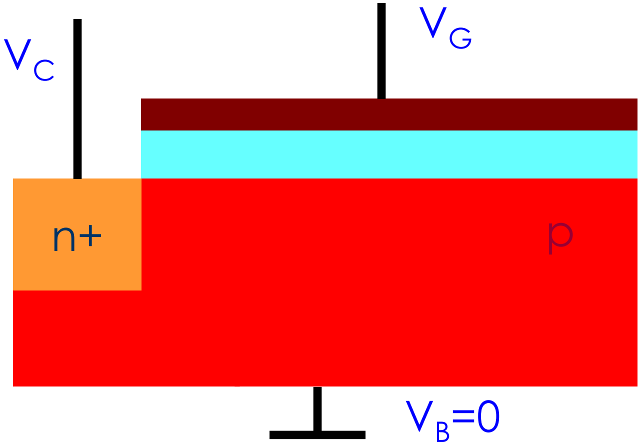
The origin of potential ϕ is taken deep in the bulk

$$p = p_0 e^{-\frac{q\varphi}{kT}}; \quad n = n_0 e^{\frac{q(\varphi - V_C)}{kT}}$$

Electrons are no longer in equilibrium with holes due to the bias of the source-bulk junction V_C

$$\boxed{pn = n_i^2 e^{-V_C/\varphi_t}}$$

2. The three-terminal MOS structure



$$C_{ox} + C_b = nC_{ox}$$

$$n = n(V_G)$$

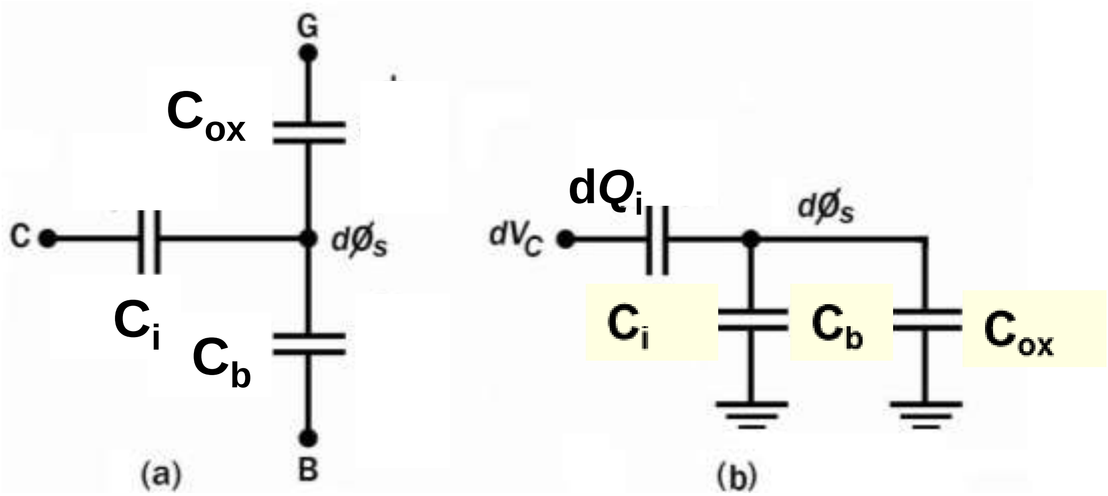
$$dQ_I = nC_{ox} d\phi_s$$

$$\frac{d\phi_s}{dV_C} = \frac{C_i}{C_i + C_{ox} + C_b} \begin{cases} \sim -\dfrac{Q_I}{nC_{ox}\phi_t} < 1 & \text{WI} \\ \sim 1 & \text{SI} \end{cases}$$

$$C_i = -\frac{Q_I}{\phi_t}$$

$$\Downarrow$$

$$\boxed{dV_C = dQ_I \left(\frac{1}{nC_{ox}} - \frac{\phi_t}{Q_I} \right)}$$



$$V_S \le V_C \le V_D$$

2. The three-terminal MOS structure

Unified Charge Control Model (UCCM)

$$dQ_I\left(\frac{1}{nC_{ox}}-\frac{\phi_t}{Q_I}\right)=dV_C$$

$$n=1+\frac{C_b}{C_{ox}}=n\left(V_G\right)$$

$$Q_{IP}=Q_I\big|_{V_C=V_P}$$

Integrating from an arbitrary channel potential V_C to a reference potential V_P (pinch-off) yields UCCM

$$\boxed{V_P-V_C=\phi_t\left[\frac{Q_{IP}-Q_I}{nC_{ox}\phi_t}+\ln\left(\frac{Q_I}{Q_{IP}}\right)\right]}$$

Choosing the thermal charge as the pinch-off charge

$$Q_{IP}=-nC_{ox}\phi_t \xrightarrow{**} V_P\cong\frac{V_{GB}-V_T}{n}$$

The normalized inversion (areal) charge density is

$$\frac{Q_I}{Q_{IP}}=q_I$$

Normalized UCCM

$$\boxed{\frac{V_P-V_C}{\phi_t}=q_I-1+\ln q_I}$$

** This is an approximate value of V_P, which is very useful for first order calculations

2. The three-terminal MOS structure

Unified Charge Control Model (UCCM)

The “regional” strong and weak inversion approximations

$$V_P - V_C = \phi_t\left[\frac{Q_{IP}-Q_I}{nC_{ox}\phi_t} + \ln\left(\frac{Q_I}{Q_{IP}}\right)\right]$$

$$V_P \cong \frac{V_G - V_T}{n}$$

$|Q_I| \gg Q_{IP}$

strong inversion

$$-Q_I \cong nC_{ox}\left(\frac{V_G - V_T}{n} - V_C\right)$$

$|Q_I| \ll Q_{IP}$

weak inversion

$$\frac{V_{GB} - V_T}{n} - V_C \cong \phi_t\left[\ln\left(\frac{Q_I}{Q_{IP}}\right) - 1\right]$$

or, equivalently

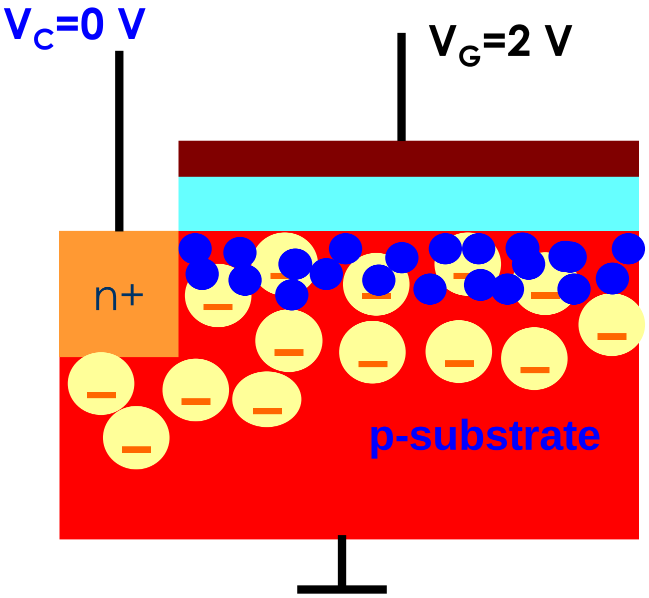
$$Q_I = Q_{IP}e^{\frac{\frac{V_G-V_T}{n}-V_C+\phi_t}{\phi_t}}$$

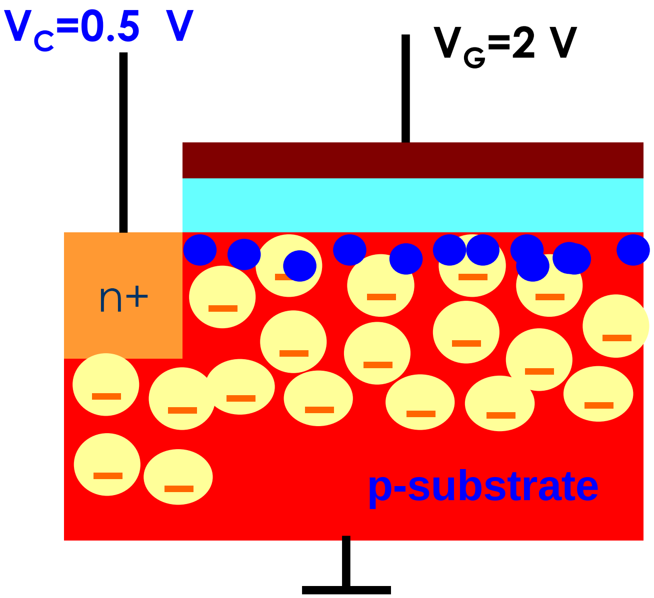
Note: expressions above can be referred to bulk potential ≠ 0

$V_G \rightarrow V_{GB}$

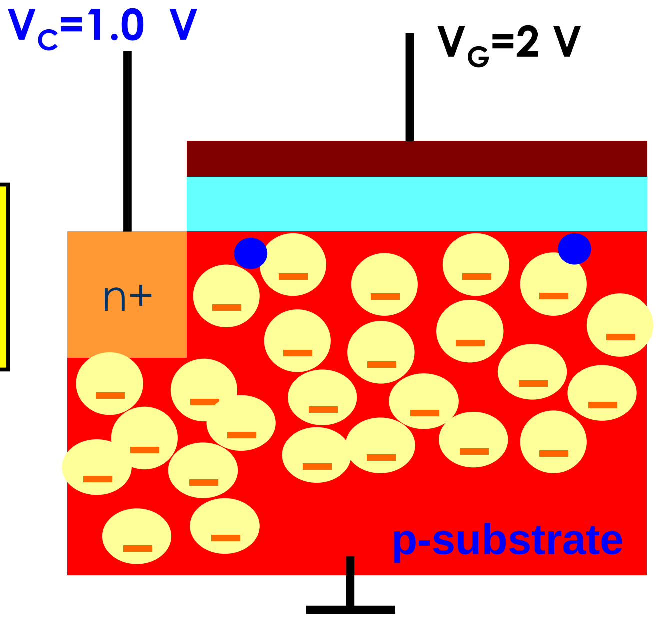
$V_C \rightarrow V_{CB}$

2. The three-terminal MOS structure



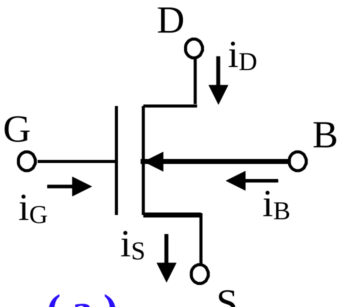


$$V_P - V_C = \phi_t \left[\frac{-Q_I}{nC_{ox}\phi_t} - 1 + \ln\left(\frac{-Q_I}{nC_{ox}\phi_t} \right) \right]$$



3. The NMOS Transistor

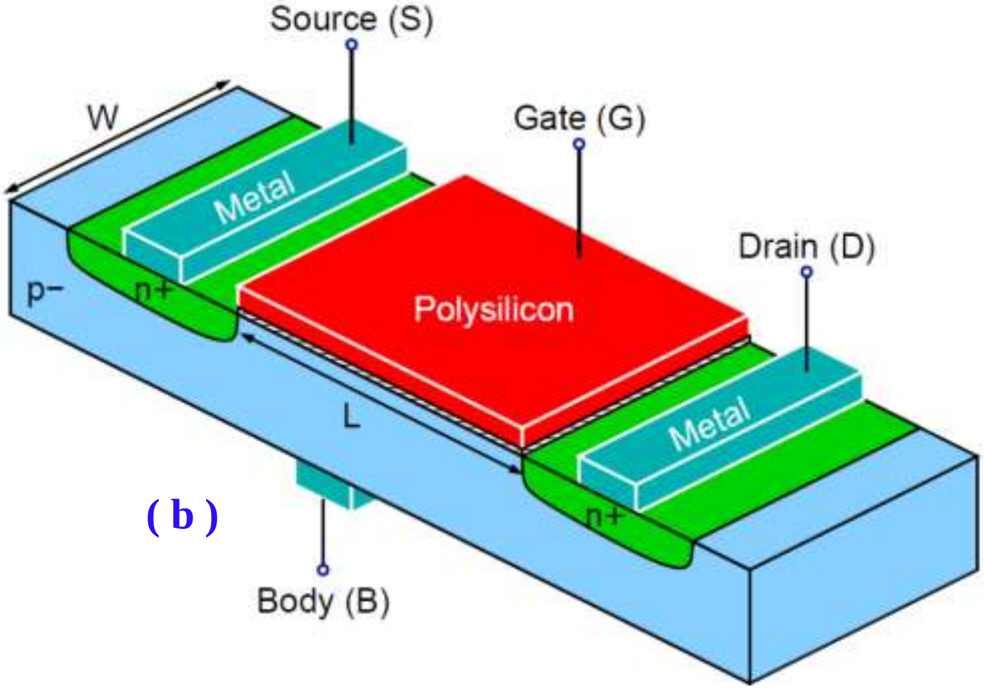
(a) NMOS transistor symbol (b) NMOS transistor structure (c) cross section



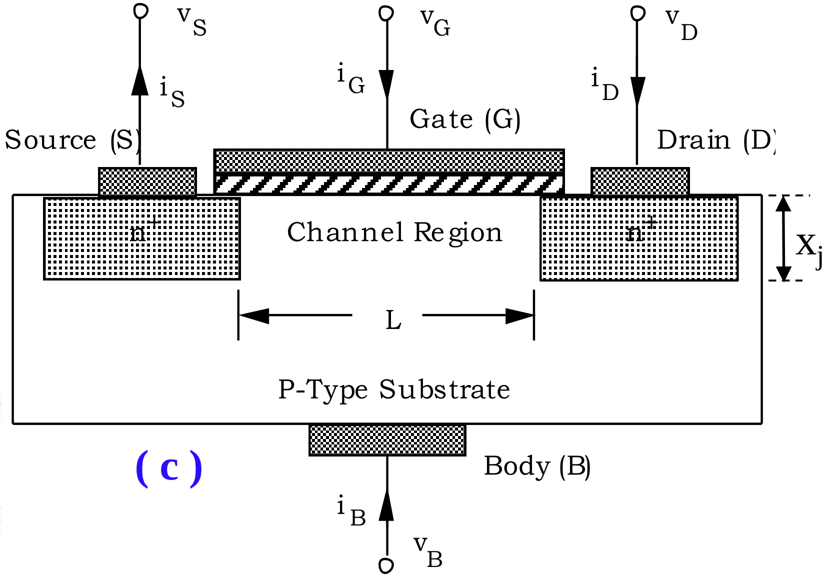
(a)

$$i_G = 0$$
$$i_B = 0$$
$$i_D = i_S$$

Technology	180 nm	65 nm
L_{min} (nm)	180	60
W_{min} (nm)	220	120
t_{ox} (nm)	4	2.6
Metal width, min (nm)	230	90
X_j (nm)	160	86



(b)

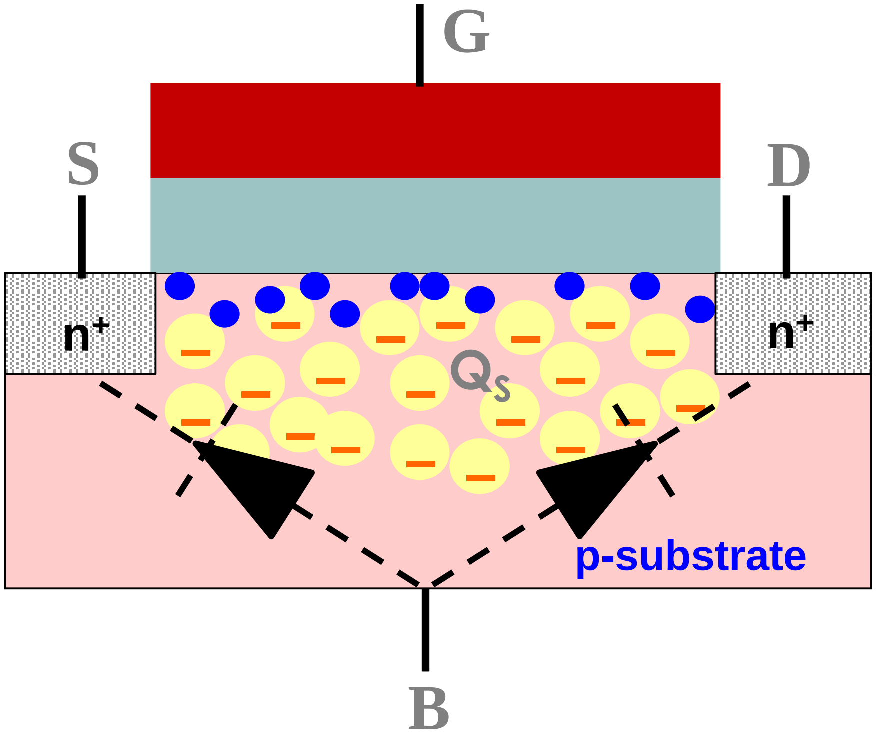


(c)

https://people.engr.tamu.edu/spalermo/ecen474/lecture02_ee474_mos_models.pdf

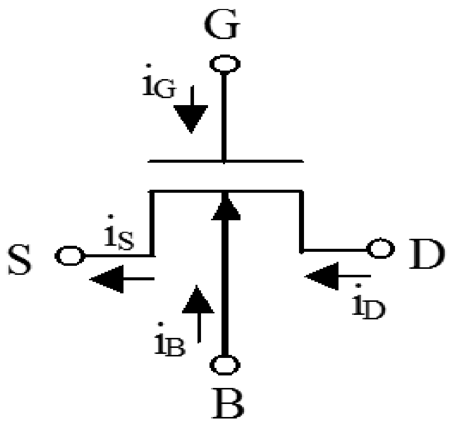
3. The NMOS Transistor

NMOS Transistor =
NMOSCAP +
source & drain terminals



In general, bulk-to-source & bulk-to-drain diodes are reverse (or zero) biased. Thus

$$i_G = 0$$
$$i_B = 0$$
$$i_D = i_S$$



Q_S (semiconductor charge density) =

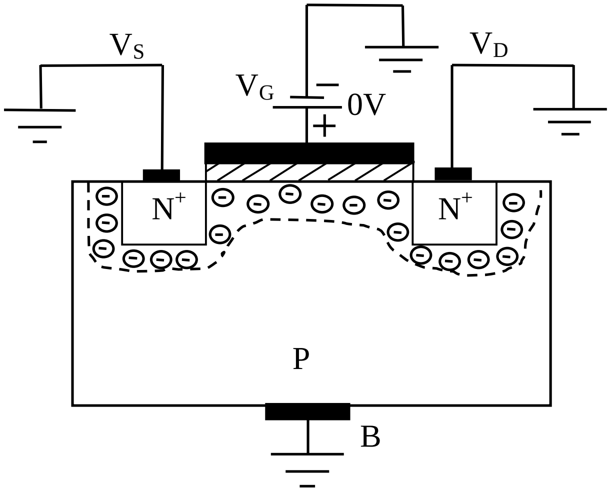
Q_N (carrier charge density)+

Q_D (ion charge density)

mobile
●

fixed

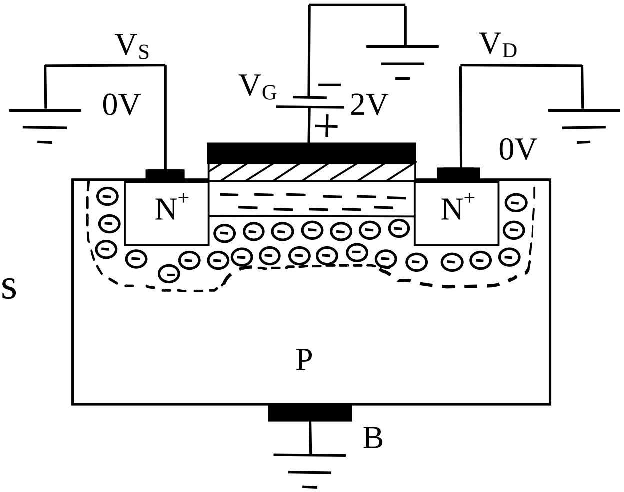
3. The NMOS Transistor



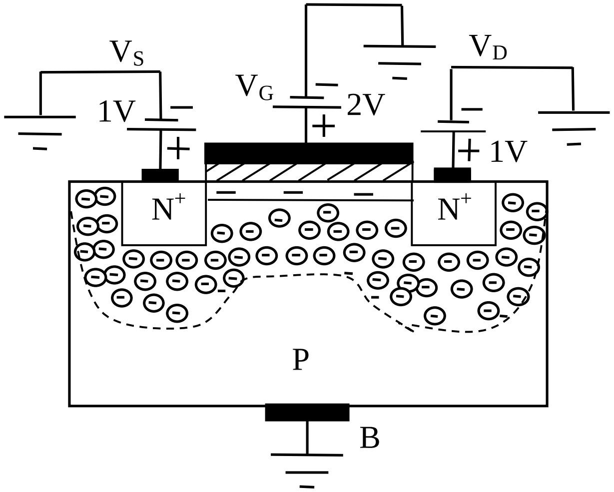
(a) $V_G = 0V$ $V_S = V_D = 0V$

⊖ ions

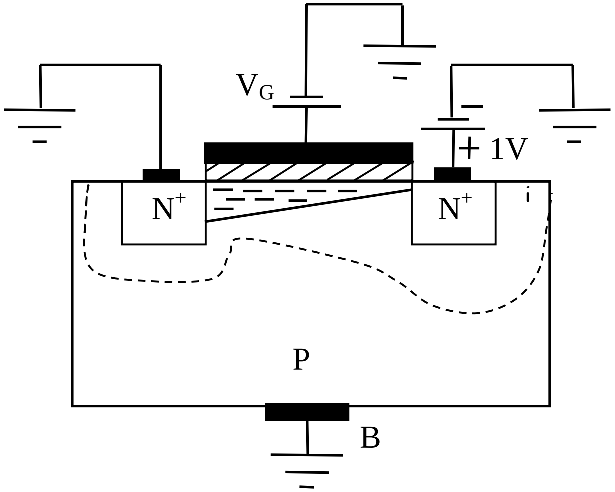
– electrons



(b) $V_G = 2V$ $V_S = V_D = 0V$



(c) $V_G = 2V$ $V_S = V_D = 1V$



(d) $V_G = 2V$ $V_S = 0V$ $V_D = 1V$

4. The physical quantities of the long-channel DC model

Physical quantities

Terminal voltages

V_S, V_D, V_G, V_B

Charge densities

Q_I (carrier charge density)

Q_B (ion charge density)

Q_{IS} (carrier charge density at source)

Q_{ID} (carrier charge density at drain)

Currents

I_D (drain current)

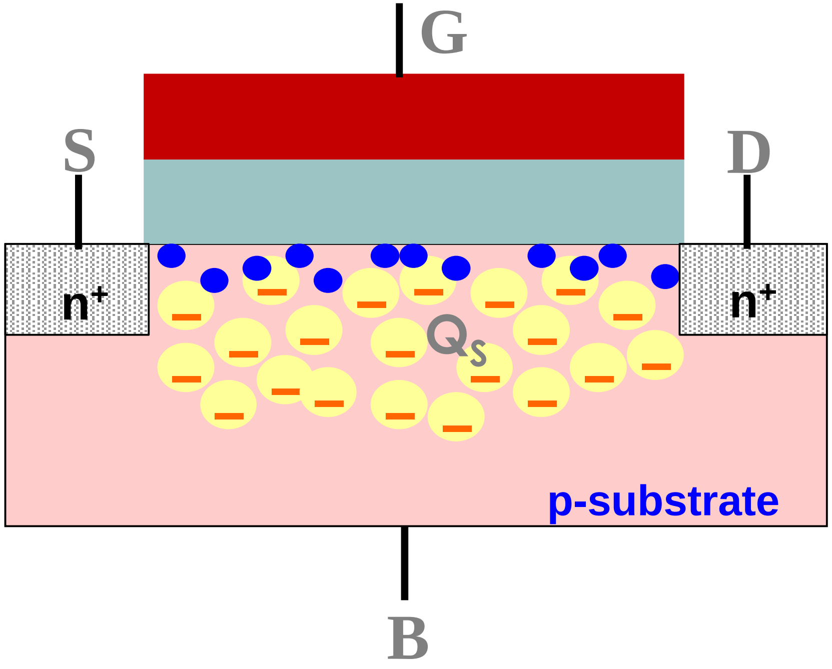
I_F (forward current)

I_R (reverse current)

NMOS Transistor = NMOSCAP

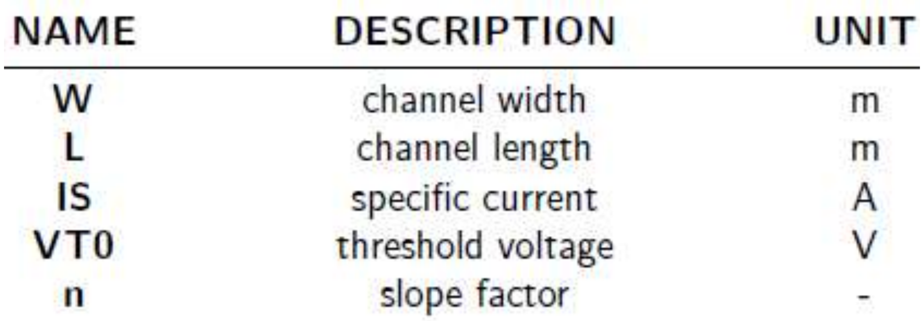
+

source & drain terminals

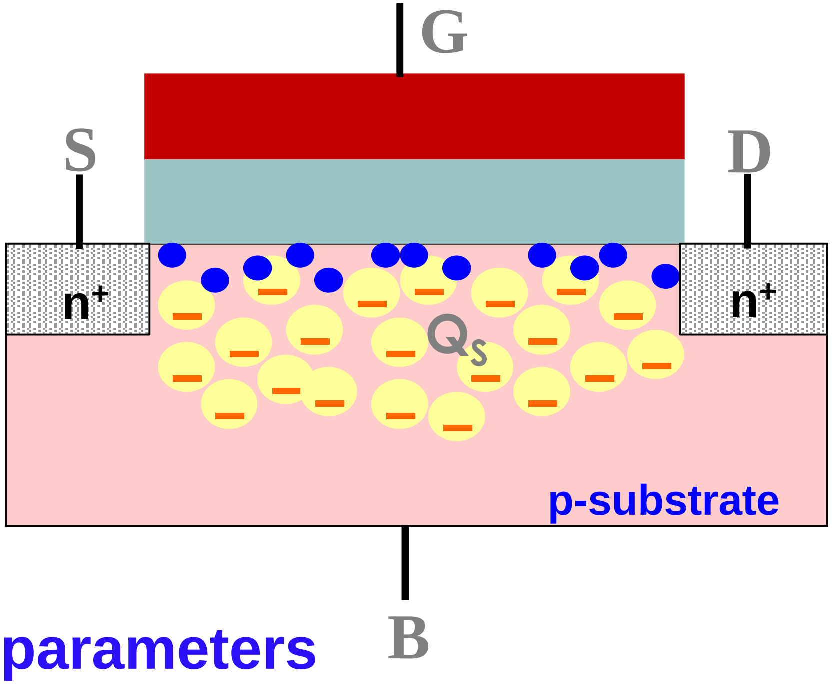


4. The physical quantities of the long-channel DC model

Input parameters



NAME	DESCRIPTION	UNIT
W	channel width	m
L	channel length	m
IS	specific current	A
VT0	threshold voltage	V
n	slope factor	-



Normalization parameters

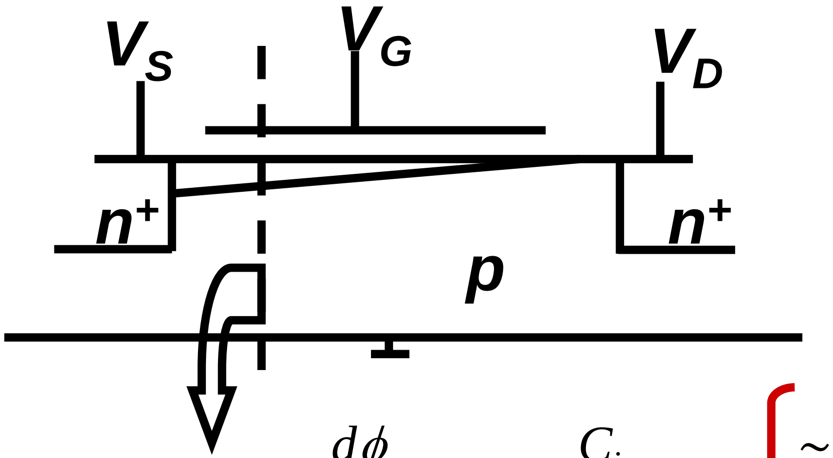
$\phi_t = \frac{kT}{q}$ Thermal voltage

$Q_{IP} = \pm n C_{ox} \phi_t$ Thermal charge density → + P channel → − N channel

$I_S = I_{SH} \frac{W}{L}$ Specific current

$I_{SH} = \mu C_{ox} n \frac{\phi_t^2}{2}$: Sheet specific current

5. The Unified Charge Control Model (UCCM)



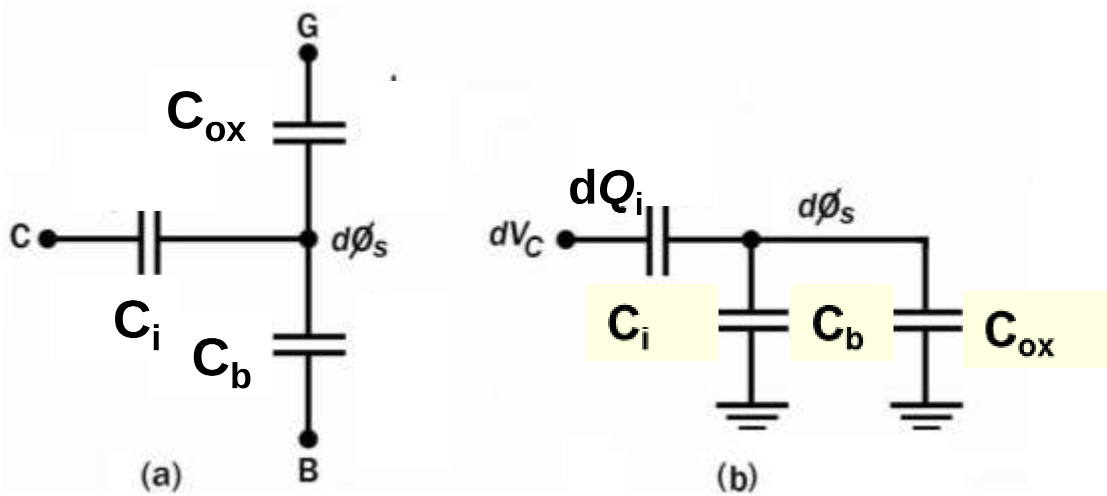
$$C_{ox}+C_b=nC_{ox}$$

$$n=n(V_G)$$

$$dQ_I=nC_{ox}d\phi_s$$

$$\frac{d\phi_s}{dV_C}=\frac{C_i}{C_i+C_{ox}+C_b}\begin{cases}\sim-\dfrac{Q_I}{nC_{ox}\phi_t}<1 & \text{WI}\\ \sim1 & \text{SI}\end{cases}$$

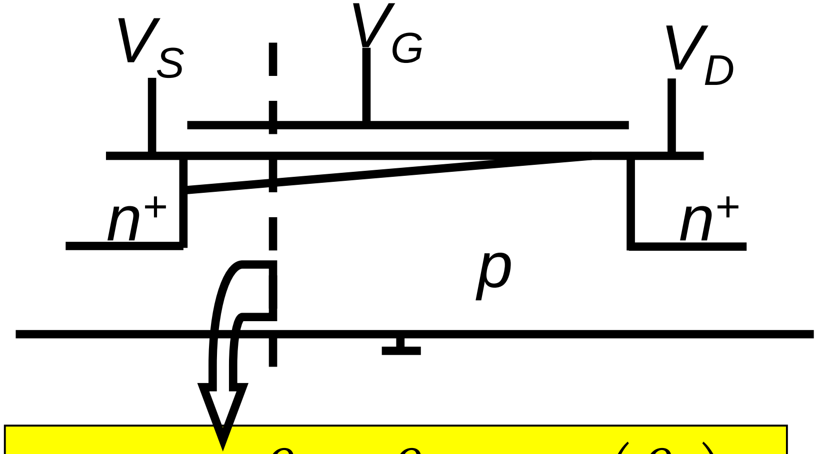
$$C_i=-\frac{Q_I}{\phi_t}$$



$$dV_C=dQ_I\left(\frac{1}{nC_{ox}}-\frac{\phi_t}{Q_I}\right)$$

$$V_S\le V_C\le V_D$$

5 . The Unified Charge Control Model (UCCM)



Channel potential → $V_S \le V_C \le V_D$

$$n = 1 + \frac{C_b}{C_{ox}} = n(V_G)$$ → slightly non-linear function of V_G

$$\boxed{V_P - V_{CB} = \frac{Q_{IP} - Q_I}{nC_{ox}} + \varphi_t \ln\left(\frac{Q_I}{Q_{IP}}\right)}$$

UCCM

$$Q_{IP} = Q_I\Big|_{V_C = V_P}$$

Thermal charge $\boxed{Q_{IP} = -nC_{ox}\varphi_t}$

Pinch-off voltage $\boxed{V_P \cong \frac{V_{GB} - V_T}{n}}$

The normalized inversion (areal) charge density is $\frac{Q_I}{Q_{IP}} = q_I$

Normalized UCCM $\boxed{\frac{V_P - V_{CB}}{\varphi_t} = q_I - 1 + \ln q_I}$

5. The Unified Charge Control Model (UCCM)

$$V_P - V_C = \frac{Q_{IP} - Q_I}{nC_{ox}} + \varphi_t \ln\left(\frac{Q_I}{Q_{IP}}\right)$$

UCCM

$$\frac{V_P - V_C}{\varphi_t} = q_I - 1 + \ln q_I$$

Normalized UCCM

The “Regional” Weak (WI) and Strong Inversion (SI) Approximations

WI

$$q_I \ll 1 \;\rightarrow V_P - V_C \ll -\varphi_t$$

$$q_I \cong e^{\frac{V_P - V_C + \varphi_t}{\varphi_t}}$$

Error <10% for $q_I < 0.22$

SI

$$q_I \gg 1 \;\rightarrow V_P - V_C \gg \varphi_t$$

$$q_I \;\cong \frac{V_P - V_C + \varphi_t}{\varphi_t}$$

Error <10% for $q_I > 20$

$0.22 < q_I < 20$ → **Moderate inversion**

5. The Unified Charge Control Model (UCCM)

$$V_P - V_{S(D)B} = \frac{Q_{IP} - Q_{IS(D)}}{nC_{ox}} + \varphi_t \ln\left(\frac{Q_{IS(D)}}{Q_{IP}}\right)$$

UCCM at source (drain)

$$\frac{V_P - V_{S(D)B}}{\varphi_t} = q_{S(D)} - 1 + \ln q_{S(D)}$$

Normalized UCCM at source (drain)

The pinch-off voltage V_P

$$V_P = \left[\sqrt{V_G - V_{T0} + \left(\sqrt{2\phi_F} + \frac{\gamma}{2}\right)^2} - \frac{\gamma}{2}\right]^2 - 2\phi_F$$

Useful approximation:

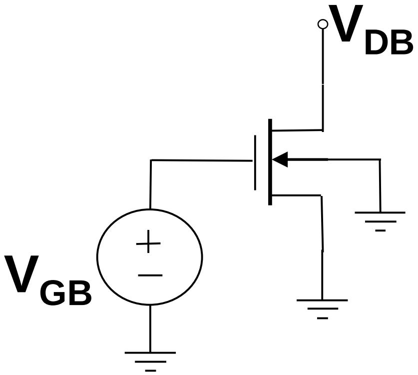
$$V_P \cong \frac{V_{GB} - V_{T0}}{n}$$

Use of UCCM applied to an NMOS transistor. Parameters:
$n=1.25$, $C_{ox}= 1\ \mathrm{uF/cm^2}$, $\phi_t = 26\ \mathrm{mV}$, $V_T = 0.5\ \mathrm{V}$, W=L= 1 um.
Complete the table below.

$$\frac{V_P - V_{S(D)B}}{\varphi_t} = q_{S(D)} - 1 + \ln q_{S(D)}$$

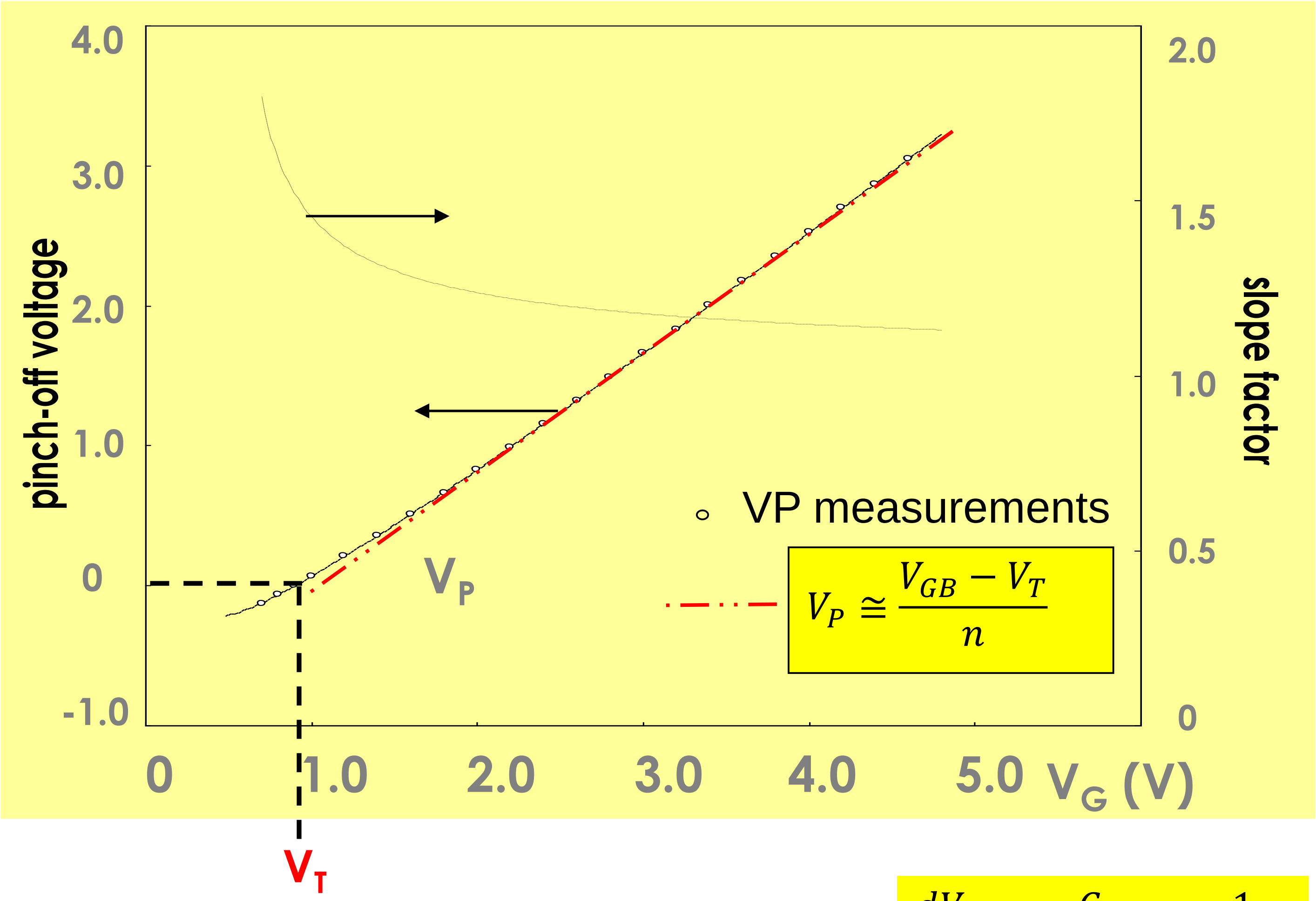
$$\boxed{V_P \cong \frac{V_{GB} - V_{T0}}{n}}$$

V_{GB} **(V)**	V_P **(V)**	V_{DB} **(V)**	q_S **(-)**	q_D **(-)**
318 m	-146 m	0	0.01	0.01
461 m	-31 m	97 m	0.5	0.05
500 m	0	86.3 m	1	0.1
600 m	80 m	36 m	3	2
867 m	241 m	95.2 m	10	5
1.55	842 m	408 m	30	15



5. The Unified Charge Control Model (UCCM)

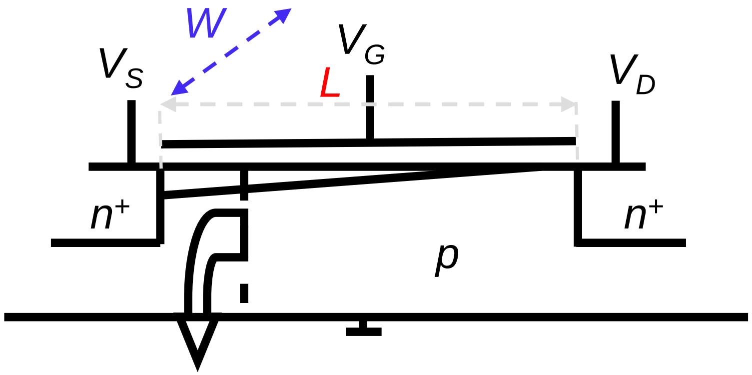
Pinch-off voltage and slope factor vs. gate voltage



$$V_P \cong \frac{V_{GB} - V_T}{n}$$

$$\frac{dV_P}{dV_G} = \frac{C_{ox}}{C_b + C_{ox}} = \frac{1}{n}$$

6. The Unified Current Control Mode (UICM)



$$\frac{Q_{IP}-Q_I}{nC_{ox}}+\phi_t\ln\left(\frac{Q_I}{Q_{IP}}\right)=V_P-V_C$$

UCCM

$$\frac{-dQ_I}{nC_{ox}}+\phi_t\frac{dQ_I}{Q_I}=-dV_C$$

Differential UCCM

Using

$$I_D=-\frac{\mu_n W}{L}\int_{Q_{IS}}^{Q_{ID}}Q_I\,dV_C$$

Pao-Sah equation

and differential UCCM :

$$I_D=\frac{\mu_n W}{L}\left[\frac{Q_{IS}^2-Q_{ID}^2}{nC_{ox}}-\phi_t(Q_{IS}-Q_{ID})\right]$$

drift + diffusion

6. The Unified Current Control Mode (UICM)

With charge density normalization $q_{S(D)} = Q_{IS(D)}/(-nC_{ox}\phi_t)$

$$\boxed{I_D = \frac{\mu_n W}{L}\left[\frac{Q_{IS}^2 - Q_{ID}^2}{nC_{ox}} - \phi_t(Q_{IS} - Q_{ID})\right]}$$

is written as

$$\boxed{I_D = I_S[(q_S^2 + 2q_S) - (q_D^2 + 2q_D)]}$$

(A)

$$I_S = \mu_n C_{ox} n \frac{\phi_t^2}{2}\frac{W}{L} = \frac{W}{L} I_{SH} = S\ I_{SH}$$

I_S : specific (normalization) current

I_{SH}: sheet specific current

S : aspect ratio

(A) can also be written as

$$\boxed{I_D = I_F - I_R = I_S\left[i_f - i_r\right]}$$

$\boxed{I_F, I_R}$: forward and reverse currents

$\boxed{i_{f(r)} = q_{S(D)}^2 + 2q_{S(D)}}$: forward (reverse) inversion coefficients

6. The Unified Current Control Mode (UICM)

$$i_{f(r)} = q_{S(D)}^2 + 2q_{S(D)}$$

$$q_{S(D)} = \sqrt{1 + i_{f(r)}} - 1$$

Normalized UCCM

$$\frac{V_P - V_{S(D)B}}{\varphi_t} = q_{S(D)} - 1 + \ln q_{S(D)}$$

Normalized UICM

$$\frac{V_P - V_{S(D)B}}{\varphi_t} = \sqrt{1 + i_{f(r)}} - 2 + \ln\left(\sqrt{1 + i_{f(r)}} - 1\right)$$

Normalized current as a function of normalized carrier densities

$$i_D = \frac{I_D}{I_S} = (q_S^2 + 2q_S) - (q_D^2 + 2q_D)$$

For a PMOS transistor:

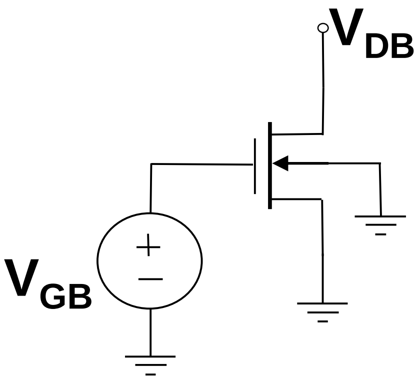
$$\frac{V_P - V_{S(D)B}}{\varphi_t} = -\left[\sqrt{1 + i_{f(r)}} - 2 + \ln\left(\sqrt{1 + i_{f(r)}} - 1\right)\right]$$

Use of UICM applied to an NMOS transistor. Parameters:
$n=1.25$, $C_{ox}= 1$ uF/cm^2, $\phi_t = 26$ mV, $V_T = 0.5$ V, W=L= 1 um.
Complete the table below.

$$\frac{V_P - V_{S(D)B}}{\varphi_t} = -\left[\sqrt{1+i_{f(r)}} - 2 + \ln\left(\sqrt{1+i_{f(r)}} - 1\right)\right]$$

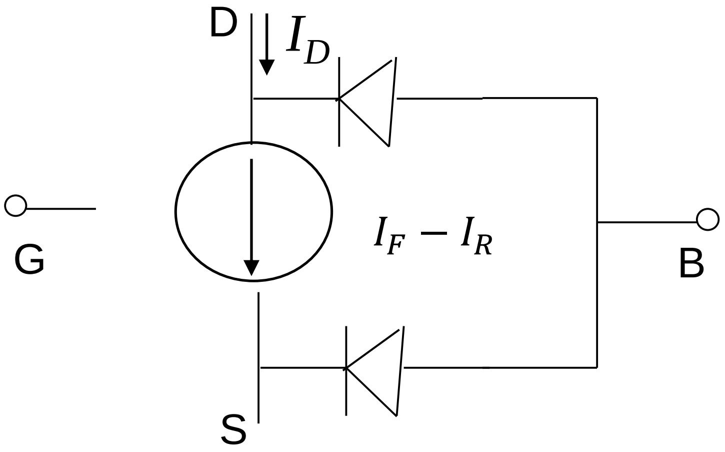
$$V_P \cong \frac{V_{GB} - V_{T0}}{n}$$

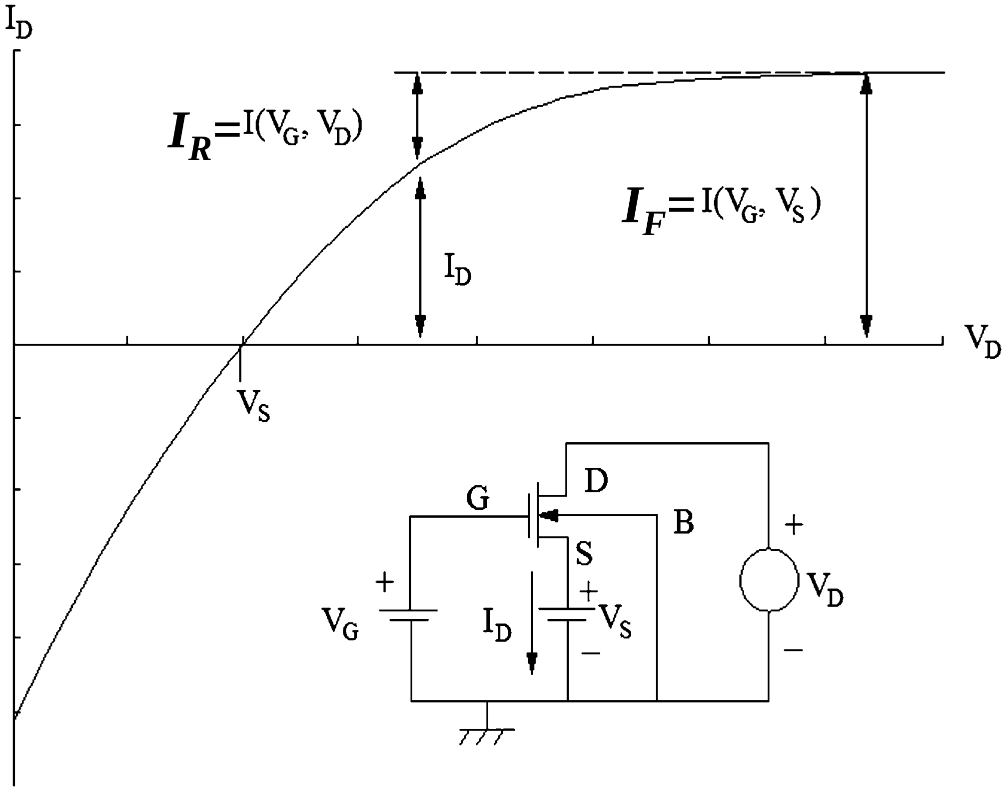
V_{GB}(V)	V_P(V)	V_{DB}(V)	q_S(-)	q_D(-)	i_f	i_r
318 m	-146 m	0	0.01	0.01	0.02	0.02
461 m	-31 m	97 m	0.5	0.05	1.25	0.102
500 m	0	86.3 m	1	0.1	3	0.21
600 m	80 m	36 m	3	2	15	8
867 m	241 m	95.2 m	10	5	120	35
1.55	842 m	408 m	30	15	960	255



6. The Unified Current Control Model (UICM)

Long-channel dc model:
forward and reverse components of the current





Saturation: $I_F \gg I_R \rightarrow I_D \cong I_F$

$V_D = V_S \rightarrow I_D = 0 \rightarrow I_F = I_R$

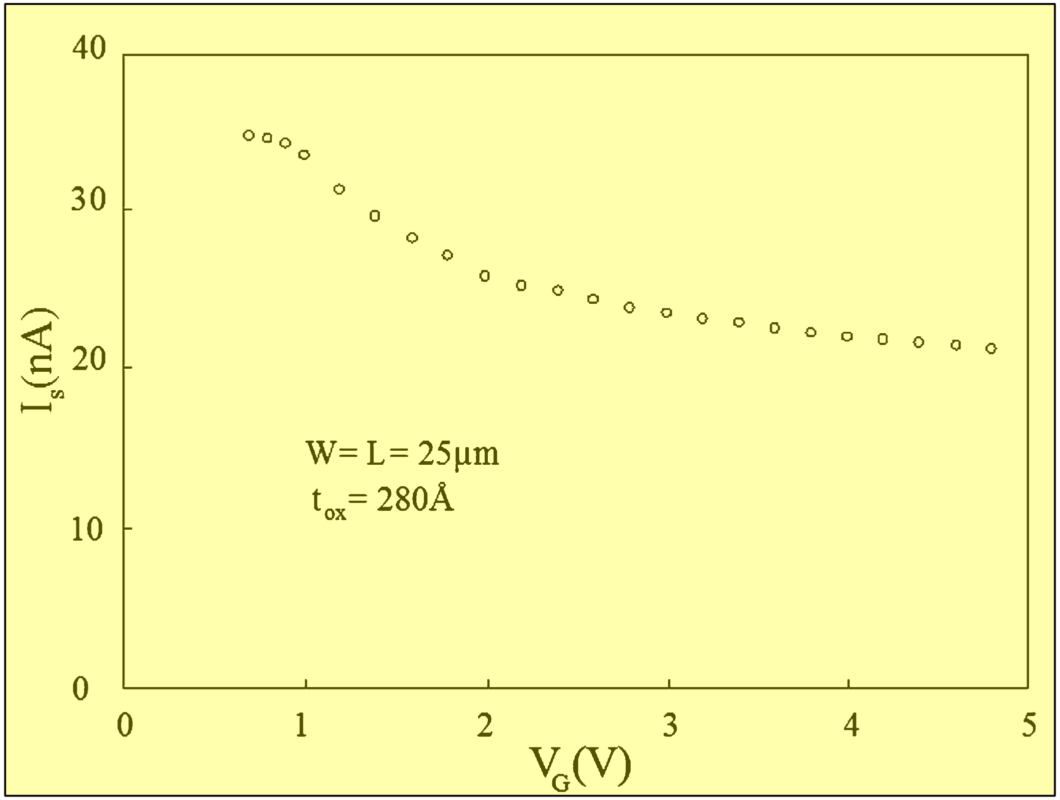
6. The Unified Current Control Mode (UICM)

The specific (normalization) current

$$I_S = \mu C_{ox} n \frac{\phi_t^2}{2} \frac{W}{L} = I_{SH} \frac{W}{L}$$

Typical values of I_{SH} of long/wide channel MOSFETs

Technology	NMOSFET	PMOSFET
350 nm	75 nA	25 nA
180 nm	100 nA	40 nA
65 nm	150 nA	50 nA

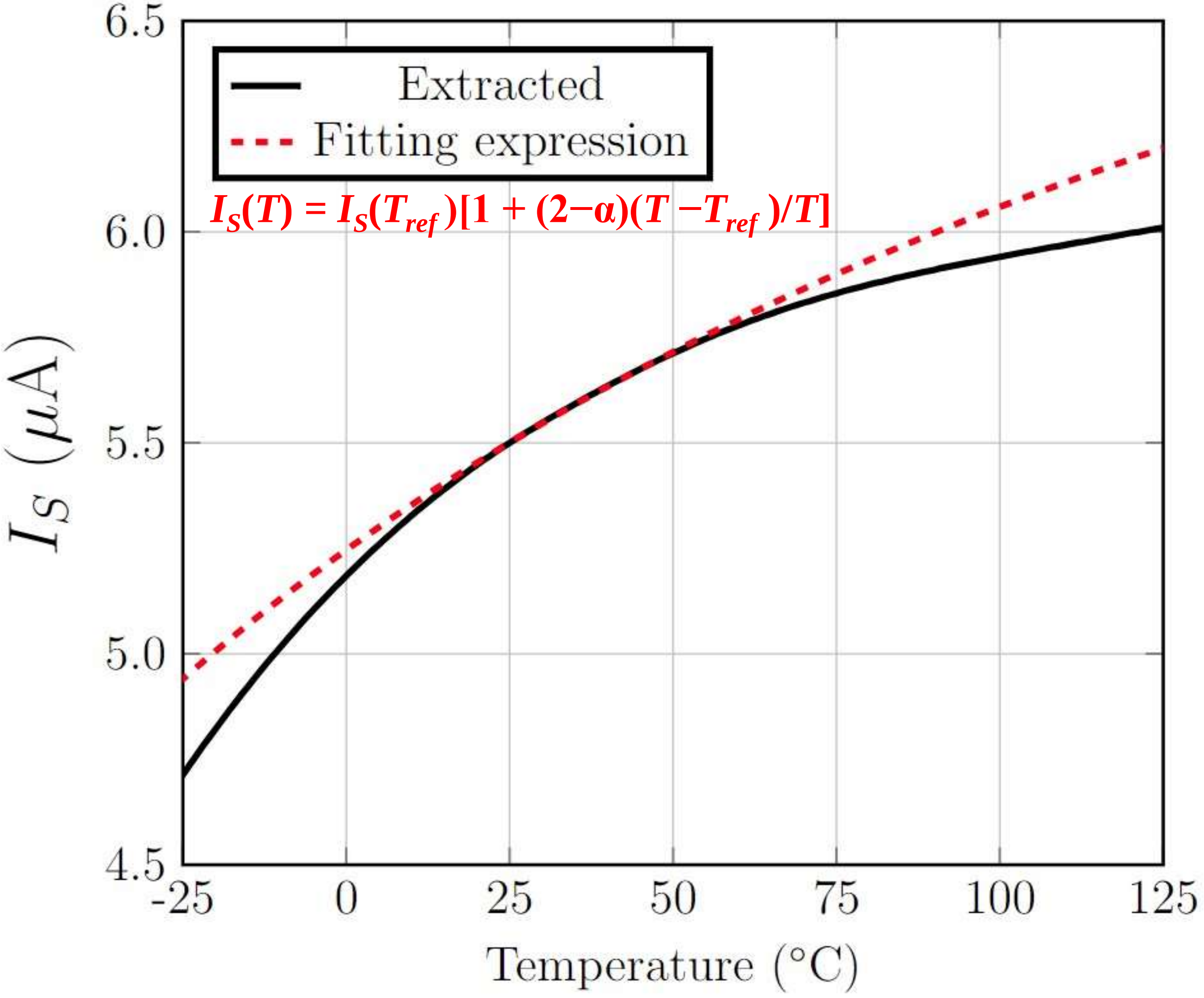


Sheet specific current of PMOS transistor 0.35 µm CMOS technology

6. The Unified Current Control Mode (UICM)

$$I_S = \mu C_{ox} n \frac{\phi_t^2}{2}\frac{W}{L} = I_{SH}\frac{W}{L}$$

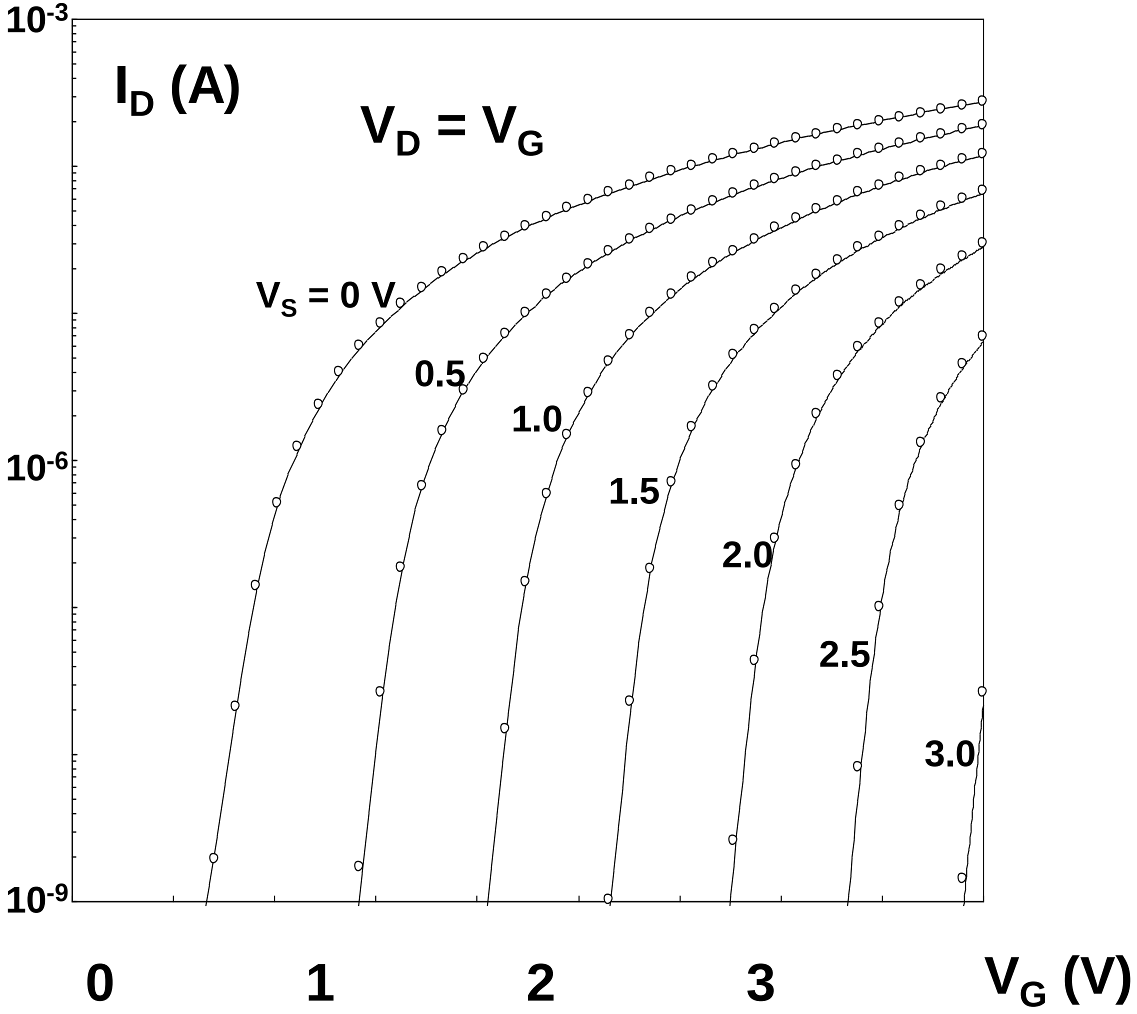
$\mu \propto T^{-\alpha}$

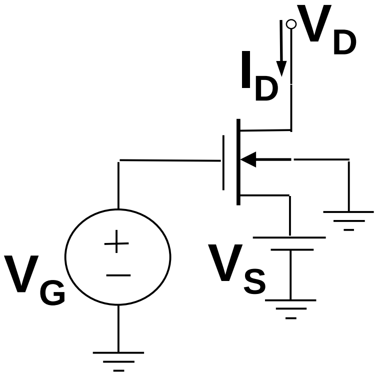


$I_S(T) = I_S(T_{ref})[1 + (2-\alpha)(T - T_{ref})/T]$

6. The Unified Current Control Mode (UICM)

$$V_P - V_S = \phi_t \left[\sqrt{1+i_f} - 2 + \ln\left(\sqrt{1+i_f} - 1\right) \right]$$





Common-source characteristics

6. The Unified Current Control Mode (UICM)

$$V_P - V_S = \phi_t\left[\sqrt{1+i_f} - 2 + \ln\left(\sqrt{1+i_f} - 1\right)\right]$$

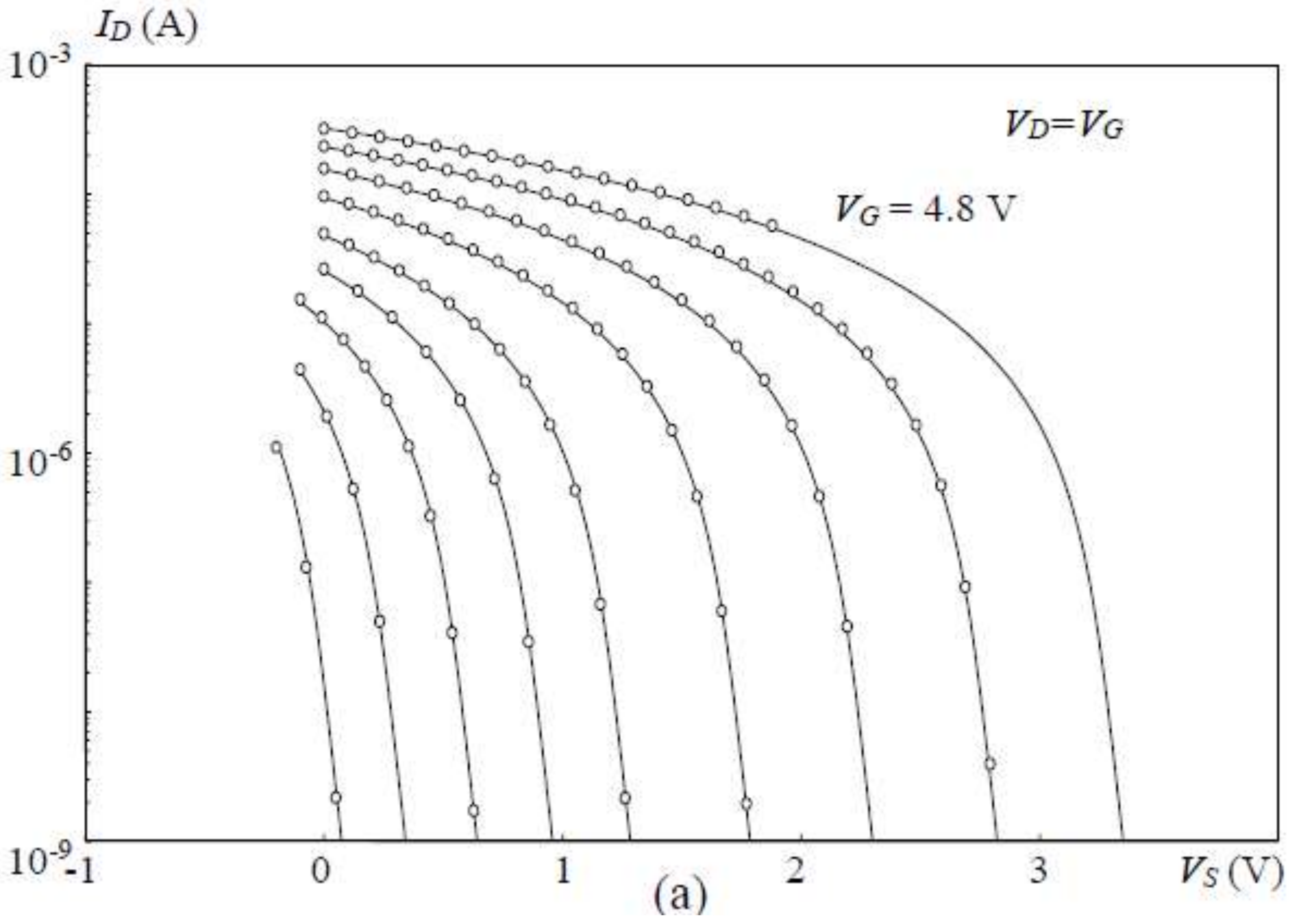


Fig. 2.9 Common-gate characteristics of NMOS transistor (t_{ox}=280 Å, W=L=25 μm) in saturation (V_G=0.8, 1.2, 1.6, 2.0, 2.4, 3.0, 3.6, 4.2, 4.8 V). (—) simulated and (O) measured data.

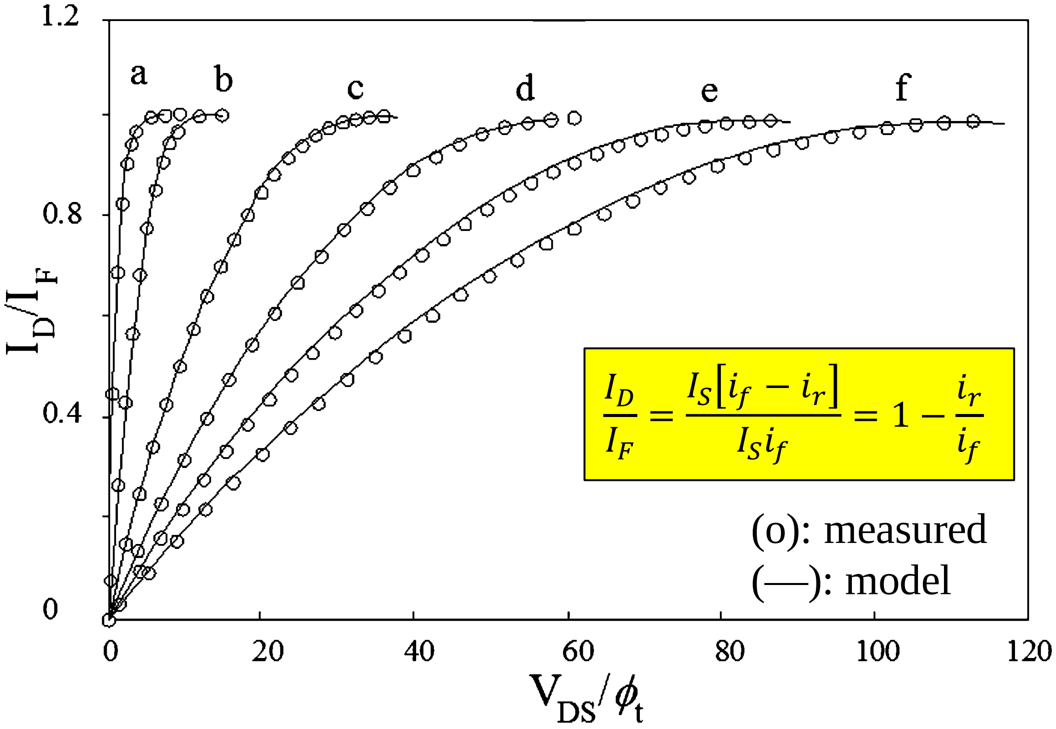
6. The Unified Current Control Mode (UICM)

Long-channel dc model:Universal output characteristics

(I) $$\frac{\frac{V_{GB}-V_{T0}}{n}-V_{S(D)B}}{\phi_t}=\sqrt{1+i_{f(r)}}-2+\ln\left(\sqrt{1+i_{f(r)}}-1\right)$$

The application of (I) to source and drain gives:

$$\frac{V_{DS}}{\phi_t}=q_S-q_D+\ln\frac{q_S}{q_D}=\sqrt{1+i_f}-\sqrt{1+i_r}+\ln\left(\frac{\sqrt{1+i_f}-1}{\sqrt{1+i_r}-1}\right)$$



$$\frac{I_D}{I_F}=\frac{I_S[i_f-i_r]}{I_S i_f}=1-\frac{i_r}{i_f}$$

(a) i_f= 4.5x 10^{-2} (V_G=0.7 V).
(b) i_f= 65 (V_G= 1.2 V).
(c) i_f= 9.5x10^2 (V_G= 2.0 V).
(d) i_f= 3.1x 10^3 (V_G= 2.8 V).
(e) i_f= 6.8x 10^3 (V_G= 3.6 V).
(f) i_f= 1.2x 10^4 (V_G= 4.4 V).

6. The Unified Current Control Mode (UICM)

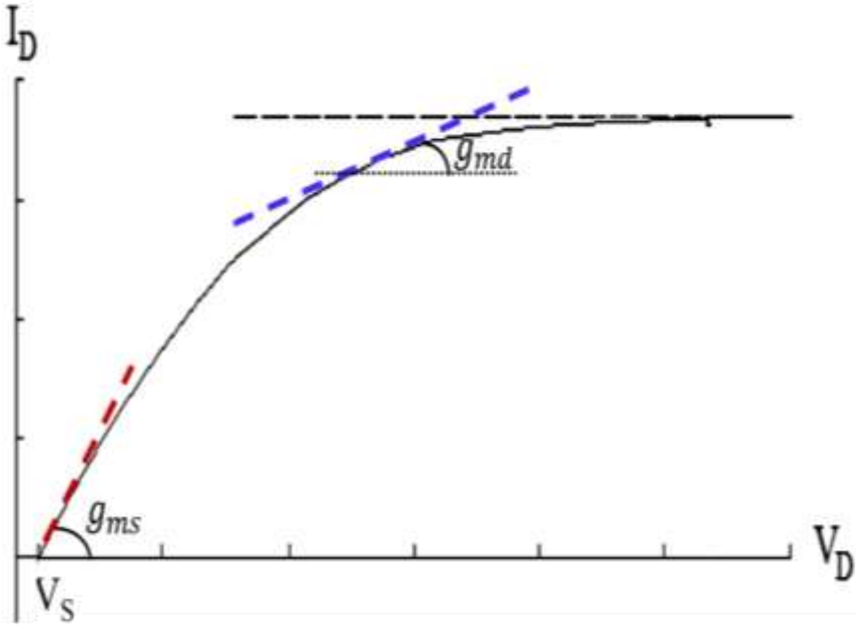
Long-channel dc model: The saturation voltage

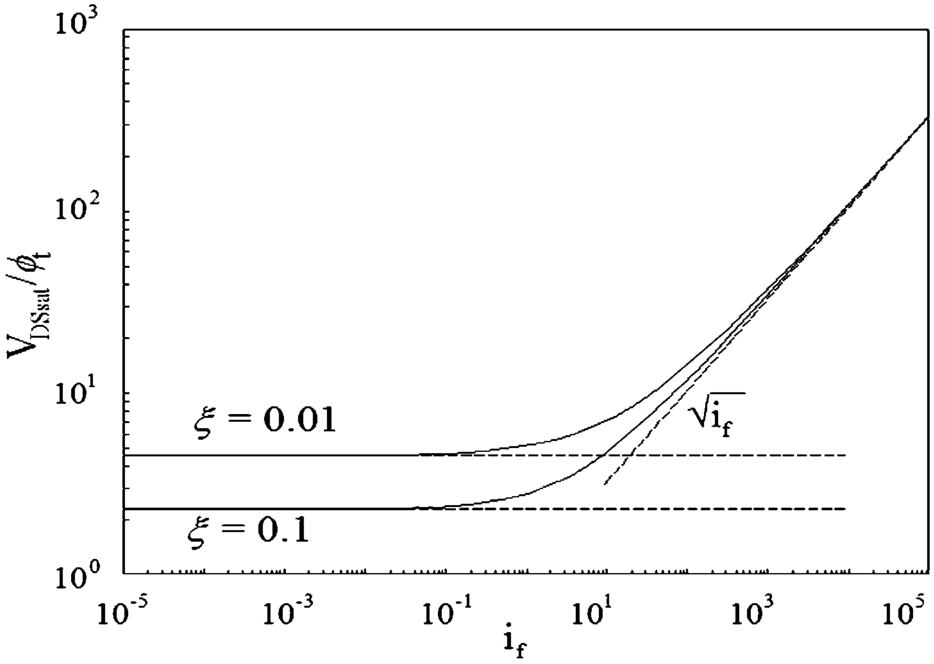
$V_{DSsat} = V_{DS}$ **such that**

$$g_{md}/g_{ms} = \frac{q_{ID}}{q_{IS}} = \xi \ll 1$$

UCCM

$$V_{DSsat} = \phi_t \left[\ln\left(\frac{1}{\xi}\right) + (1-\xi)\left(\sqrt{1+i_f} - 1\right) \right]$$





$(1-\xi)$ is the saturation level

A practical approximation for the saturation voltage:

$$V_{DSsat} \cong \phi_t\left(\sqrt{1+i_f} + 3\right)$$

6. The Unified Current Control Mode (UICM)

Long-channel dc model: Weak inversion

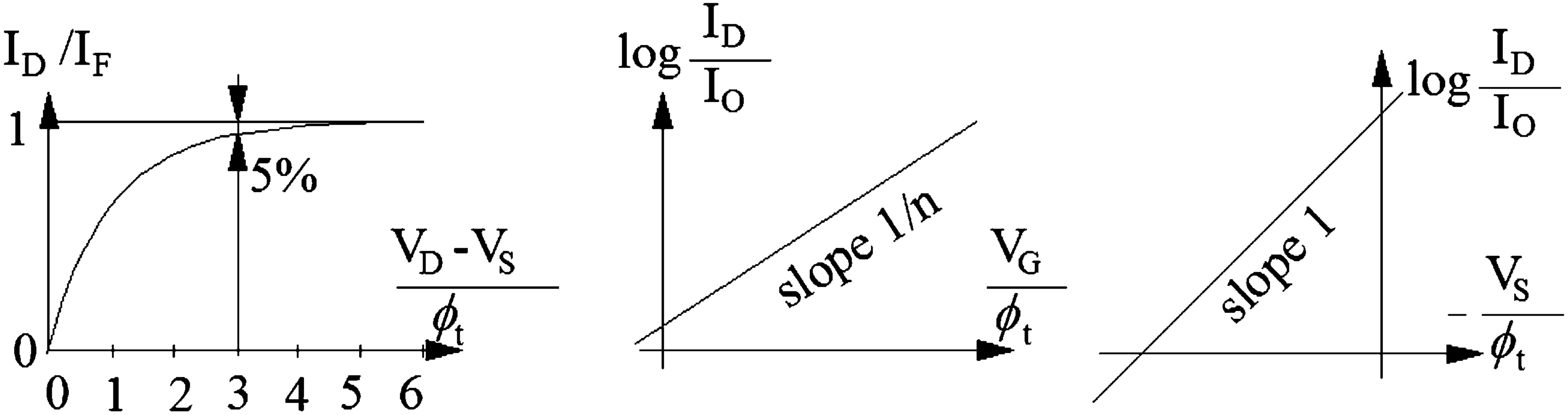
Weak inversion

$i_{f(r)} < 1$

$$\frac{V_G - V_{T0}}{n} - V_{S(D)} = \phi_t\left[\underbrace{\sqrt{1+i_{f(r)}} - 2}_{-1} + \ln\underbrace{\left(\sqrt{1+i_{f(r)}} - 1\right)}_{i_{f(r)}/2}\right]$$

$$\boxed{I_D = I_0 e^{\left(\frac{V_G - V_{T0}}{n} - V_S\right)/\phi_t}\left[1 - e^{-V_{DS}/\phi_t}\right]}$$

$$\boxed{I_0 = \mu_n \frac{W}{L} n C_{ox} \phi_t^2 e^1 = 2 I_S e^1}$$


V_G , V_S = const.

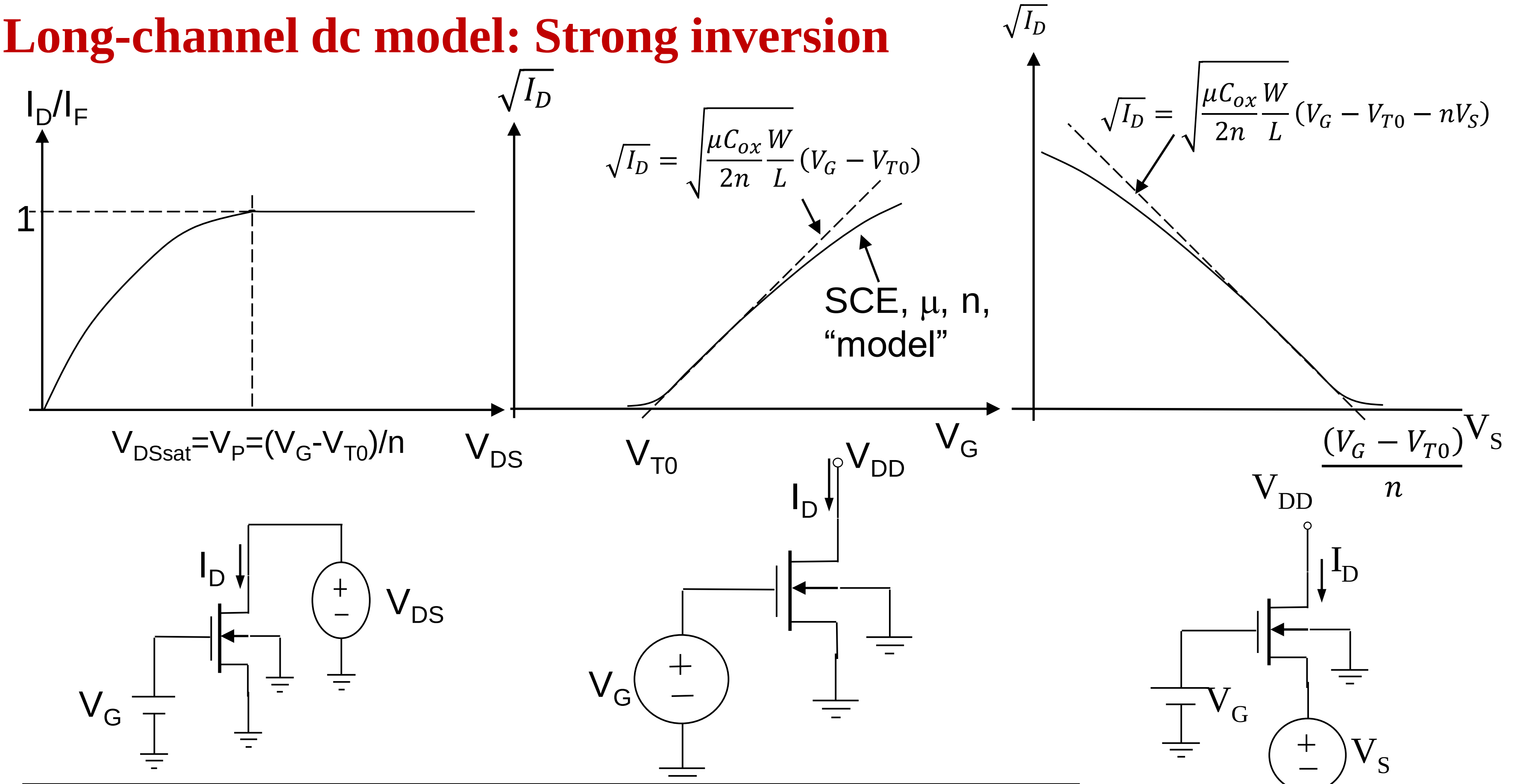
V_S , V_D = const.

V_G , V_D = const.

E. Vittoz, “MOS Transistor: Model and Modes of Operation,” Course on Advanced Analog CMOS IC Design, 2019

6. The Unified Current Control Mode (UICM)

Long-channel dc model: Strong inversion



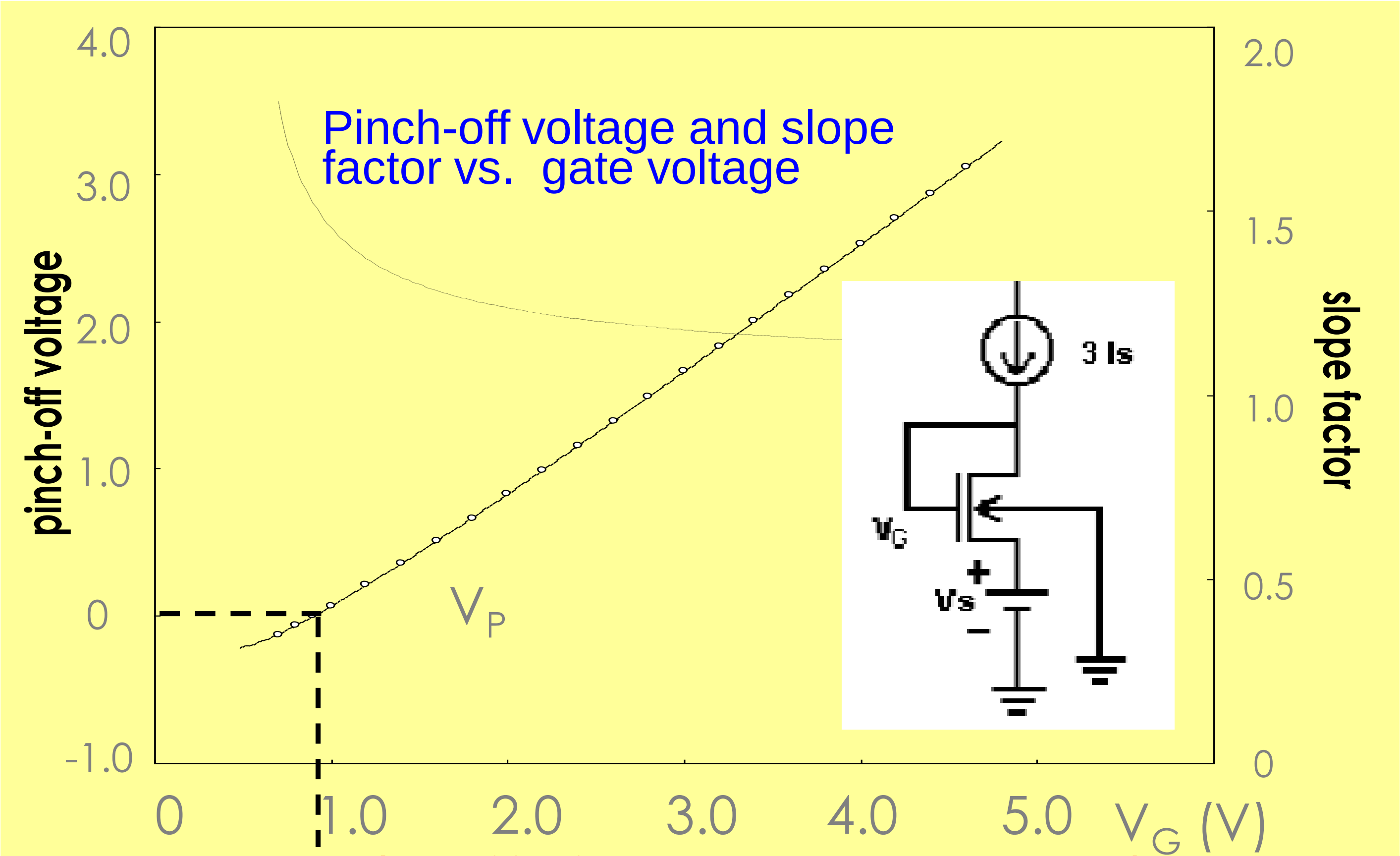
$$I_D = I_F - I_R \cong \mu_n C_{ox}\frac{W}{2nL}\left[\left(V_G - V_{T0} - nV_S\right)^2 - \left(V_G - V_{T0} - nV_D\right)^2\right]$$

Moderate inversion
$1 < i_{f(r)} < 100$

➡ Both sqrt(.) and ln(.) terms of UICM are important

6. The Unified Current Control Mode (UICM)

Long-channel dc model: $V_P (V_G)$ & $n(V_G)$



V_{T0} (equilibrium threshold voltage)

$$I_D = I_F - I_R \cong I_F = 3 I_S$$

$$i_f = 3$$

$$V_P \cong \frac{V_G - V_{T0}}{n}$$

$$\frac{V_P - V_S}{\phi_t} = \sqrt{1 + i_f} - 2 + \ln\left(\sqrt{1 + i_f} - 1\right) \Rightarrow V_P - V_S\Big|_{i_f = 3} = 0 \ \rightarrow V_G = V_{T0}\Big|_{V_S = 0}$$

6. The Unified Current Control Mode (UICM)

The I-V relationship (NMOS & PMOS)

$$\frac{V_P - V_{S(D)B}}{\phi_t} = q_{IS(D)} - 1 + \ln q_{IS(D)}$$

Normalized UCCM

&

$$i_{f(r)} = q_{IS(D)}^2 + 2q_{IS(D)}$$

Normalized i-q relationship

$$q_{IS(D)} = \sqrt{1 + i_{f(r)}} - 1$$

$$\frac{\frac{V_{GB} - V_{T0}}{n} - V_{S(D)B}}{\phi_t} = \sqrt{1 + i_{f(r)}} - 2 + \ln\left(\sqrt{1 + i_{f(r)}} - 1\right)$$

NMOS

Normalized UICM

UICM = Unified Current Control Model

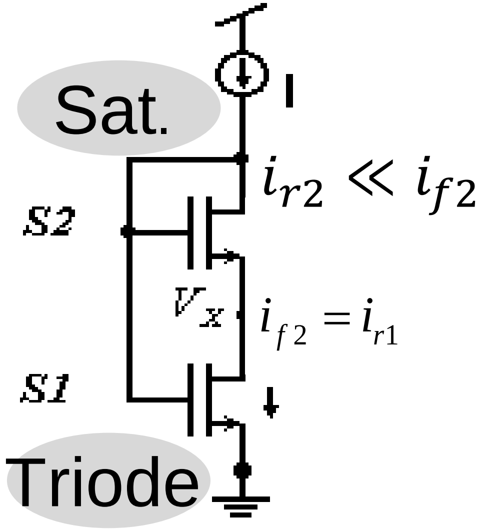
$$-\left(\frac{\frac{V_{GB} - V_{T0}}{n} - V_{S(D)B}}{\phi_t}\right) = \sqrt{1 + i_{f(r)}} - 2 + \ln\left(\sqrt{1 + i_{f(r)}} - 1\right)$$

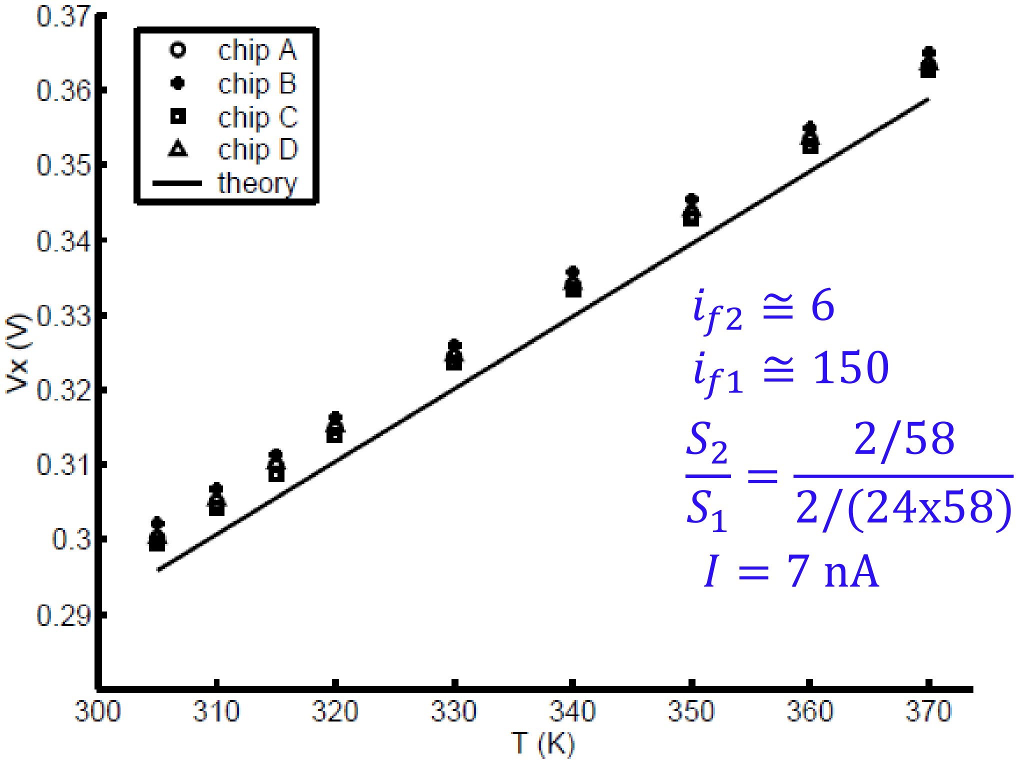
PMOS

6. The Unified Current Control Mode (UICM)

Circuit #1: PTAT voltage generator using an MOS voltage divider

Bias current I is proportional to the transistor specific (normalization) current I_S.





$i_{f2} \cong 6$

$i_{f1} \cong 150$

$$\frac{S_2}{S_1} = \frac{2/58}{2/(24\text{x}58)} = 24$$

$I = 7$ nA

$$I = I_{S2} i_{f2} = I_{S1}(i_{f1} - i_{f2})$$

$$i_{f1} = \left(1+\frac{I_{S2}}{I_{S1}}\right) = \left(1+\frac{S_2}{S_1}\right) i_{f2} = \alpha i_{f2}$$

Applying UICM to M1 ⇨

$$\boxed{\frac{V_X}{\phi_t} = \sqrt{1+\alpha i_{f2}} - \sqrt{1+i_{f2}} + \ln\left(\frac{\sqrt{1+\alpha i_{f2}}-1}{\sqrt{1+i_{f2}}-1}\right)}$$

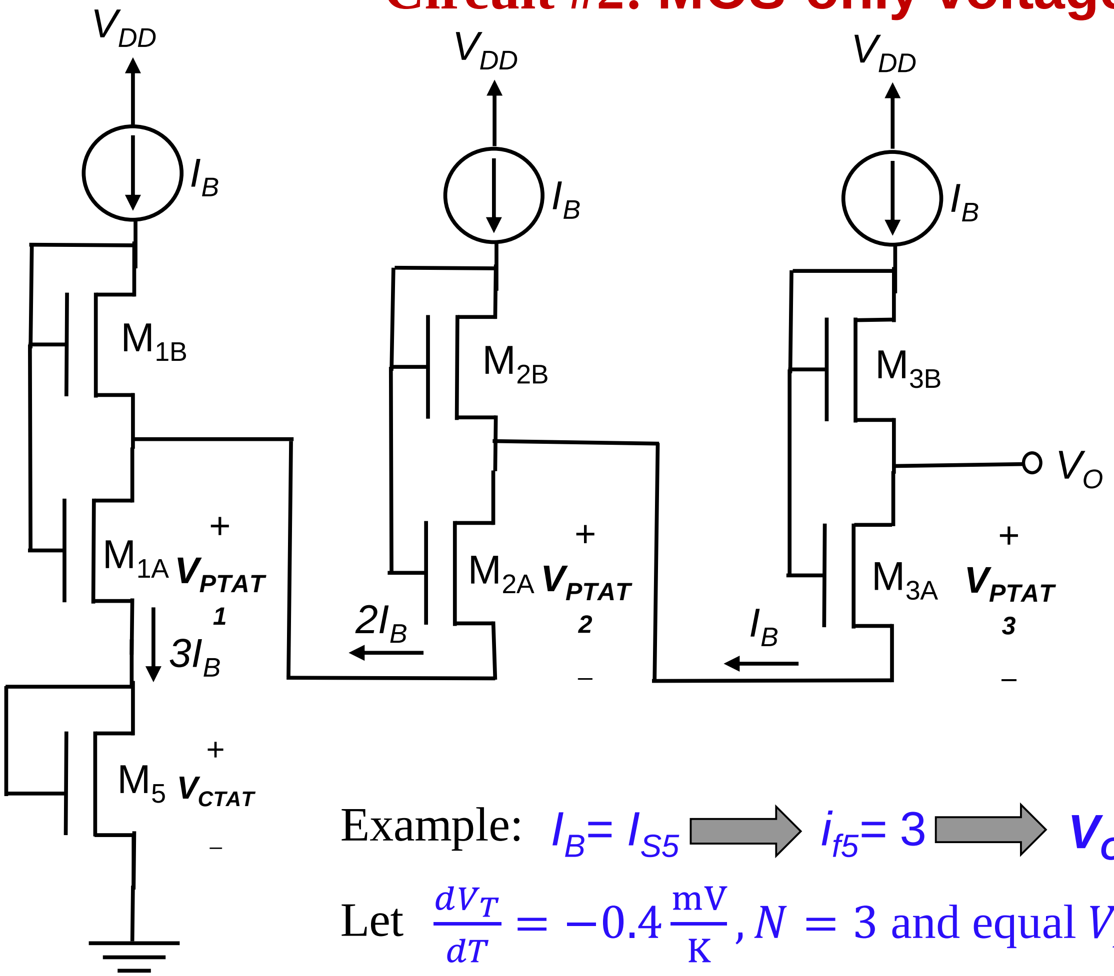
In weak inversion,

$i_{f1} \ll 1$ $\boxed{\frac{V_X}{\phi_t} \to \ln \alpha}$

C. Rossi, C. Galup-Montoro and M.C. Schneider, "PTAT voltage generator based on an MOS voltage divider", Proceedings of Nanotech 2007, pp. 626- 629, May 2007.

6. The Unified Current Control Mode (UICM)

Circuit #2: MOS-only voltage reference



$$\boxed{V_O = V_{CTAT} + \sum_{i=1}^{N} V_{PTATi}}$$

	W/L (μm/μm)	i_f	i_r
M5	1/1	3	<<3
M1A	20/1	19/100	1/25
M1B	25/1	1/25	<<1/25
M2A	20/1	4.7/37	1/37
M2B	37/1	1/37	<<1/37
M3A	20/1	4.7/74	1/74
M3B	74/1	1/74	<<1/74

Example: $I_B = I_{S5}$ ⇒ $i_{f5} = 3$ ⇒ $V_{CTAT} = V_T$

Let $\frac{dV_T}{dT} = -0.4\frac{\mathrm{mV}}{\mathrm{K}}, N = 3$ and equal V_{PTATi}

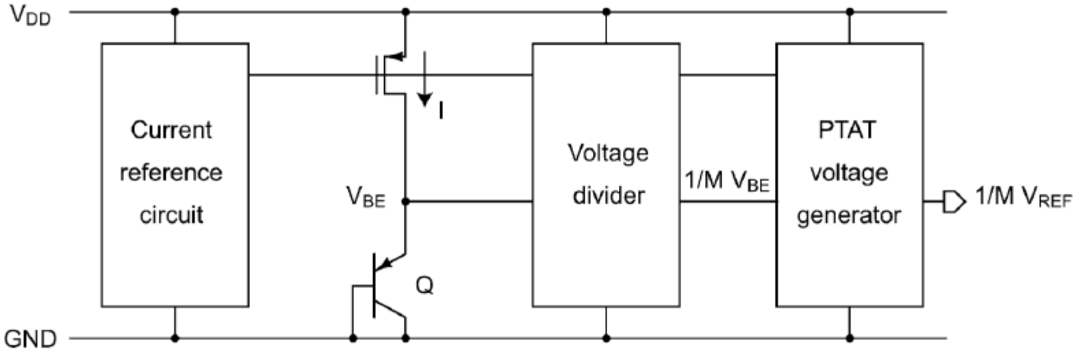
$$\boxed{\frac{dV_O}{dT} = 0 \rightarrow 3\frac{dV_{PTAT}}{dT} = -\frac{dV_{CTAT}}{dT}}$$

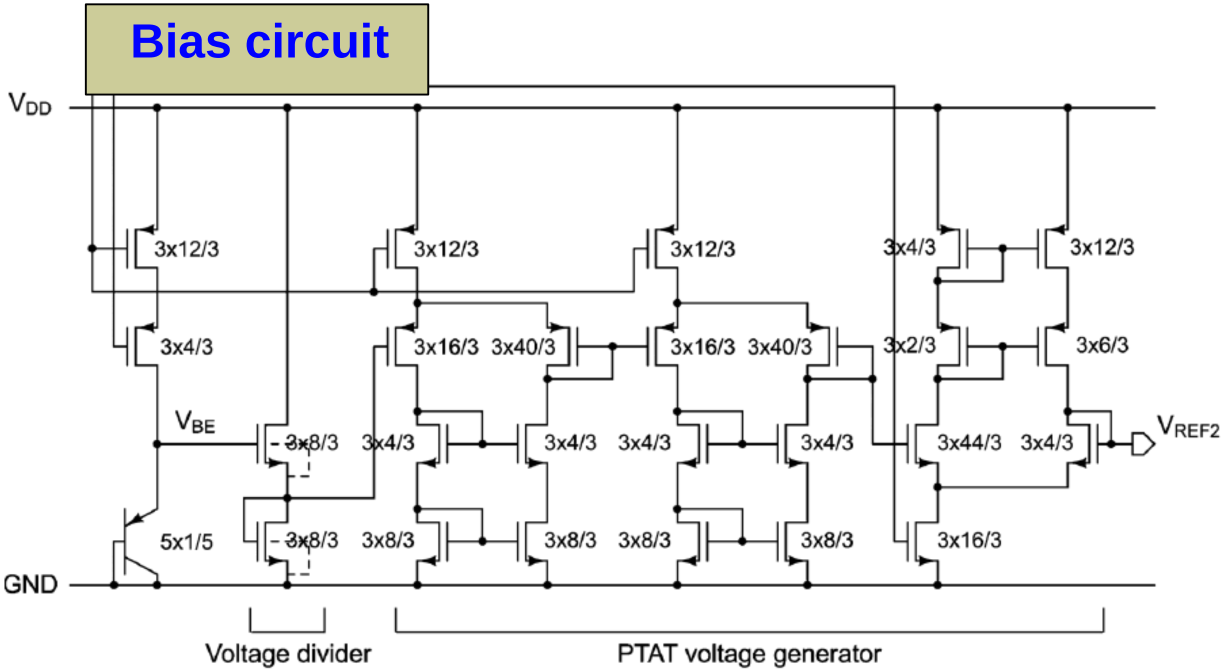
$$\boxed{\frac{dV_O}{dT} = 0 \rightarrow \frac{dV_{PTAT}}{dT} = 133\ \mu\mathrm{V/K}}$$

E. Vittoz and O. Neyroud, "A low-voltage CMOS bandgap reference," Solid-State Circuits, IEEE Journal of, vol. 14, no. 3, pp. 573–579, 1979.

6. The Unified Current Control Mode (UICM)

Circuit #3: Resistorless sub-bandgap voltage reference

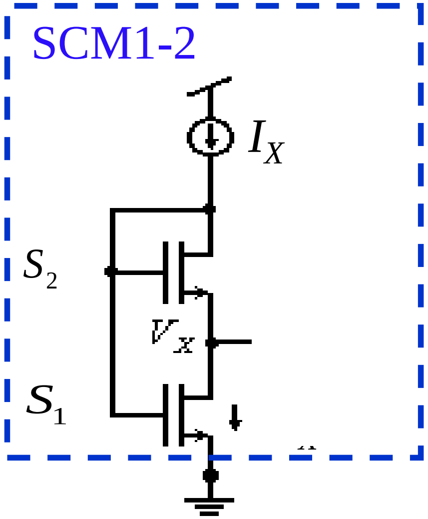


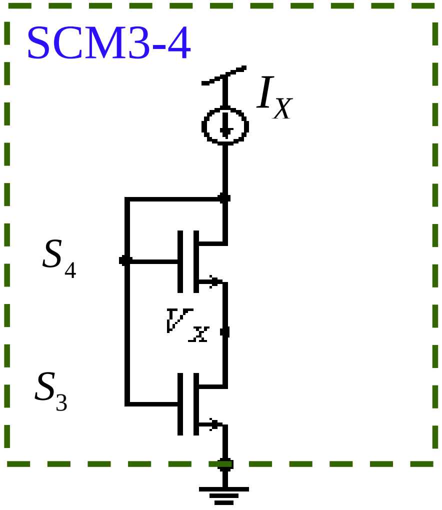

Bias circuit

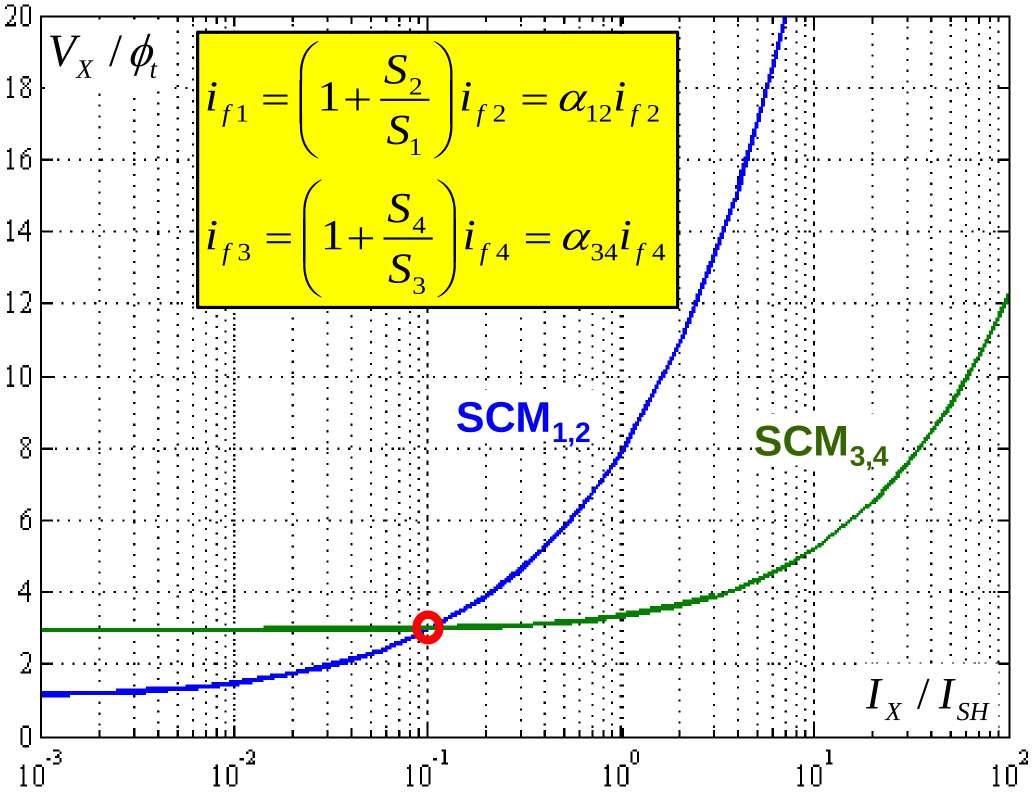
OSAKI *et al.*: 1.2-V SUPPLY, 100-NW, 1.09-V BANDGAP AND 0.7-V SUPPLY, 52.5-NW, 0.55-V SUB-BGR CIRCUITS FOR NANOWATT CMOS LSIs
IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 48, NO. 6, JUNE 2013

6. The Unified Current Control Mode (UICM)

Circuit #4: Self-Biased Current Source (SBCS)







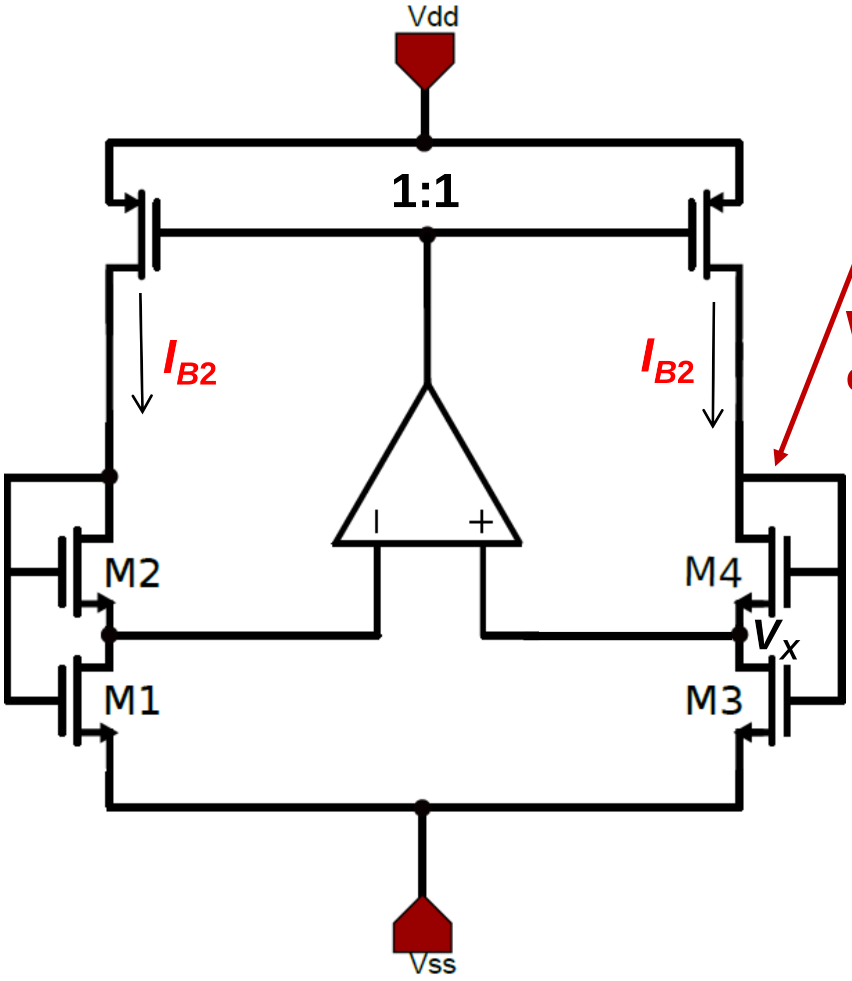
$$i_{f1} = \left(1 + \frac{S_2}{S_1}\right) i_{f2} = \alpha_{12} i_{f2}$$

$$i_{f3} = \left(1 + \frac{S_4}{S_3}\right) i_{f4} = \alpha_{34} i_{f4}$$

$$\frac{V_X}{\phi_t} = \sqrt{1 + \alpha \frac{I_X}{SI_{SH}}} - \sqrt{1 + \frac{I_X}{SI_{SH}}} + \ln\left(\frac{\sqrt{1 + \alpha \frac{I_X}{SI_{SH}}} - 1}{\sqrt{1 + \frac{I_X}{SI_{SH}}} - 1}\right)$$

6. The Unified Current Control Mode (UICM)

Circuit #4: Self-Biased Current Source (SBCS)



$$\ln\alpha_{34} = \sqrt{1+\alpha_{12}i_{f2}} - \sqrt{1+i_{f2}} + \ln\left(\frac{\sqrt{1+\alpha_{12}i_{f2}}-1}{\sqrt{1+i_{f2}}-1}\right);$$

$$\alpha_{12} = 1+\frac{S_2}{S_1} \qquad \alpha_{34} = 1+\frac{S_4}{S_3}$$

$$\frac{V_X}{\phi_t} \rightarrow \ln\alpha_{34}$$

Weak inversion operation of M3 & M4

i_{f2} (inversion level of M_2) is constant (it depends only on geometrical ratios α_{12} and α_{34})

The reference current $I_{B2} = I_{S2}i_{f2}$ is proportional to the specific current of M_2

- useful to bias transistors at constant inversion levels
- if mobility ~ T^{-1}, then I ~ I_{S2} is PTAT

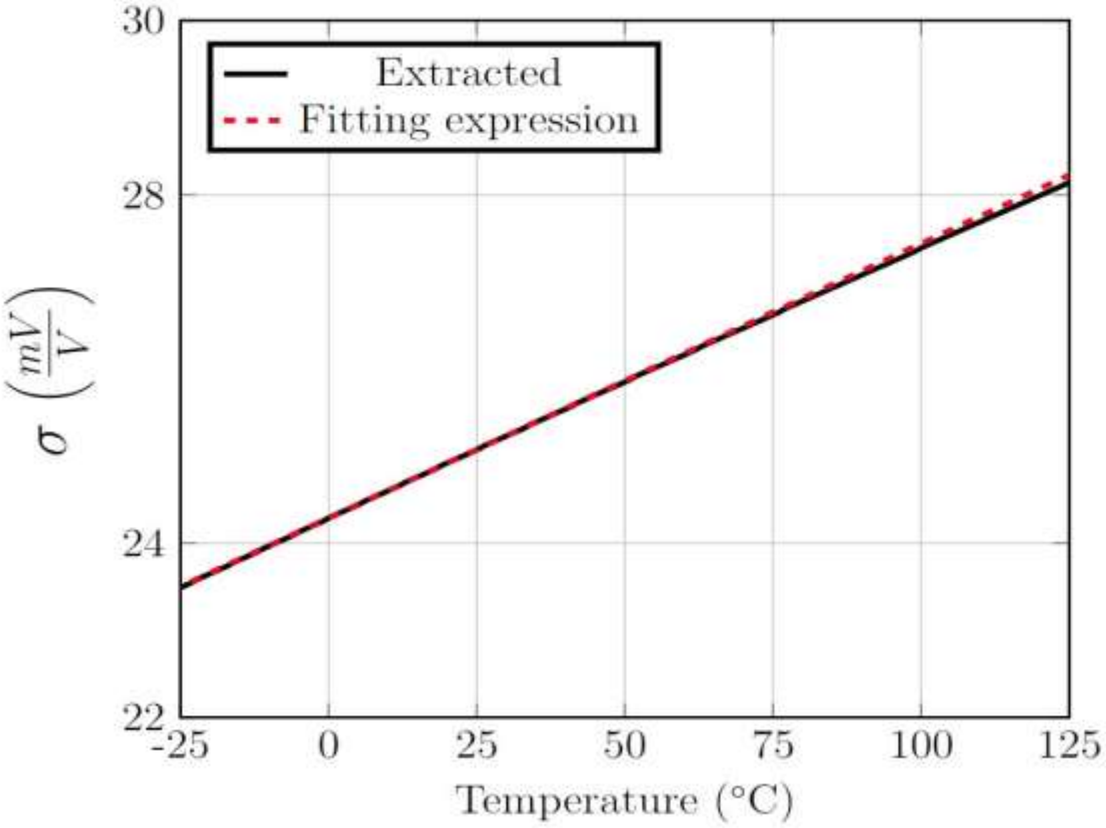
7. Drain-Induced Barrier Lowering (DIBL)

Increase in the drain/source voltage → **reduction in the potential barrier seen by the carriers at the source/drain.**

Inclusion of the DIBL effect → **generally through the threshold voltage.**

$$V_T \cong V_{T0} - \sigma(V_{SB} + V_{DB})$$

$$V_P \cong \frac{V_{GB} - [V_{T0} - \sigma(V_{SB} + V_{DB})]}{n}$$



Lima - September 2024

8. The 4-PM of the ACM model

0.18 um CMOS technology

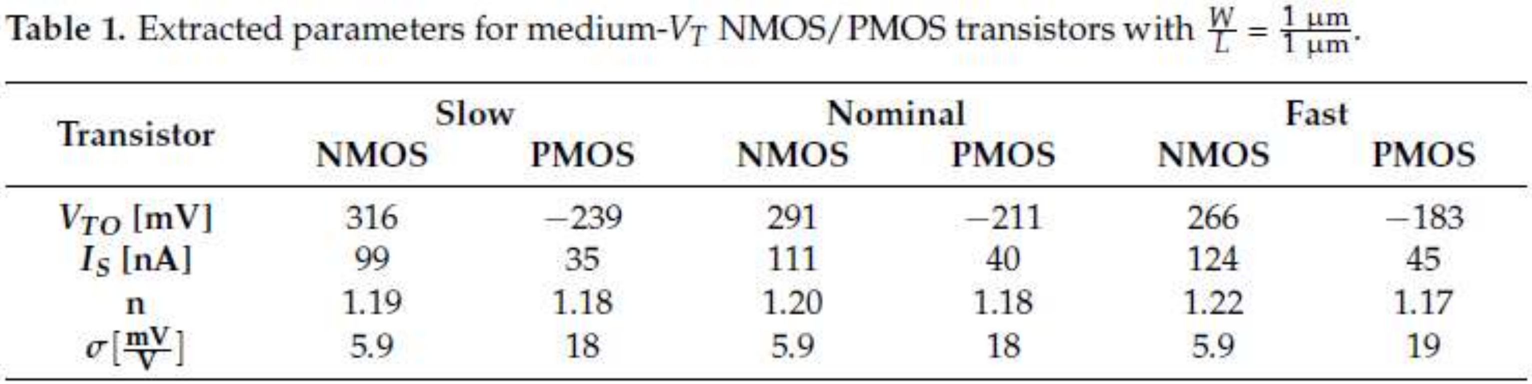


Table 1. Extracted parameters for medium-V_T NMOS/PMOS transistors with $\frac{W}{L} = \frac{1\ \mu m}{1\ \mu m}$.

Transistor	Slow		Nominal		Fast	
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
V_{TO} [mV]	316	−239	291	−211	266	−183
I_S [nA]	99	35	111	40	124	45
n	1.19	1.18	1.20	1.18	1.22	1.17
$\sigma [\frac{mV}{V}]$	5.9	18	5.9	18	5.9	19

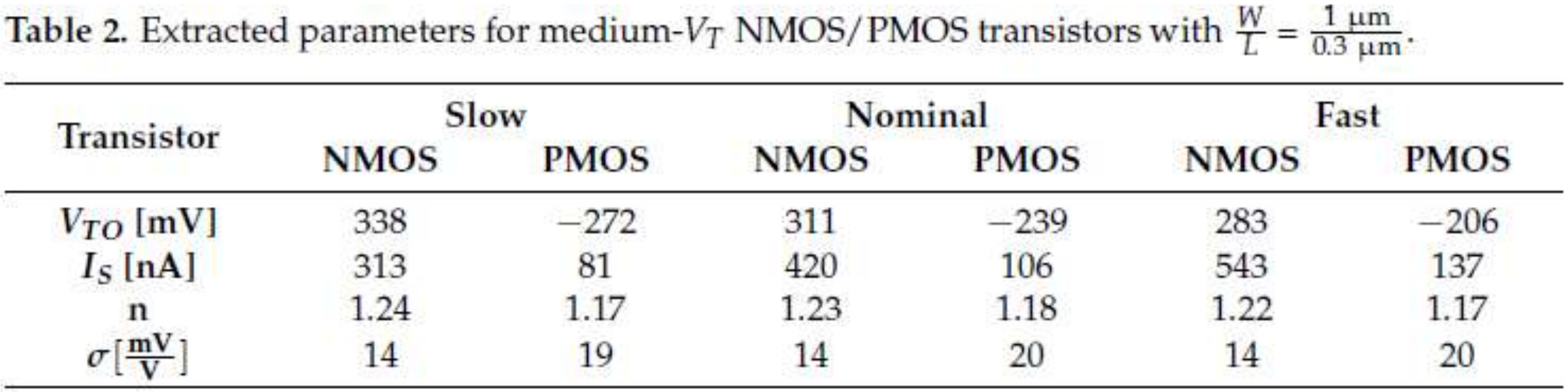


Table 2. Extracted parameters for medium-V_T NMOS/PMOS transistors with $\frac{W}{L} = \frac{1\ \mu m}{0.3\ \mu m}$.

Transistor	Slow		Nominal		Fast	
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
V_{TO} [mV]	338	−272	311	−239	283	−206
I_S [nA]	313	81	420	106	543	137
n	1.24	1.17	1.23	1.18	1.22	1.17
$\sigma [\frac{mV}{V}]$	14	19	14	20	14	20

8. The 4-PM of the ACM model

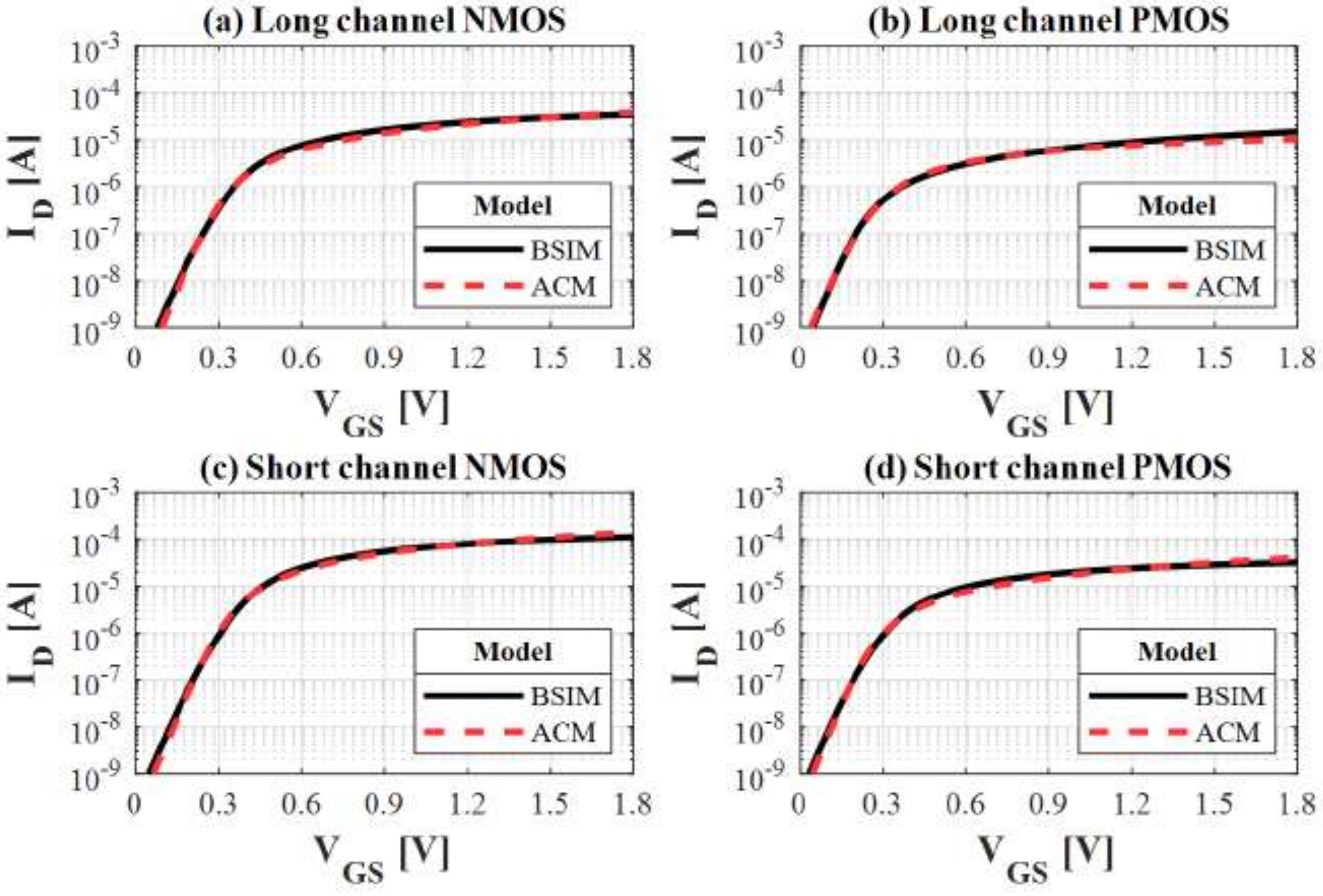


Figure 8. $I_D \times V_{GS}$ @ $V_{DS} = 200$ mV for (**a**) medium (nominal) V_T long-channel NMOS and (**b**) PMOS transistors and for (**c**) medium (nominal) V_T short-channel NMOS and (**d**) PMOS transistors.

8. The 4-PM of the ACM model

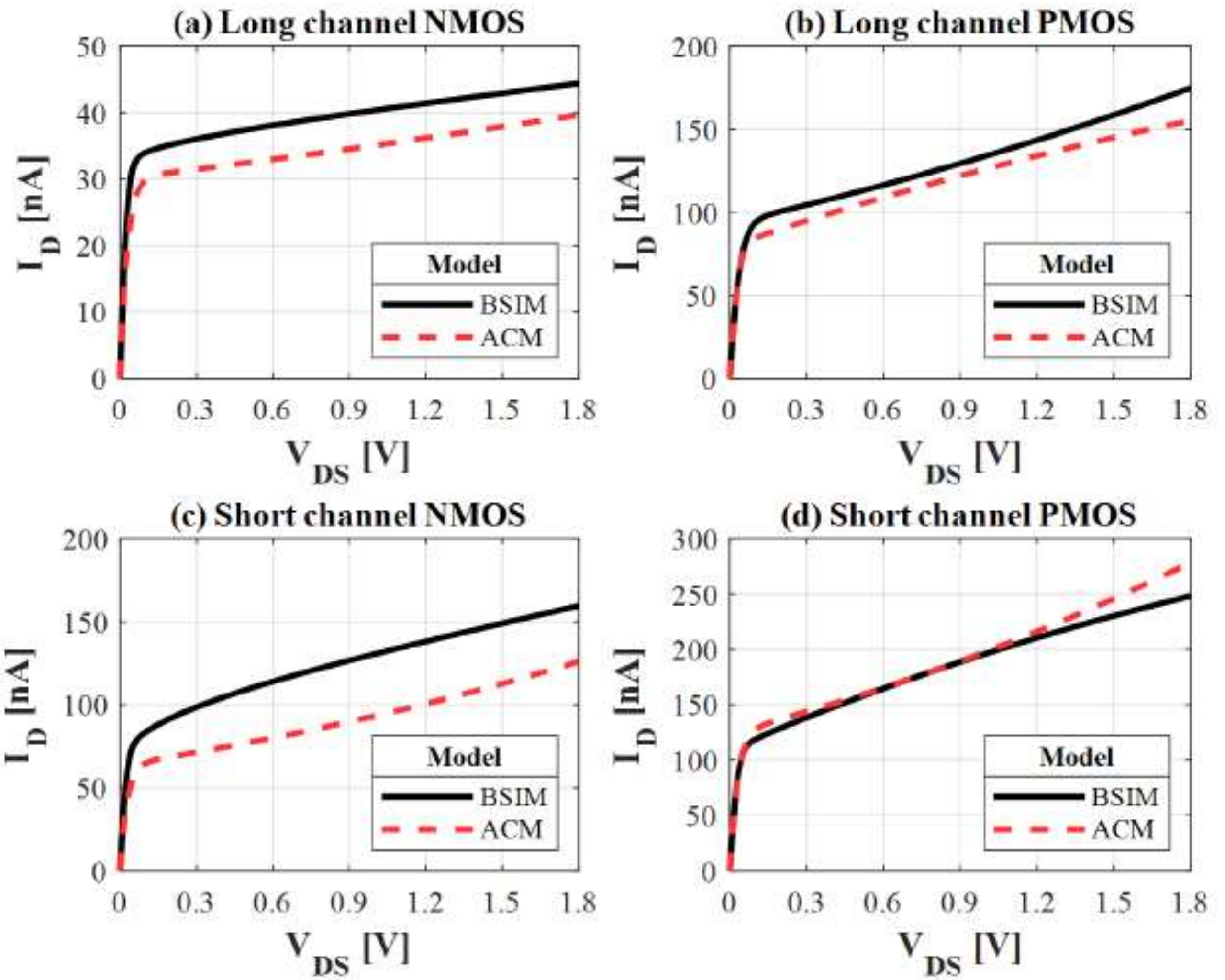


Figure 9. $I_D \times V_{DS}$ @ $V_{GS} = 200$ mV for (**a**) medium (nominal) V_T long-channel NMOS and (**b**) PMOS transistors and for (**c**) medium (nominal) V_T short-channel NMOS and (**d**) PMOS transistors.

8. The 4-PM of the ACM model

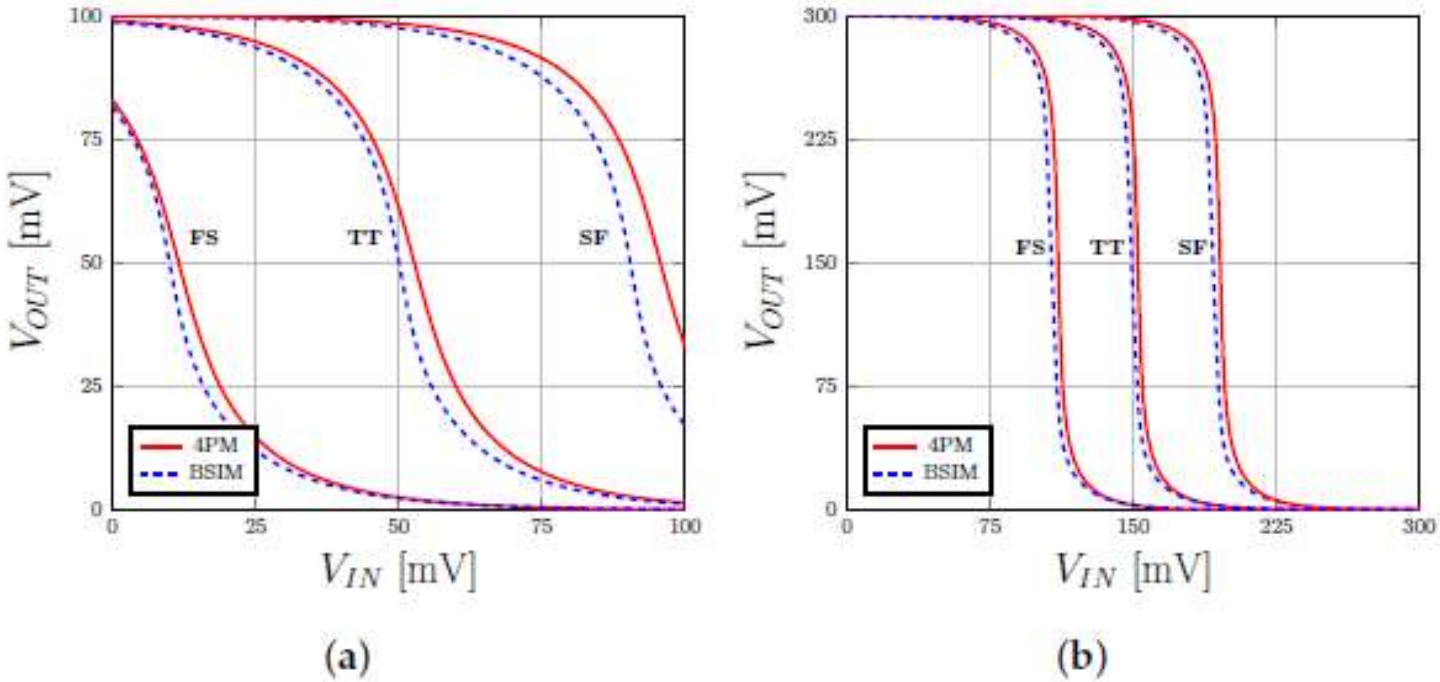


Figure 12. Voltage-transfer characteristics of the CMOS inverter using BSIM and the 4PM across the corners of process variation. (**a**) V_{DD} = 100 mV. (**b**) V_{DD} = 300 mV.

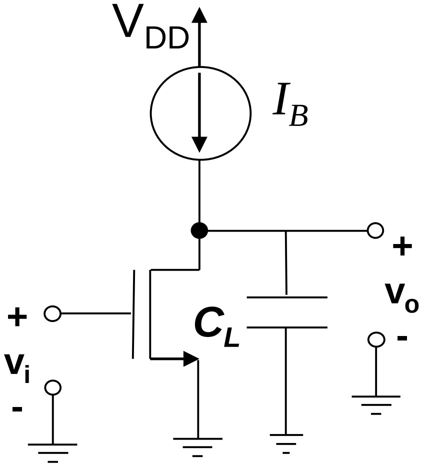
8. The 4-PM of the ACM model

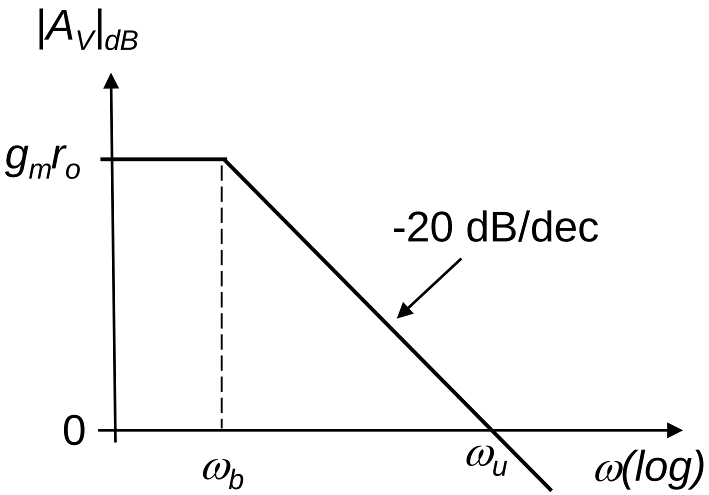
Circuit #5: Common-source amplifier – Sizing and biasing

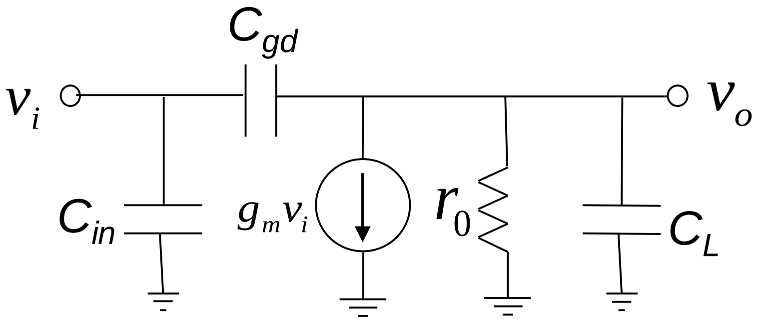
Input specs: gain-bandwidth product (GB), load capacitance (C_L), fixed channel length (L)

Assumptions: ideal input voltage source, $C_{gd}=0$

$$\omega_u = 2\pi GB = g_m / C_L$$







$$g_m = \frac{2I_S}{n\phi_t}\left(\sqrt{1+\frac{I_B}{I_S}}-1\right)$$

$$I_S = I_{SH}(W/L)$$

How would you choose I_B and $I_S(W)$?

8. The 4-PM of the ACM model

Circuit #5: Common-source amplifier – Sizing and biasing

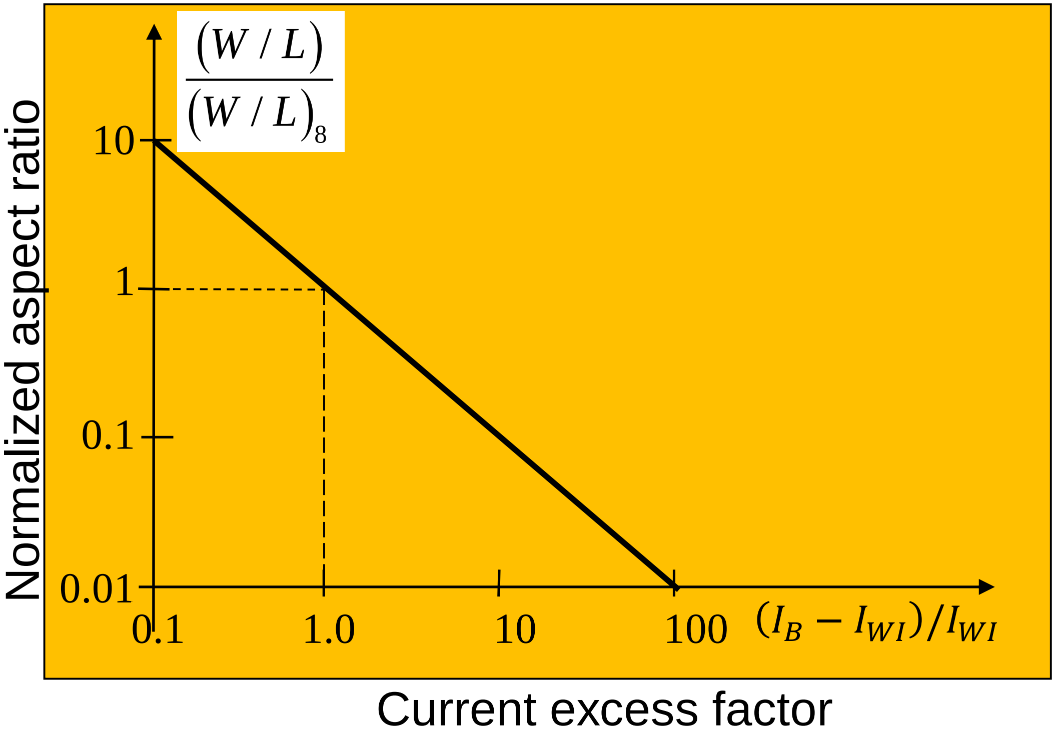
$$g_m = \frac{2I_S}{n\varphi_t}\left(\sqrt{1+\frac{I_B}{I_S}}-1\right) \xrightarrow{\textbf{WI}} \frac{I_B}{I_S} \ll \mathbf{1} \rightarrow g_m \cong \frac{I_{\boldsymbol{B}}}{n\varphi_t} \Longrightarrow I_{WI} = g_m n\phi_t = 2\pi GBC_L n\phi_t$$

Let us choose $(W/L)_{\boldsymbol{ref}} = (W/L)_{i_f=8} = (W/L)_8 \Longrightarrow g_m = \frac{2I_{S\boldsymbol{H}}(W/L)_8}{n\varphi_t}\left(\sqrt{1+8}-1\right)$

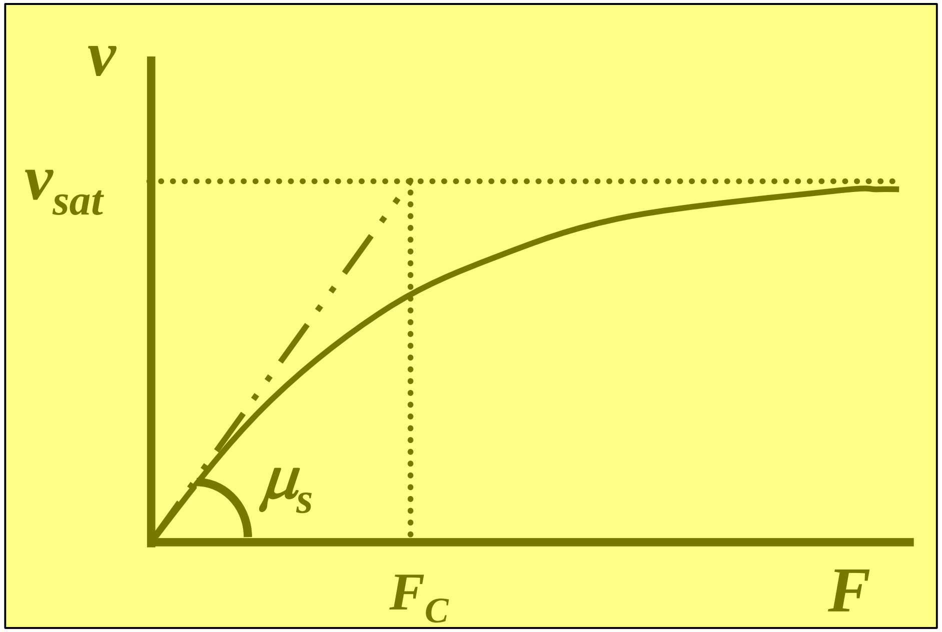
$$(W/L)_8 = (W/L)_{i_f=8} = \frac{g_m n\phi_t}{4I_{SH}} = \frac{g_m}{2\mu C'_{ox}\phi_t}$$

Power-area tradeoff

$$I_B = I_{WI}\left(1+\frac{(W/L)_8}{(W/L)}\right)$$



9. Velocity saturation



Carrier velocity vs. electric field

$$\boxed{\mu \cong \frac{\mu_s}{1+\frac{F}{F_C}}}$$

$$\frac{v_{sat}}{\mu_s} = F_C$$

F_C: critical longitudinal field

μ_s : low-field mobility

Approximation

$$\boxed{v = \mu F \cong \frac{\mu_s F}{1+\frac{F}{F_C}}}$$

allows analytical integration for I_D

9. Velocity saturation

$$i_D = \frac{I_D}{I_S} = (q_S + q_D + 2)(q_S - q_D)$$

for

low electric field $F << F_C$

or, equivalently

$$\zeta |q_S - q_D| << 1$$

$$i_D = \frac{(q_S + q_D + 2)(q_S - q_D)}{1 + \zeta |q_S - q_D|}$$

Mobility degradation due to longitudinal electric field

$$\zeta = \frac{(\mu_s \phi_t / L)}{v_{sat}}$$

: ratio of diffusion-related velocity to saturation velocity

9. Velocity saturation

Saturation current due to velocity saturation of the carriers

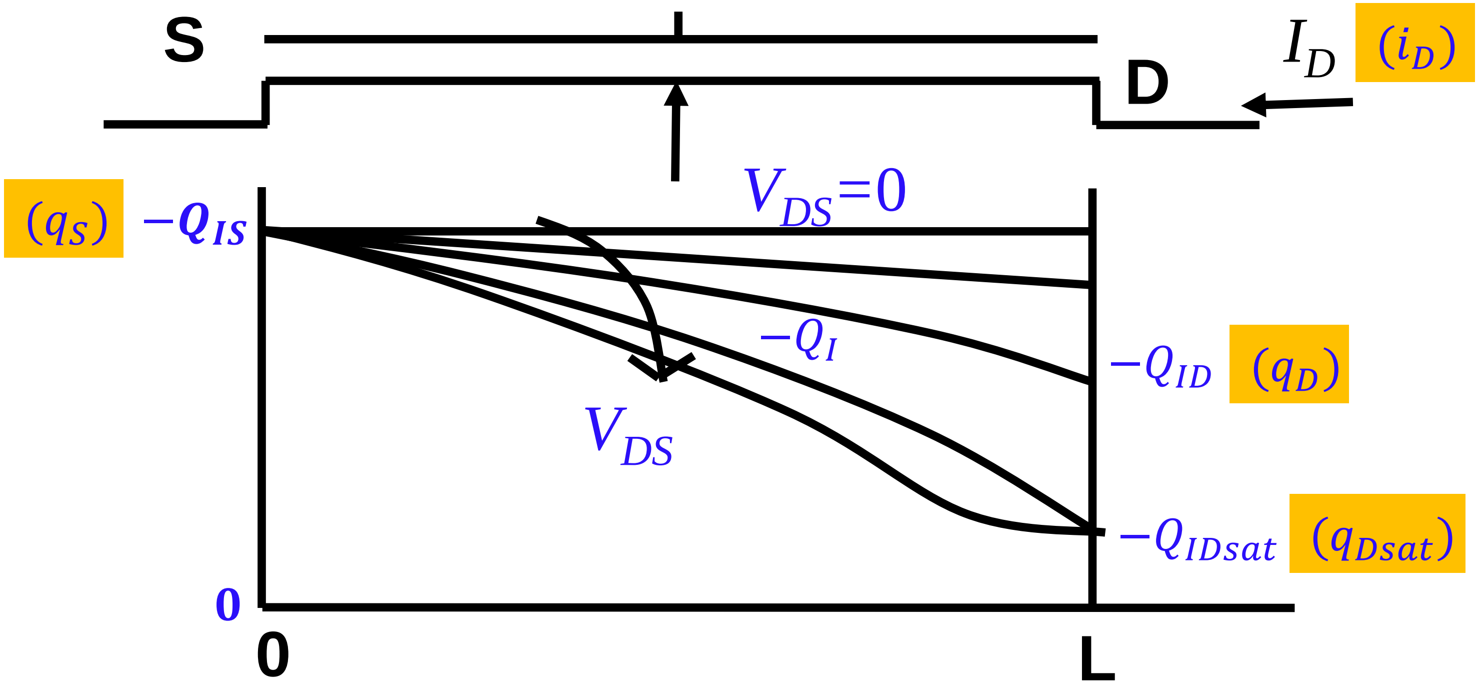
$$\boxed{I_{Dsat} = -WQ_{IDsat}v_{sat}}$$

The minimum amount of (electron) charge flowing at the saturation velocity, required to sustain the current:

$$\boxed{Q_{IDsat} = -I_{Dsat}/Wv_{sat}}$$

Normalized variables

$$\boxed{i_{Dsat} = \frac{2}{\zeta}q_{dsat}}$$

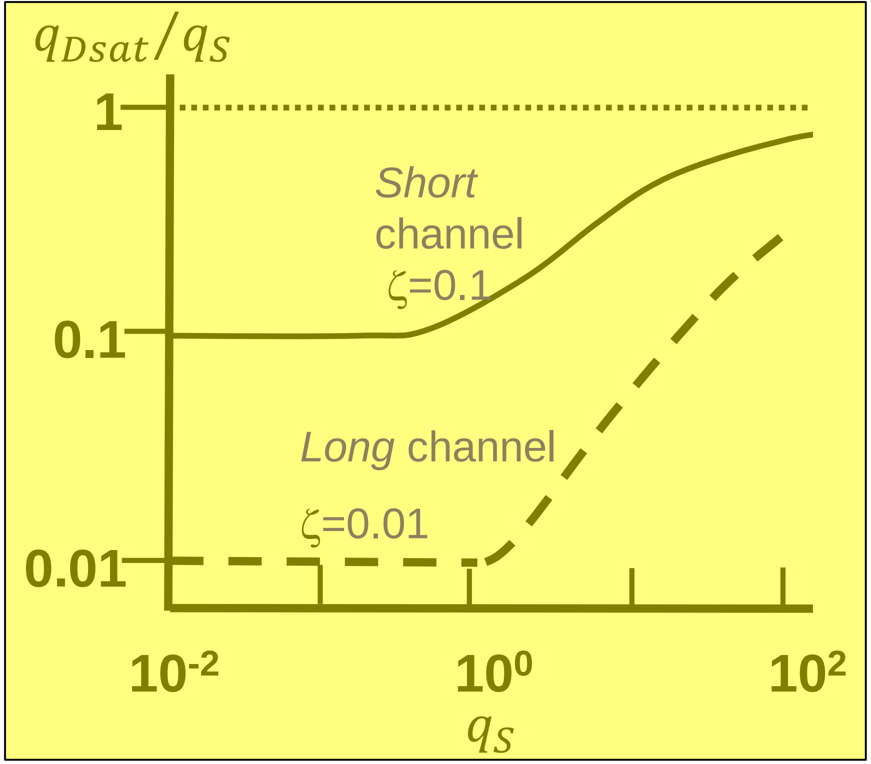


9. Velocity saturation

$$i_{Dsat} = \frac{(q_S + q_{Dsat} + 2)}{1 + \zeta(q_S - q_{Dsat})}(q_S - q_{Dsat})$$

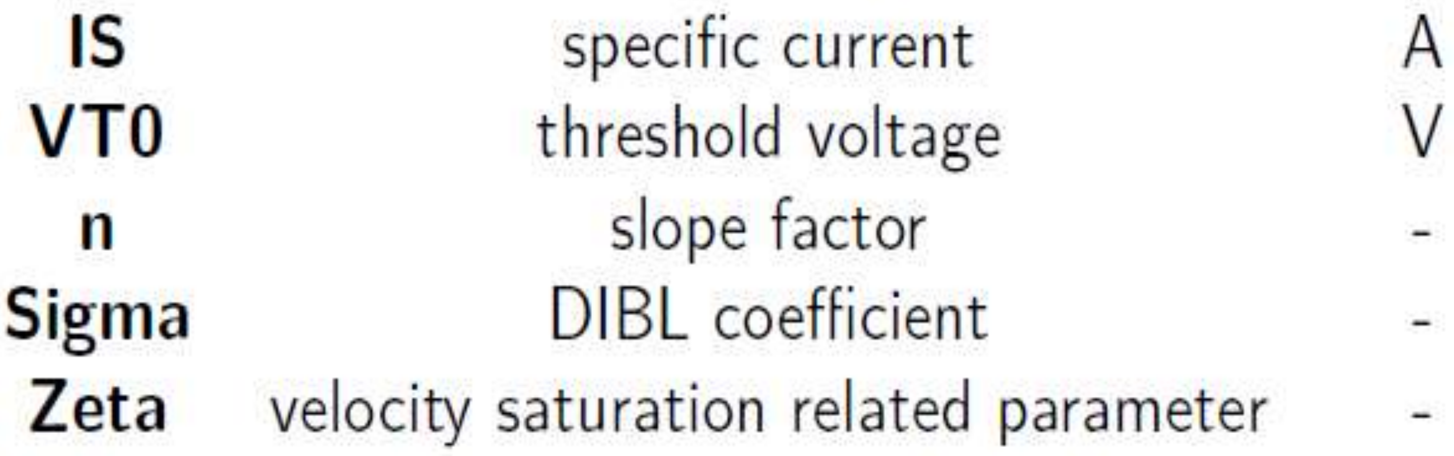
$$i_{Dsat} = \frac{2}{\zeta} q_{dsat}$$

$$q_{Dsat} = q_s + 1 + \frac{1}{\zeta} - \sqrt{\left(1 + \frac{1}{\zeta}\right)^2 + \frac{2q_S}{\zeta}}$$



10. The 5-PM of the ACM model

5 DC parameters of the ACM model



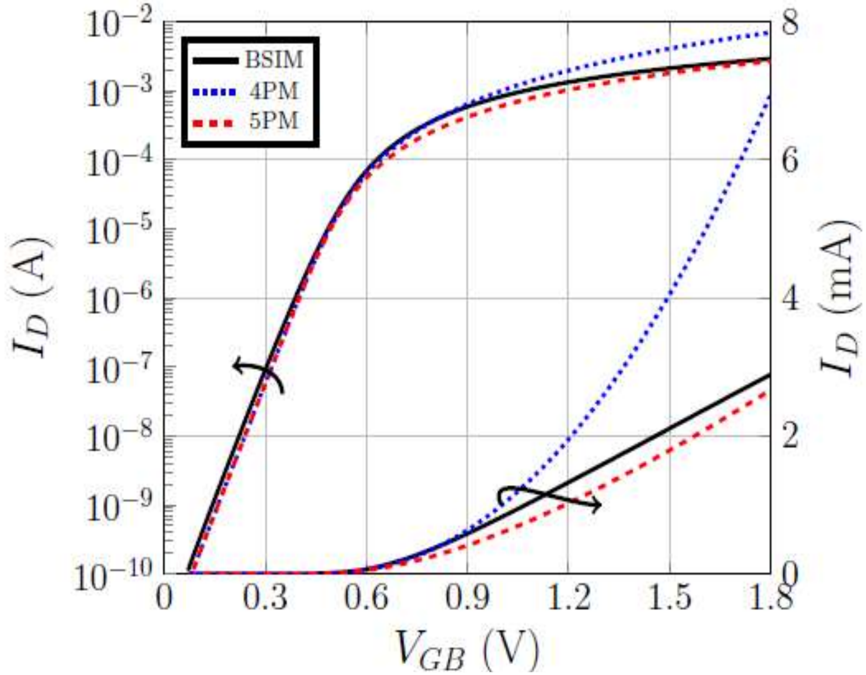
I_S	IS	specific current	A
V_{T0}	VT0	threshold voltage	V
n	n	slope factor	-
σ	Sigma	DIBL coefficient	- (mV/V)
ζ	Zeta	velocity saturation related parameter	-

Modified UCCM for inclusion of saturation velocity

$$\frac{V_P - V_{SB}}{\varphi_t} = q_S - 1 + \ln q_S$$

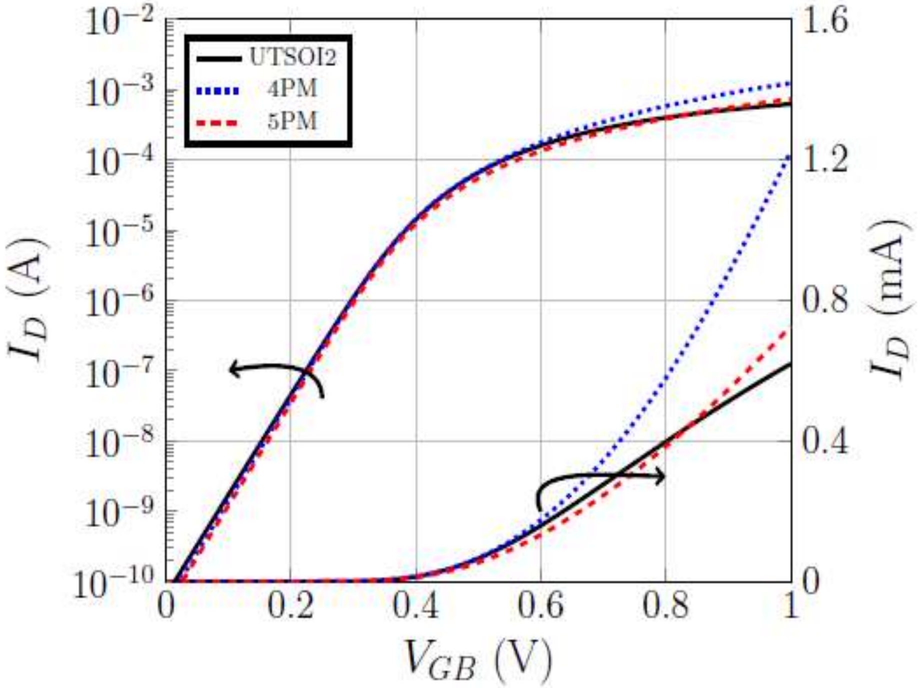
$$\frac{V_{DS}}{\varphi_t} = q_S - q_D + \ln\left[\frac{q_S - q_{Dsat}}{q_D - q_{Dsat}}\right]$$

10. The 5-PM of the ACM model



$I_D \times V_{GB}$ at $V_{GB} = V_{DB}$ of the SVT n-channel MOSFET

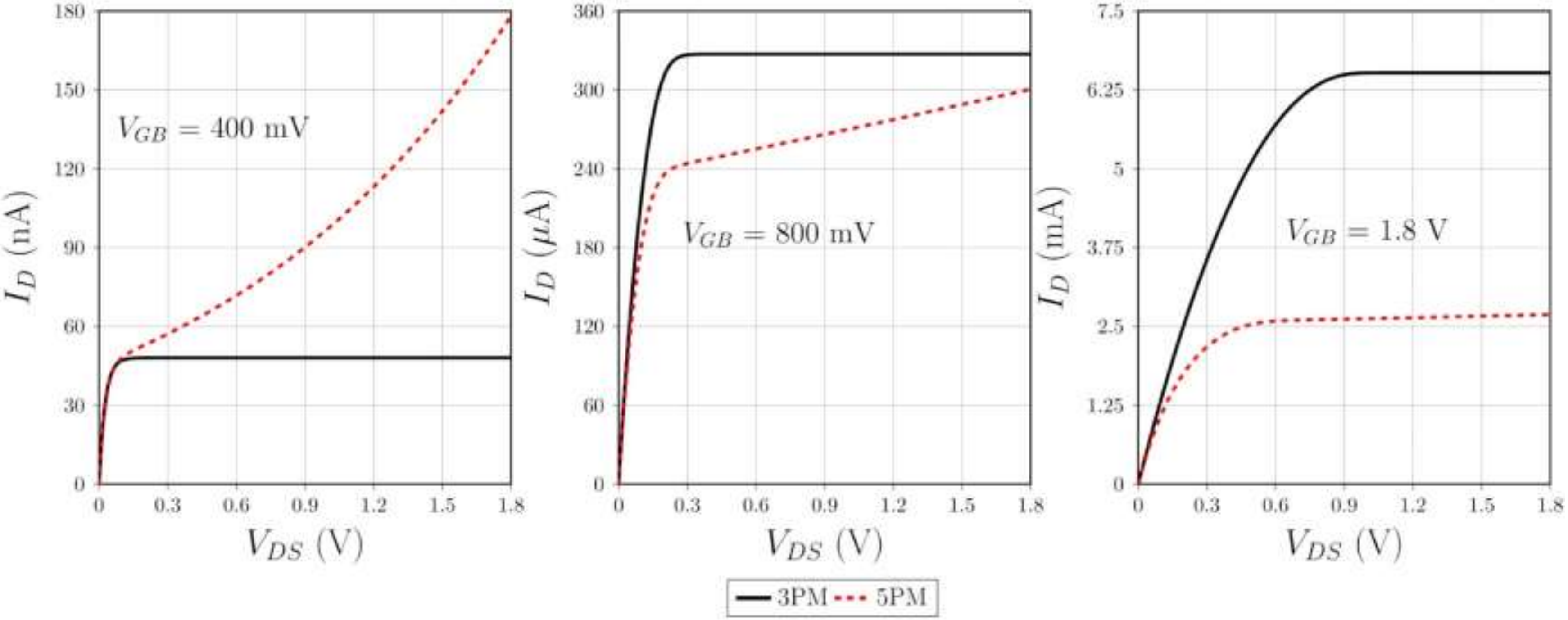
W/L = 5 μm/0.18 μm from a 0.18 μm CMOS process.



$I_D \times V_{GB}$ with V_{DS} = 500 mV of the LVT n-channel MOSFET

W/L = 1 μm/60 nm from a 28-nm FD-SOI

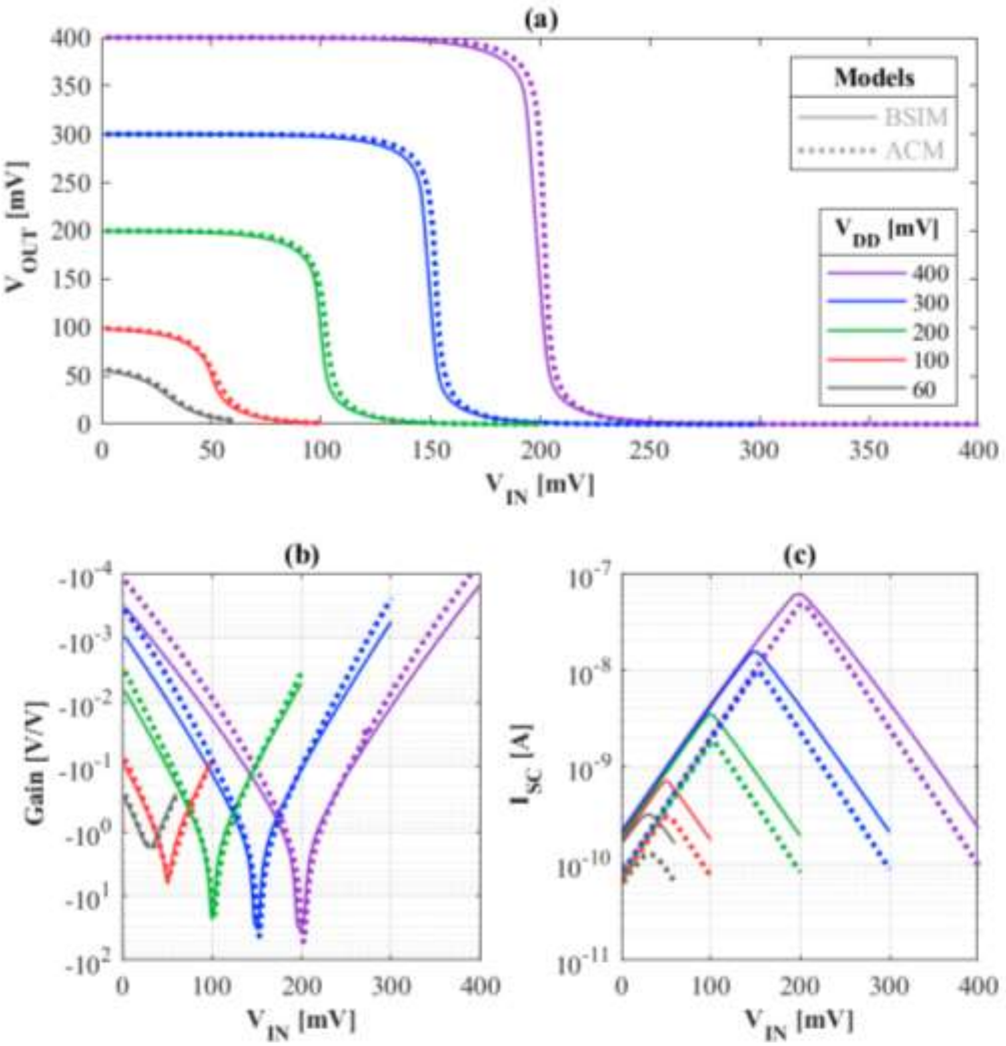
10. The 5-PM of the ACM model



DIBL model: $V_T = V_{T0} - \sigma(V_{SB} + V_{DB})$

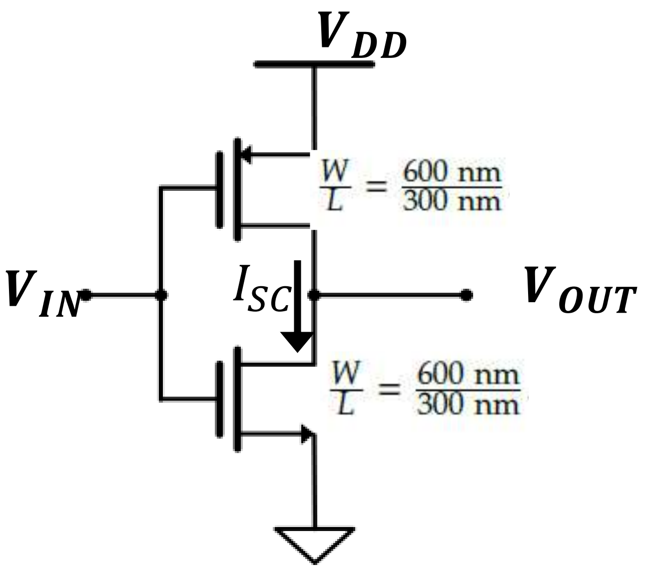
Transistor	W/L ($\mu m/\mu m$)	V_{T0} (mV)	I_S (μA)	n	σ	ζ
NMOS2V	$\mathbf{5/0.18}$	528	5.52	1.37	0.025	0.056

10. The 5-PM of the ACM model



CMOS inverter: (a) Voltage transfer characteristic (VTC), (b) small-signal gain and (c) short-circuit current for BSIM and ACM models

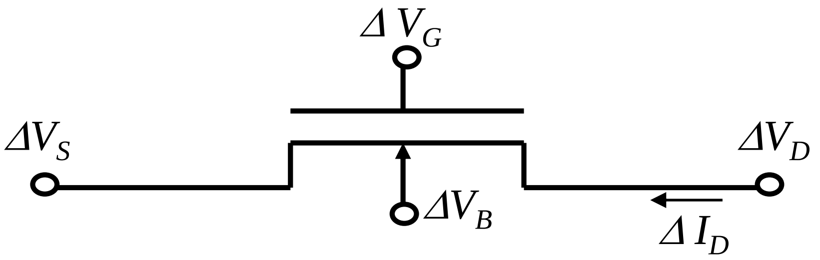
CMOS inverter



ACM 4-parameter model

Transistor	NMOS	PMOS
V_{TO} [mV]	309	–269
I_S [nA]	280	89
n	1.24	1.25
$\sigma\left[\frac{\text{mV}}{\text{V}}\right]$	15	23

11. Small-signal transconductances



$$\Delta I_D \cong g_{mg}\Delta V_G - g_{ms}\Delta V_S + g_{md}\Delta V_D + g_{mb}\Delta V_B \qquad g_{mg}=\frac{\partial I_D}{\partial V_G},\, g_{ms}=-\frac{\partial I_D}{\partial V_S},\, g_{md}=\frac{\partial I_D}{\partial V_D},\, g_{mb}=\frac{\partial I_D}{\partial V_B}$$

$$\Delta I_D = 0 \text{ if } \Delta V_G=\Delta V_S=\Delta V_D=\Delta V_B \Rightarrow g_{mg}-g_{ms}+g_{md}+g_{mb}=0$$

Calculation of g_{ms} (long-channel)

$$\boxed{g_{ms} = -\frac{\partial(I_F-I_R)}{\partial V_S} = -\frac{\partial I_F}{\partial V_S} = -I_S\frac{\partial i_f}{\partial V_S} = -\mu\frac{W}{L}Q_{IS}}$$

Symmetry

Calculation of g_{md} (long-channel)

$$\boxed{g_{md} = \frac{\partial(I_F-I_R)}{\partial V_D} = -\frac{\partial I_R}{\partial V_D} = -\mu\frac{W}{L}Q_{ID}}$$

$$g_{mg} \cong I_S\frac{\partial(i_f-i_r)}{\partial V_G} \Rightarrow \begin{cases} \dfrac{\partial i_f}{\partial V_G} = -\dfrac{\partial i_f}{n\partial V_S} \\ \dfrac{\partial i_r}{\partial V_G} = -\dfrac{\partial i_r}{n\partial V_D} \end{cases} \Rightarrow \boxed{g_{mg} = g_m = \frac{g_{ms}-g_{md}}{n}}$$

$$g_m = \frac{g_{ms}}{n}$$ → in saturation

Since $g_{mg}-g_{ms}+g_{md}+g_{mb}=0 \Rightarrow \boxed{g_{mb}=(n-1)\,g_m}$

11. Small-signal transconductances

$$g_{ms(d)} = \frac{2I_S}{\phi_t}\left(\sqrt{1+i_{f(r)}}-1\right) = \frac{W}{L}\mu C_{ox} n\phi_t\left(\sqrt{1+i_{f(r)}}-1\right)$$

$$g_m = \frac{g_{ms}-g_{md}}{n} \qquad g_{mb} = (n-1)g_m$$

$$\boxed{\frac{g_m}{I_D} = \frac{2}{n\phi_t\left(\sqrt{1+i_f}+\sqrt{1+i_r}\right)}}$$

For V_{DS}/ϕ_t<<1 we have $i_f \cong i_r$

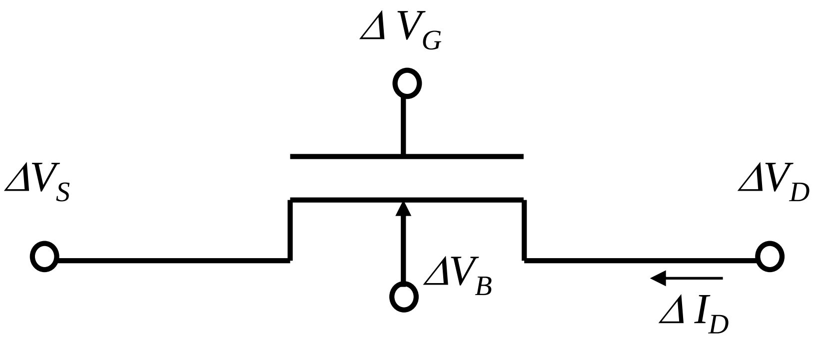
$$\boxed{\frac{g_m}{I_D} \cong \frac{1}{n\phi_t\sqrt{1+i_f}}}$$

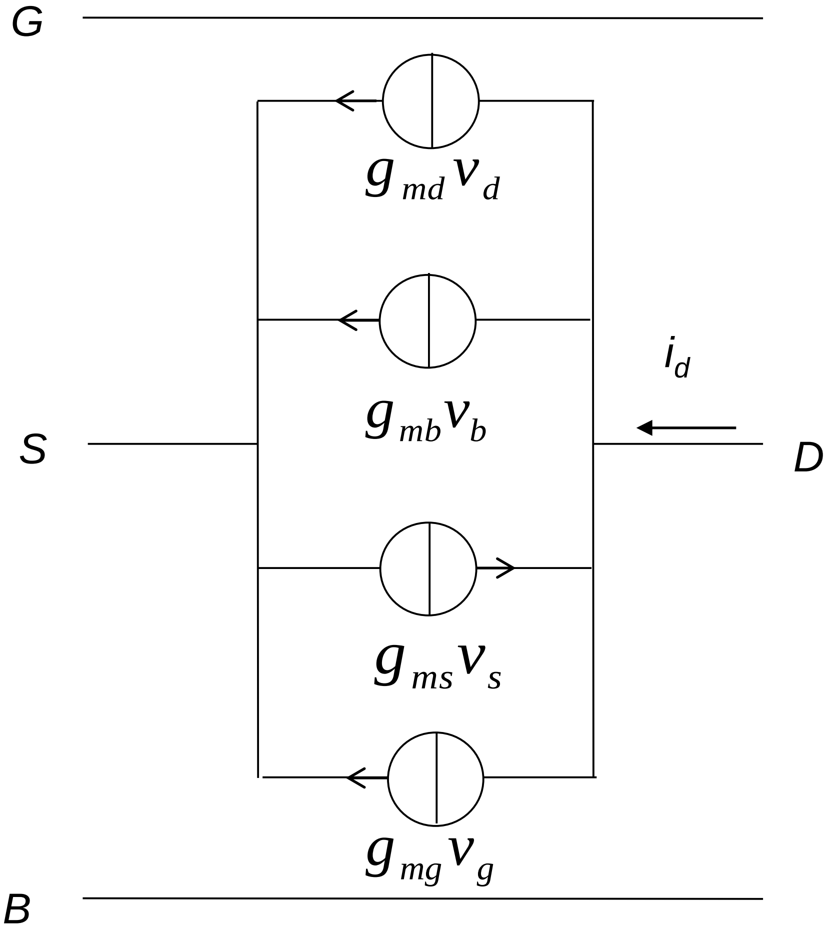
In saturation i_f>>i_r

$$\boxed{\frac{g_m}{I_D} \cong \frac{2}{n\phi_t\left(\sqrt{1+i_f}+1\right)}}$$

11. Small-signal transconductances

The low-frequency small-signal model





11. Small-signal transconductances

Low-frequency small-signal model in weak inversion

$$g_{md} = \sigma g_m + \frac{I_R}{\phi_t} \cong \frac{I_R}{\phi_t}$$

Triode

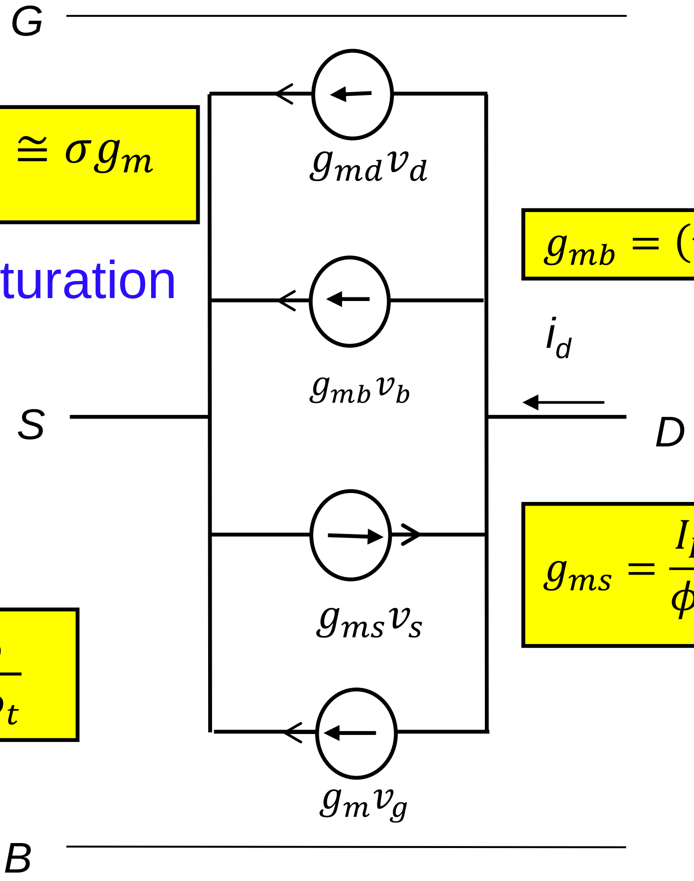
$$g_{md} \cong \sigma g_m$$

Saturation

$$g_{mb} = (n-1)\ g_m$$

$$g_{ms} = \frac{I_F}{\phi_t}$$

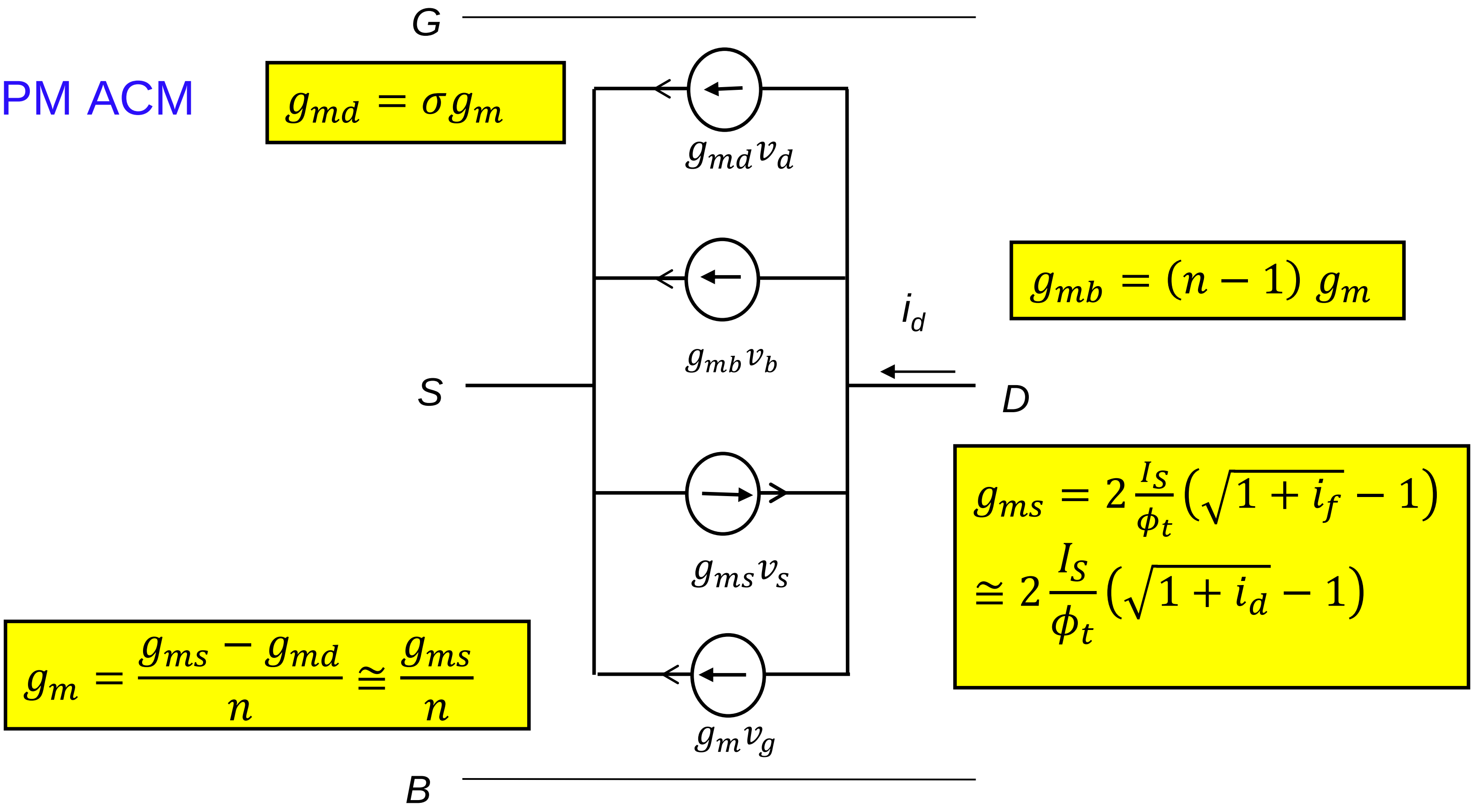
$$g_m = \frac{g_{ms} - g_{md}}{n} = \frac{I_D}{n\phi_t}$$



11. Small-signal transconductances

Low-frequency small-signal model in saturation

4-PM ACM



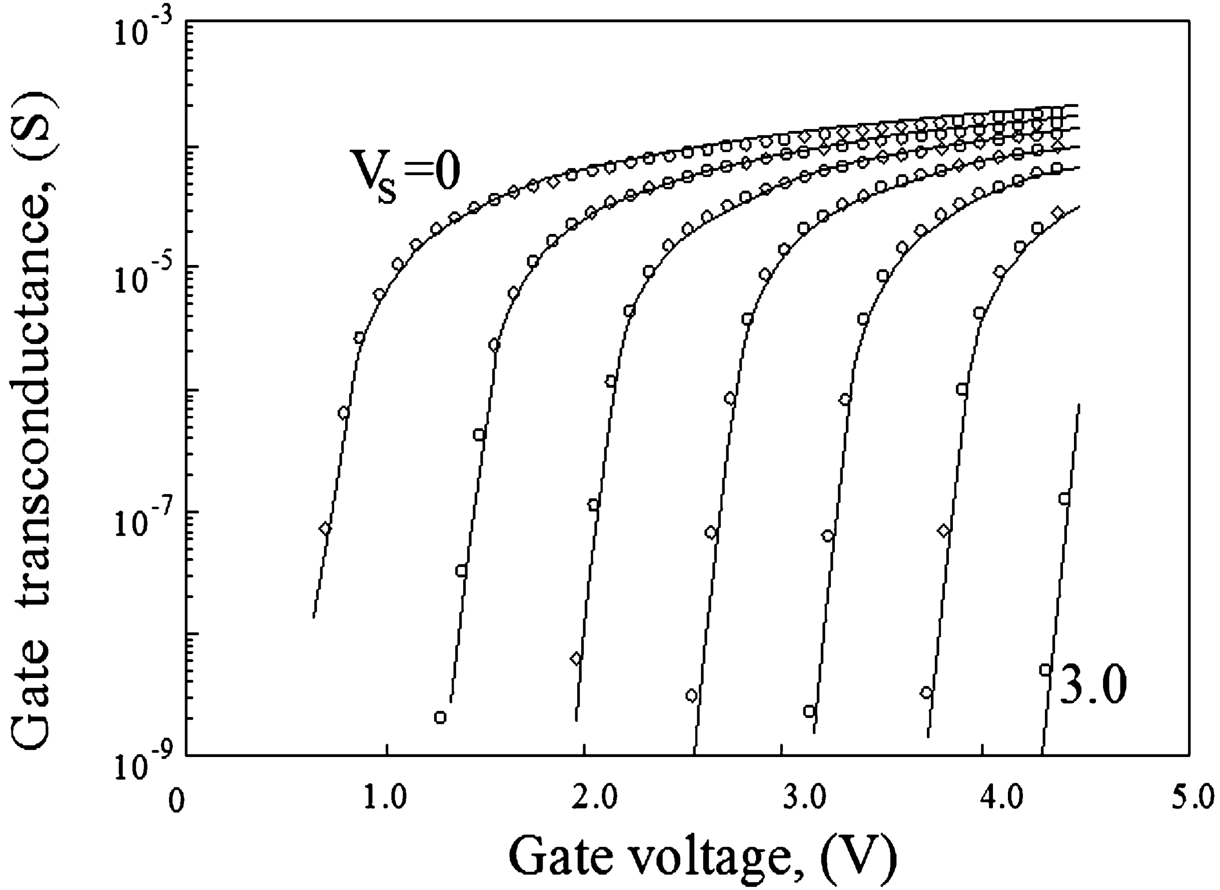
$$g_{md} = \sigma g_m$$

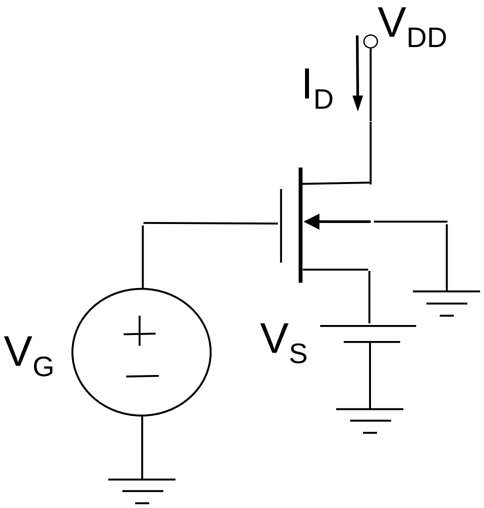
$$g_{mb} = (n-1)\, g_m$$

$$g_{ms} = 2\frac{I_S}{\phi_t}\left(\sqrt{1+i_f}-1\right) \cong 2\frac{I_S}{\phi_t}\left(\sqrt{1+i_d}-1\right)$$

$$g_m = \frac{g_{ms}-g_{md}}{n} \cong \frac{g_{ms}}{n}$$

10. Small-signal transconductances





Gate transconductance versus V_G for V_S= 0, 0.5, 1.0,1.5, 2.0, 2.5, and 3.0 V. W=L=25 µm, tox=280 Å, V_{DD}=5 V

WI: $g_m \sim exp(V_G/n\phi_t)$

SI: $g_m \sim V_G - V_T$

11. Small-signal transconductances

g_{ms}/I_F (in saturation)

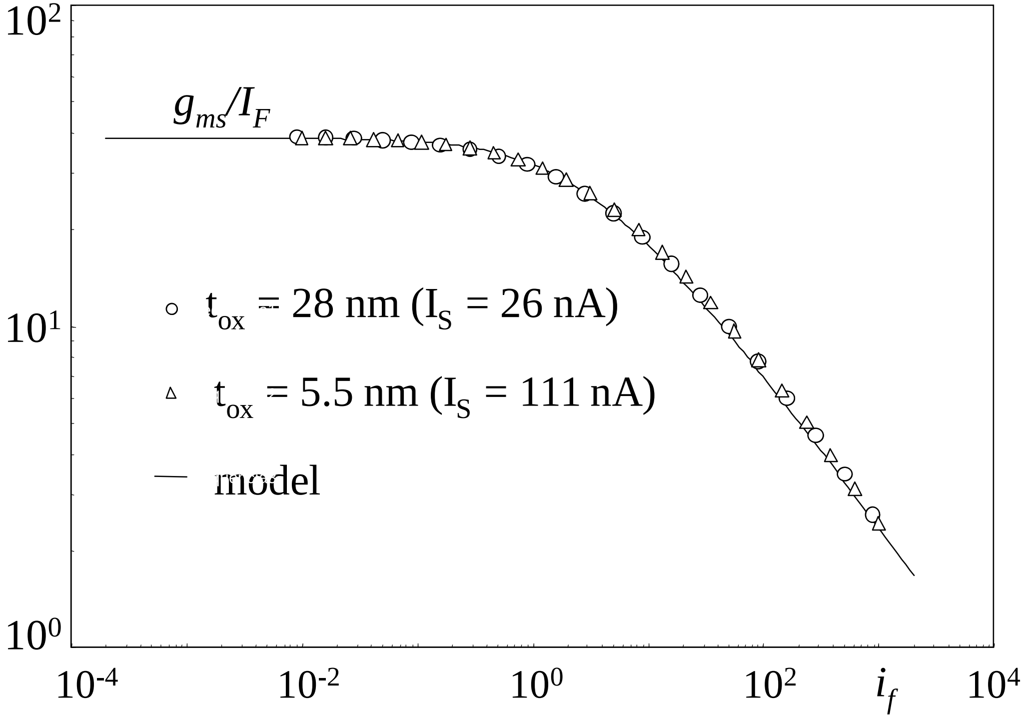
Transconductance -to-current ratio

$$\boxed{\frac{g_{ms}\phi_t}{I_F} = \frac{2}{\sqrt{1+i_f}+1} \cong \frac{2}{\sqrt{1+i_d}+1}}$$

$\cong 1 \longrightarrow$ WI ($i_f<1$)

$\cong \frac{2}{\sqrt{i_{f(r)}}} \longrightarrow$ SI ($i_f>>1$)

Saturation: $I_D = I_F$



W=25 μm

L=25 μm, t_{ox}= 280 Å

L=20 μm, t_{ox}= 55 Å

Long-channel MOSFET model at a glance

$$I_D = I_S\left[i_f - i_r\right]$$

$$I_S = \mu C_{ox} n \frac{\phi_t^2}{2}\frac{W}{L} = I_{SH}\frac{W}{L}$$

$$V_P - V_{S(D)} = \phi_t\left[\sqrt{1+i_{f(r)}} - 2 + \ln\left(\sqrt{1+i_{f(r)}} - 1\right)\right]$$

$$V_P \cong \frac{V_G - V_{T0}}{n}$$

$$g_{ms(d)} = \frac{2I_S}{\phi_t}\left(\sqrt{1+i_{f(r)}} - 1\right) = \frac{W}{L}\mu n C_{ox}\phi_t\left(\sqrt{1+i_{f(r)}} - 1\right)$$

$$g_m = \frac{g_{ms} - g_{md}}{n}$$

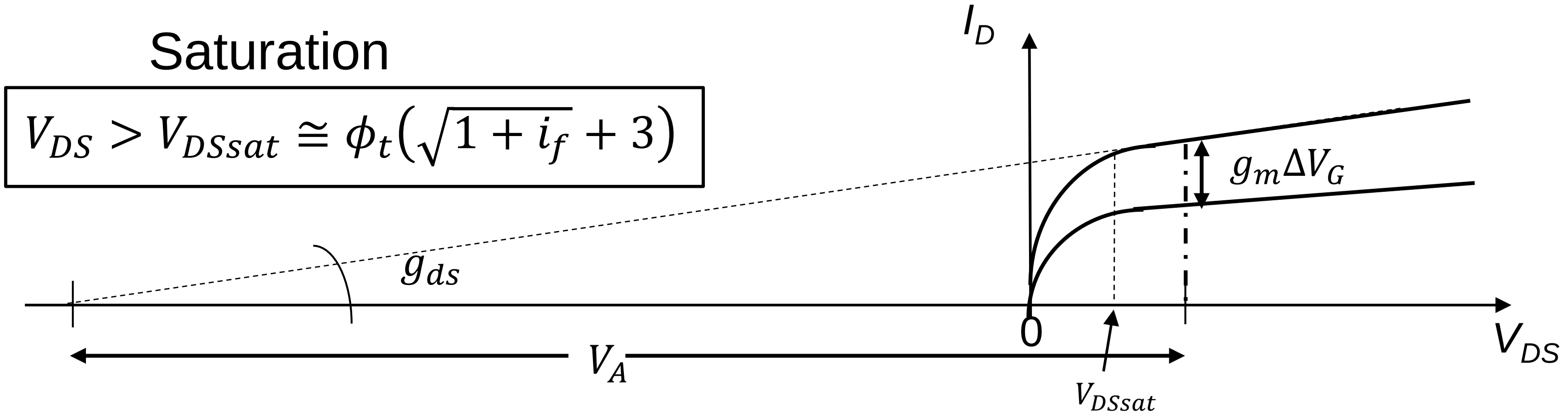
$$\frac{g_m}{I_D} = \frac{2}{n\phi_t\left(\sqrt{1+i_f} + \sqrt{1+i_r}\right)}$$

11. Small-signal transconductances

Output conductance in saturation

Saturation

$$\boxed{V_{DS} > V_{DSsat} \cong \phi_t\left(\sqrt{1+i_f}+3\right)}$$



Gate transconductance

$$\boxed{g_m = \frac{2I_S}{n\phi_t}\left(\sqrt{1+i_f}-1\right)}$$

Output conductance

$$\boxed{g_{ds} = g_{md} = \sigma g_m}$$

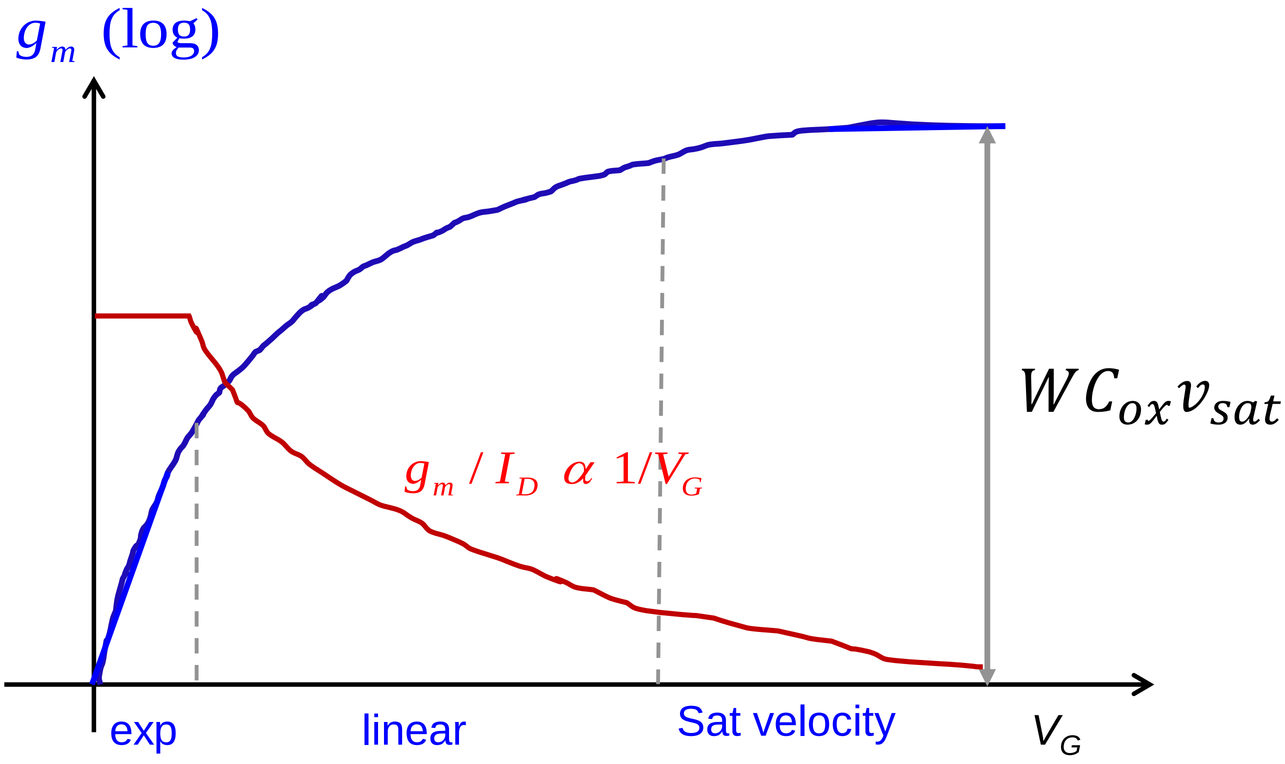
Relationship between Early voltage and DIBL parameter

$$g_{ds} = \sigma g_m = I_D/(V_A + V_{DS}) \quad \Rightarrow \quad \boxed{V_A + V_{DS} = \frac{I_D}{\sigma g_m}}$$

The Early voltage: independent of the current in WI and increases in SI

11. Small-signal transconductances

Gate transconductance in saturation



12. Quasi-static AC model

Quasi-static approximation: The charge stored in the transistor depends only on the **instantaneous** terminal voltages

The current entering each terminal of the transistor is split into a transport component (I_T) and a capacitive charging term.

$$\boxed{I_D(t) = I_T(t) + \frac{dQ_D}{dt}}$$

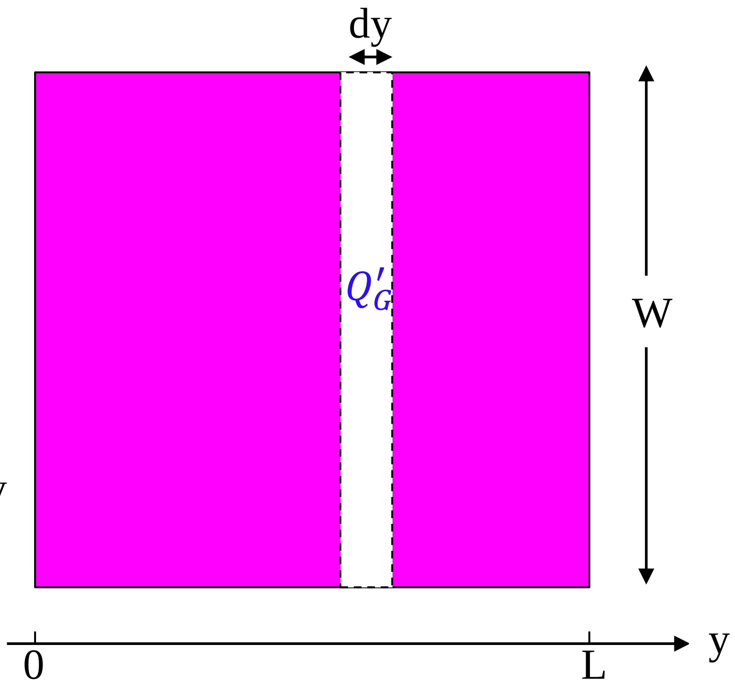
$$\boxed{I_T(t) = -\mu_n \frac{W}{L} \int_{V_S(t)}^{V_D(t)} Q_I(V_C)\, d\,V_C}$$

$$Q_G = W \int_0^L Q'_G dy$$

$$Q_B = W \int_0^L Q'_B dy$$

Q'_G Gate charge density

Q'_B Bulk charge density



Neglecting leakage currents

$$I_G(t) = \frac{dQ_G}{dt}$$

$$I_B(t) = \frac{dQ_B}{dt}$$

12. Quasi-static AC model

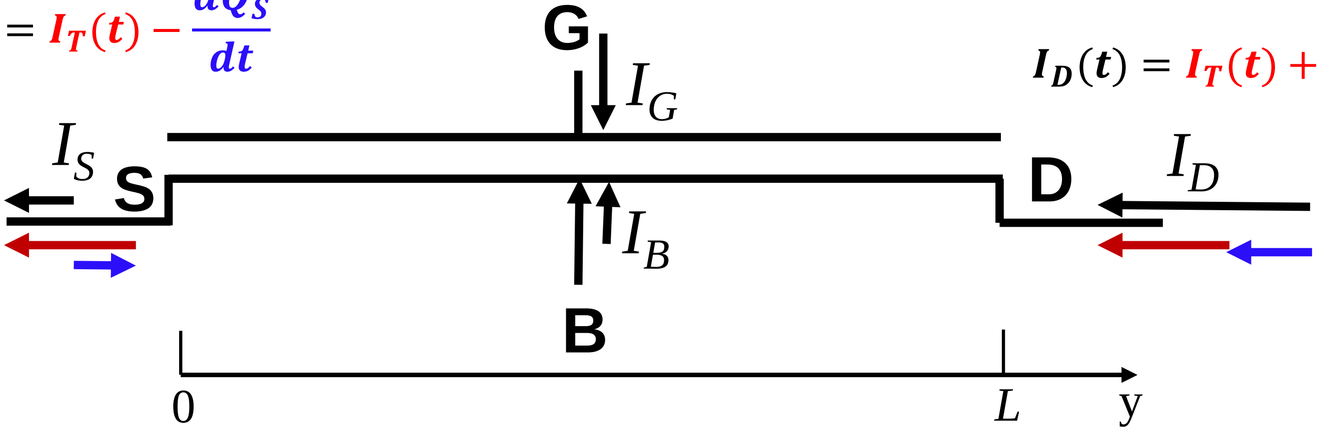
Ward-Dutton partition of the channel charge (based on charge conservation):

$$Q_S = W\int_0^L \left(1-\frac{y}{L}\right)Q_I dy$$

$$Q_D = W\int_0^L \frac{y}{L} Q_I dy$$

$$\boldsymbol{I_S(t) = I_T(t) - \frac{dQ_S}{dt}}$$

$$\boldsymbol{I_D(t) = I_T(t) + \frac{dQ_D}{dt}}$$



$$I_D(t) - I_S(t) = \frac{dQ_D}{dt} + \frac{dQ_S}{dt} = \frac{d[W\int_0^L Q_I dy]}{dt}$$

The variation of the charges that enter through drain and source equal the variation of the total **inversion charge stored** in the channel.

12. Quasi-static AC model

Once the four terminal charges $Q_D, Q_S, Q_{G,} Q_B$ are calculated, the device capacitances can be determined

The charge variation at each terminal is

$$\boxed{\frac{dQ_j}{dt} = \frac{\partial Q_j}{\partial V_G}\frac{dV_G}{dt} + \frac{\partial Q_j}{\partial V_S}\frac{dV_S}{dt} + \frac{\partial Q_j}{\partial V_D}\frac{dV_D}{dt} + \frac{\partial Q_j}{\partial V_B}\frac{dV_B}{dt}}$$

Defining $C_{jk} = -\left.\frac{\partial Q_j}{\partial V_k}\right|_0 \qquad j \neq k \qquad C_{jj} = \left.\frac{\partial Q_j}{\partial V_j}\right|_0$

$$\begin{pmatrix} dQ_G/dt \\ dQ_S/dt \\ dQ_D/dt \\ dQ_B/dt \end{pmatrix} = \begin{pmatrix} C_{gg} & -C_{gs} & -C_{gd} & -C_{gb} \\ -C_{sg} & C_{ss} & -C_{sd} & -C_{sb} \\ -C_{dg} & -C_{ds} & C_{dd} & -C_{db} \\ -C_{bg} & -C_{bs} & -C_{bd} & C_{bb} \end{pmatrix} \begin{pmatrix} dV_G/dt \\ dV_S/dt \\ dV_D/dt \\ dV_B/dt \end{pmatrix}$$

Only **nine** out of the sixteen capacitive coefficients are linearly independent

12. Quasi-static AC model

For $V_G(t) = V_S(t) = V_D(t) = V_B(t) = V(t)$ → $\frac{dQ_G}{dt} = (C_{gg} - C_{gs} - C_{gd} - C_{gb})\frac{dV}{dt} = 0$

$$\boxed{C_{gg} = C_{gs} + C_{gd} + C_{gb}}$$

Similarly, for the source, drain, and bulk →

$$\boxed{\begin{aligned} C_{ss} &= C_{sg} + C_{sd} + C_{sb} \\ C_{dd} &= C_{dg} + C_{ds} + C_{db} \\ C_{bb} &= C_{bg} + C_{bs} + C_{bd} \end{aligned}}$$

For $\frac{dV_S}{dt} = \frac{dV_D}{dt} = \frac{dV_B}{dt} = 0$

$$\frac{dQ_G}{dt} = C_{gg}\frac{dV_G}{dt}, \quad \frac{dQ_S}{dt} = -C_{sg}\frac{dV_G}{dt},$$

$$\frac{dQ_D}{dt} = -C_{dg}\frac{dV_G}{dt}, \quad \frac{dQ_B}{dt} = -C_{bg}\frac{dV_G}{dt}$$

The sum of charging currents → $\frac{dQ_G}{dt} + \frac{dQ_S}{dt} + \frac{dQ_D}{dt} + \frac{dQ_B}{dt} = (C_{gg} - C_{sg} - C_{dg} - C_{bg})\frac{dV_G}{dt}$

Charge conservation $\frac{d(Q_G + Q_S + Q_D + Q_B)}{dt} = 0$ →

$$\boxed{C_{gg} = C_{sg} + C_{dg} + C_{bg}}$$

12. Quasi-static AC model

Only nine out of the sixteen capacitive coefficients are linearly independent

$$C_{gg} = C_{gs} + C_{gd} + C_{gb} = C_{sg} + C_{dg} + C_{bg}$$

$$C_{ss} = C_{sg} + C_{sd} + C_{sb} = C_{gs} + C_{ds} + C_{bs}$$

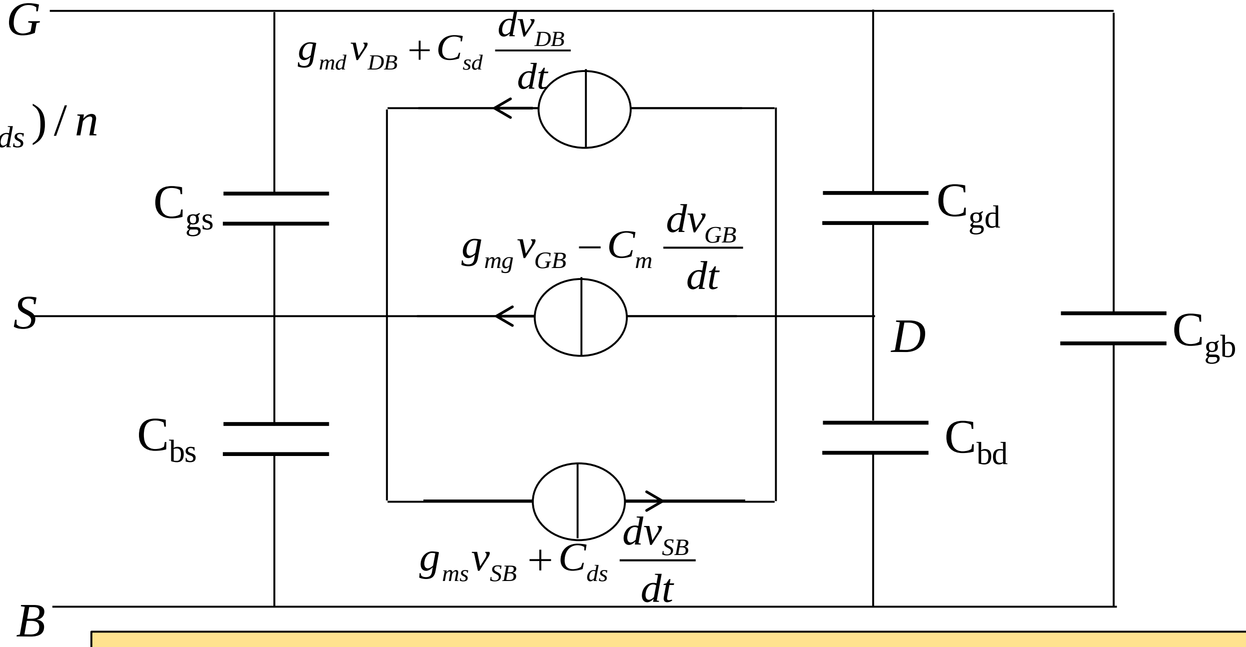
$$C_{dd} = C_{dg} + C_{ds} + C_{db} = C_{gd} + C_{sd} + C_{bd}$$

$$C_{bb} = C_{bg} + C_{bs} + C_{bd} = C_{gb} + C_{sb} + C_{db}$$

$$\begin{pmatrix} dQ_G / dt \\ dQ_S / dt \\ dQ_D / dt \\ dQ_B / dt \end{pmatrix} = \begin{pmatrix} C_{gg} & -C_{gs} & -C_{gd} & -C_{gb} \\ -C_{sg} & C_{ss} & -C_{sd} & -C_{sb} \\ -C_{dg} & -C_{ds} & C_{dd} & -C_{db} \\ -C_{bg} & -C_{bs} & -C_{bd} & C_{bb} \end{pmatrix} \begin{pmatrix} dV_G / dt \\ dV_S / dt \\ dV_D / dt \\ dV_B / dt \end{pmatrix}$$

12. Quasi-static AC model

$$C_{dg} - C_{gd} = C_m = (C_{sd} - C_{ds}) / n$$

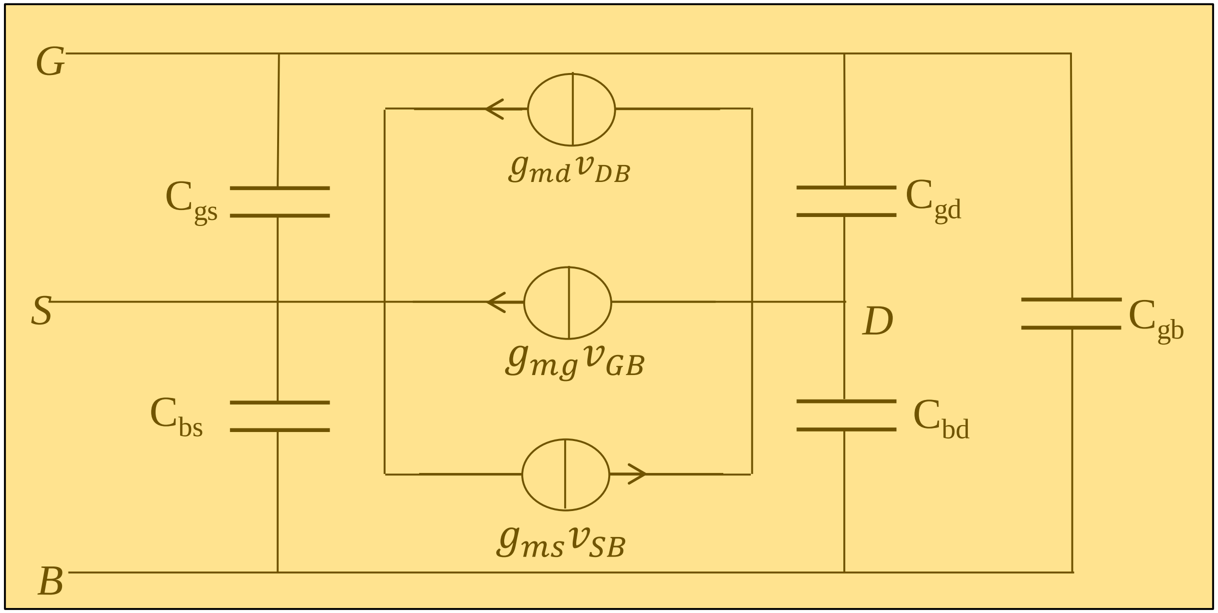


Simplified 5-capacitance small-signal equivalent circuit

$$\boxed{g_{md} \gg \omega C_{sd}}$$

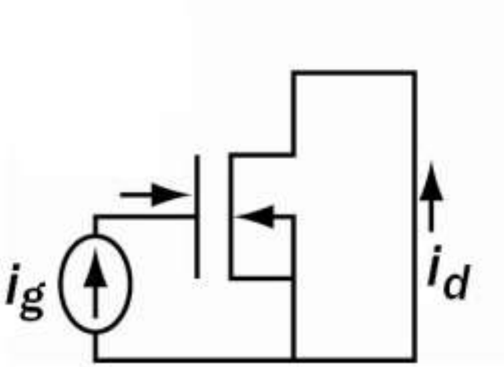
$$\boxed{g_{mg} \gg \omega C_m}$$

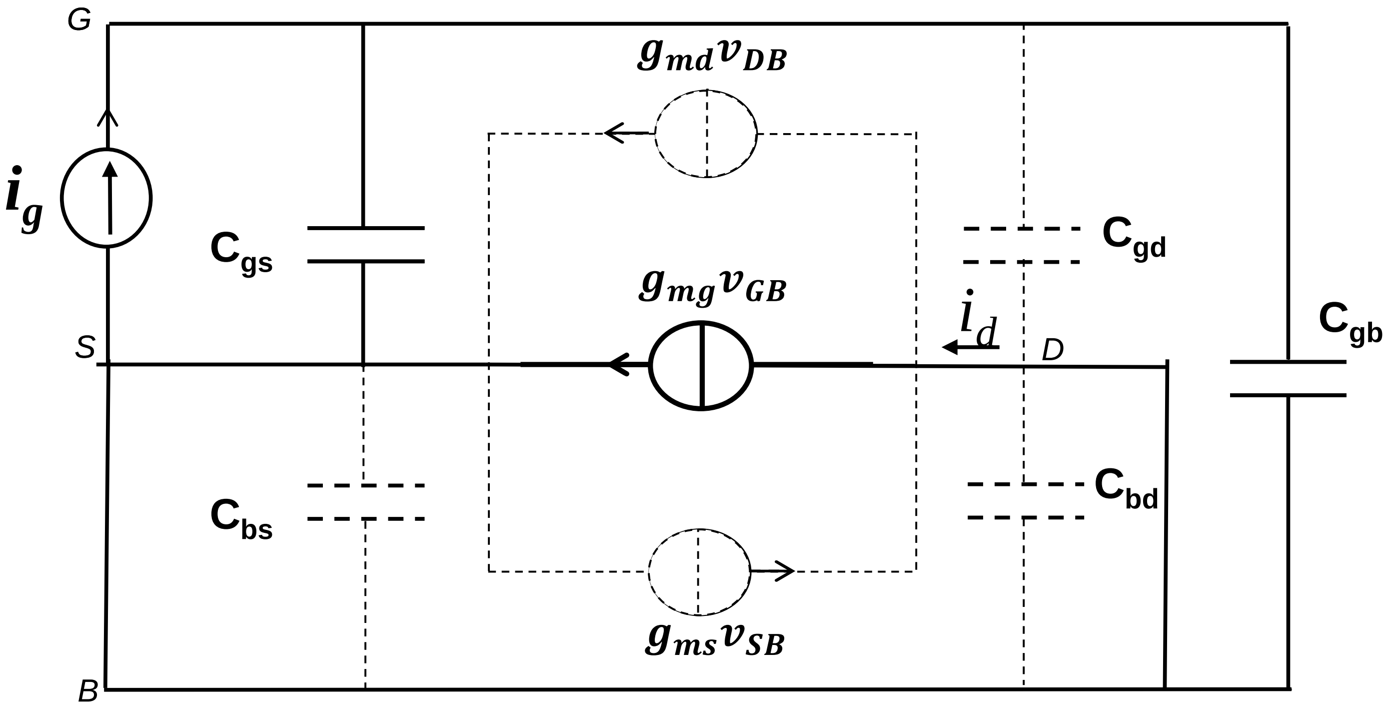
$$\boxed{g_{ms} \gg \omega C_{ds}}$$



12. Quasi-static AC model

The intrinsic transition frequency: The frequency at which $|i_d/i_g|=1$ in the common-source amplifier

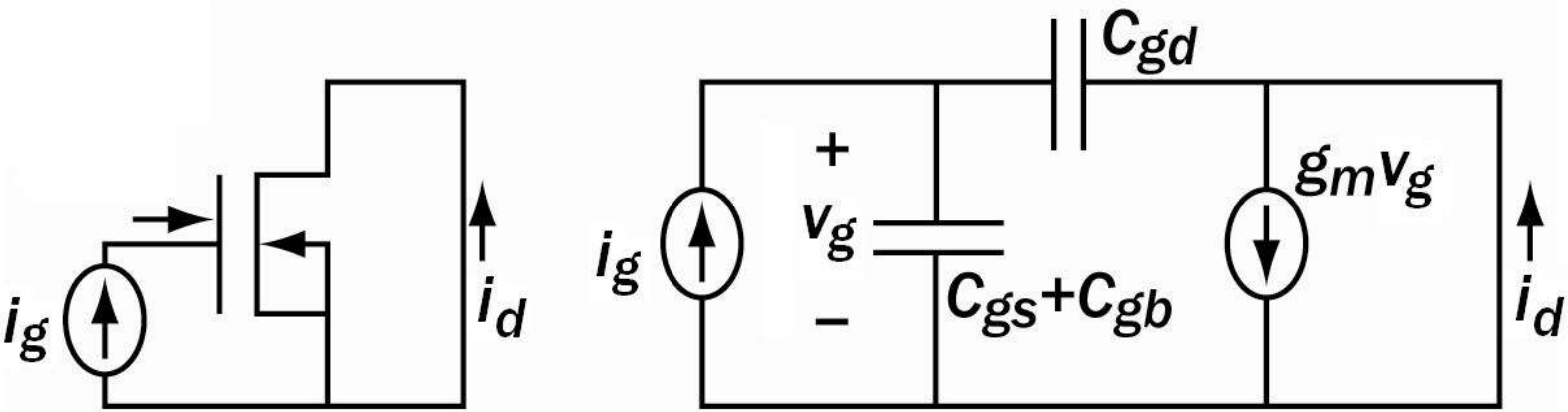




12. Quasi-static AC model

The intrinsic transition frequency

MOSFET in saturation: intrinsic C_{gd}=0



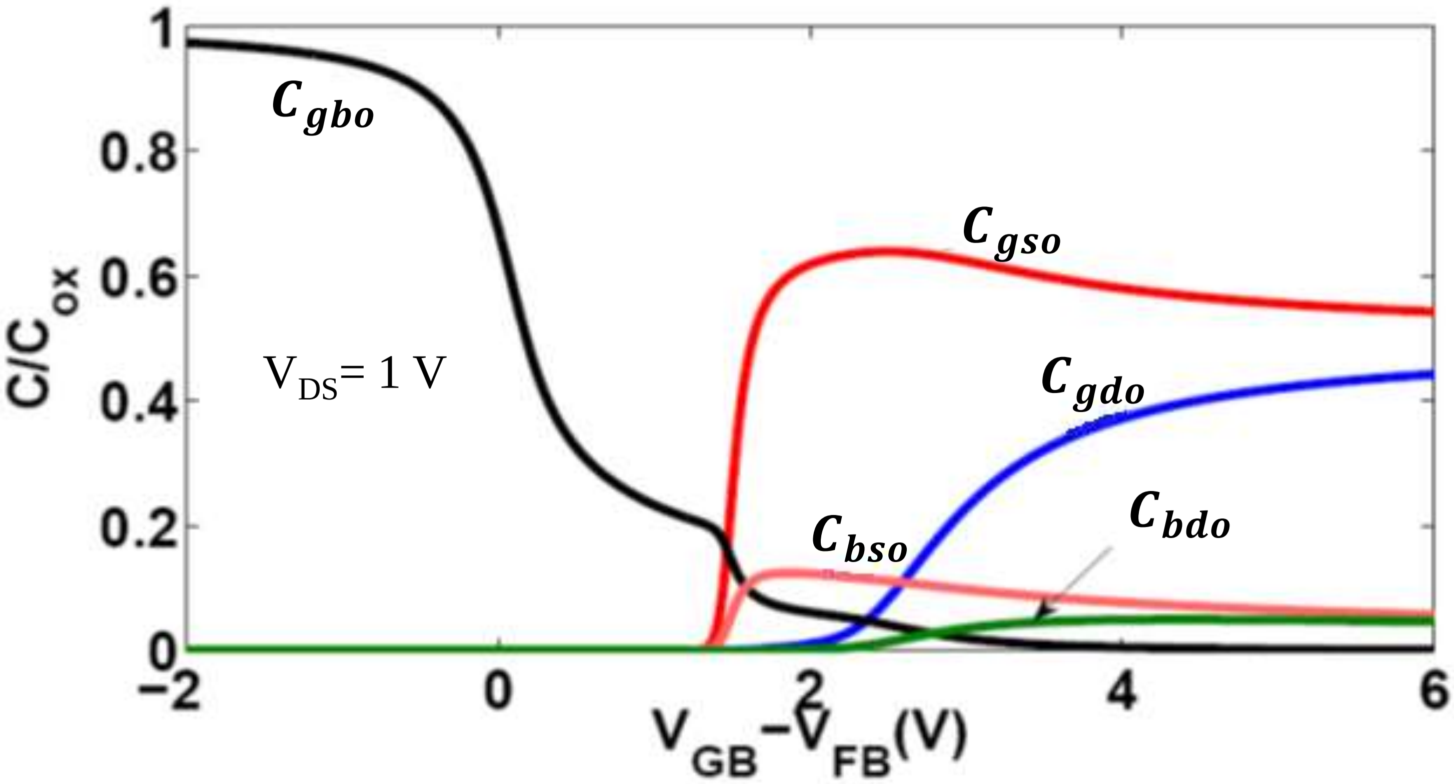
$$f_T=\frac{g_{mg}}{2\pi\left(C_{gs}+C_{gb}\right)}=\frac{g_{ms}}{2\pi n\left(C_{gs}+C_{gb}\right)}$$

$$g_{ms}=\mu C_{ox} n\varphi_t\frac{W}{L}\left(\sqrt{1+i_f}-1\right)$$

$$C_{gs}+C_{gb}\cong\frac{C_{ox}}{2}$$ **Rough approximation**

$$\boxed{f_T\cong\frac{\mu\varphi_t}{2\pi L^2}2\left(\sqrt{1+i_f}-1\right)}$$

12. Quasi-static AC model



$$C_{gbo} = \frac{n-1}{n}\left(WLC_{ox} - C_{gso} - C_{gdo}\right)$$

$$\boxed{\alpha = \frac{1+q_D}{1+q_S}}$$

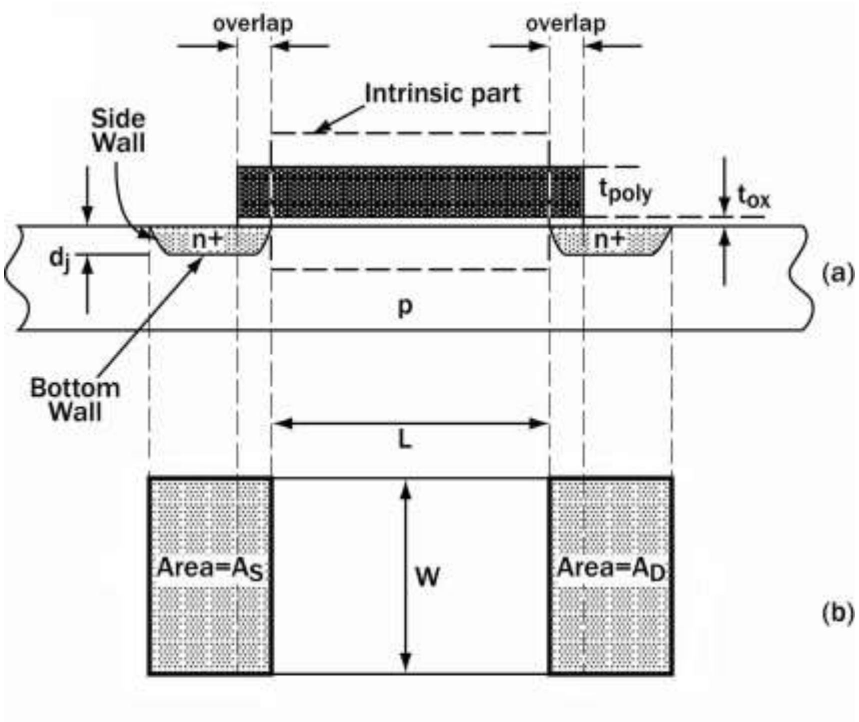
channel linearity factor

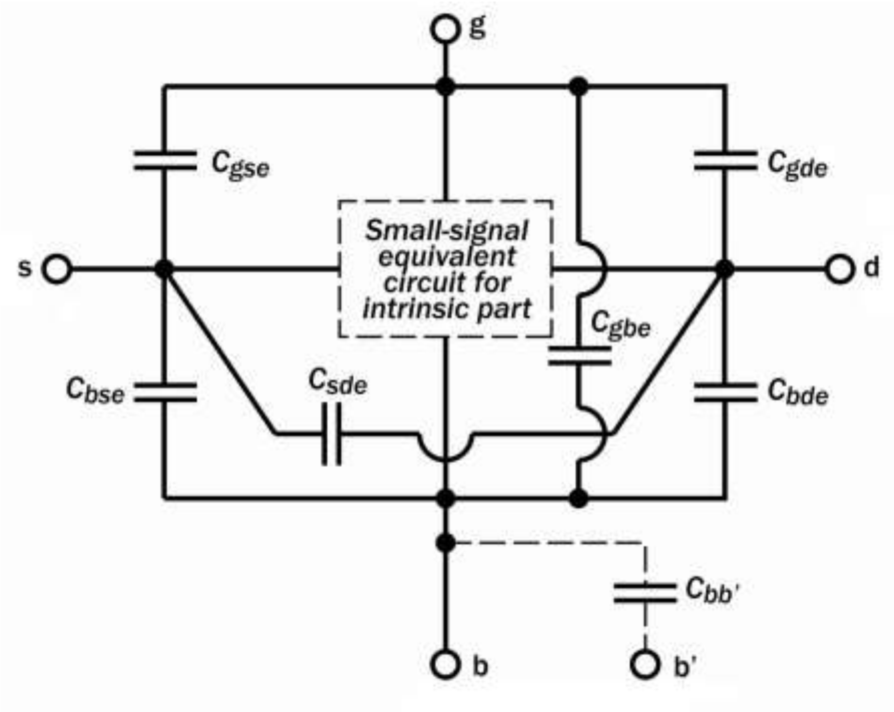
$$C_{gso} = \frac{2}{3}WLC_{ox}\frac{1+2\alpha}{(1+\alpha)^2}\frac{q_s - q_{Dsat}}{1+q_s-q_{Dsat}}$$

$$C_{gdo} = \frac{2}{3}WLC_{ox}\frac{\alpha^2+2\alpha}{(1+\alpha)^2}\frac{q_D - q_{Dsat}}{1+q_D-q_{Dsat}}$$

12. Quasi-static AC model

Capacitances of extrinsic transistor





Y. Tsividis, Operation and Modeling of the MOS Transistor,
Second edition, Oxford University Press, 1999.

13. Extraction of parameters

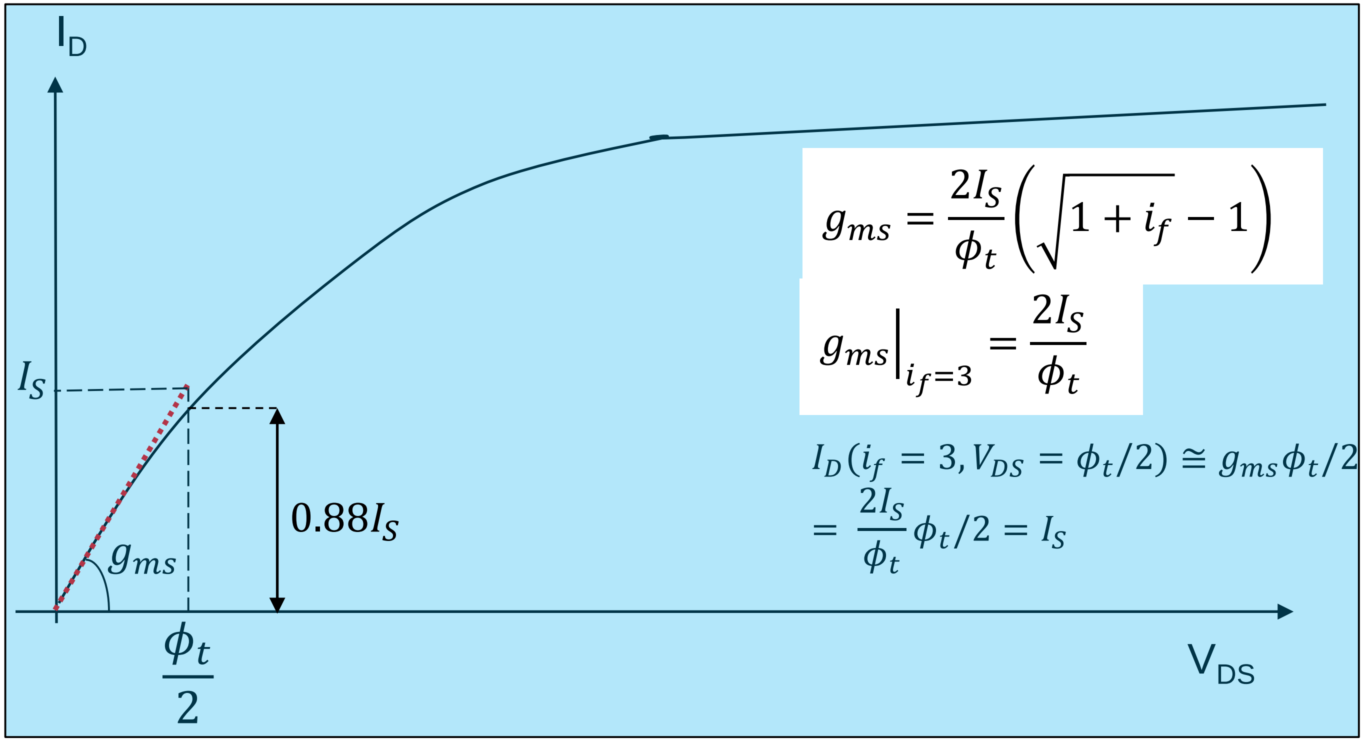
VV_{T0}, I_S and n extraction: The g_m/I_D method

$$\frac{g_m}{I_D}=\frac{2}{n\phi_t\left(\sqrt{1+i_f}+\sqrt{1+i_r}\right)}$$

$$\left.\frac{g_m}{I_D}\right|_{V_{DS}\to 0}=\frac{1}{n\phi_t\sqrt{1+i_f}}$$

$$\left(\frac{g_m}{I_D}\right)_{max}\cong\frac{1}{n\phi_t}$$

At threshold ($i_f = 3$) g_m/I_D is at **½ of its maximum value**



$$g_{ms}=\frac{2I_S}{\phi_t}\left(\sqrt{1+i_f}-1\right)$$

$$\left.g_{ms}\right|_{i_f=3}=\frac{2I_S}{\phi_t}$$

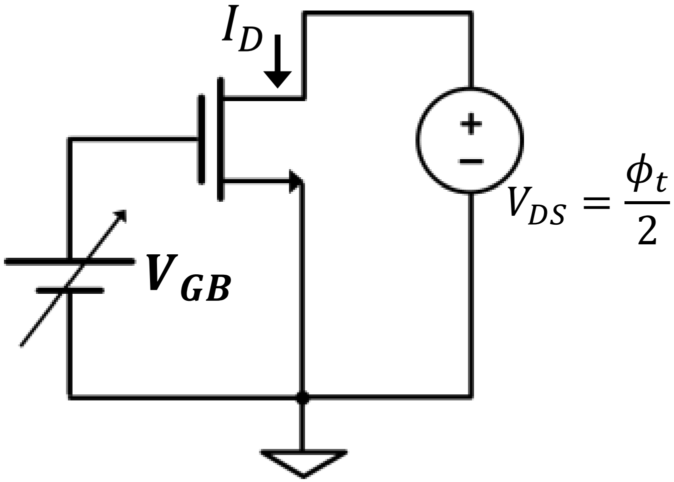
$$I_D(i_f=3, V_{DS}=\phi_t/2)\cong g_{ms}\phi_t/2$$
$$=\frac{2I_S}{\phi_t}\phi_t/2=I_S$$

11. Extraction of parameters

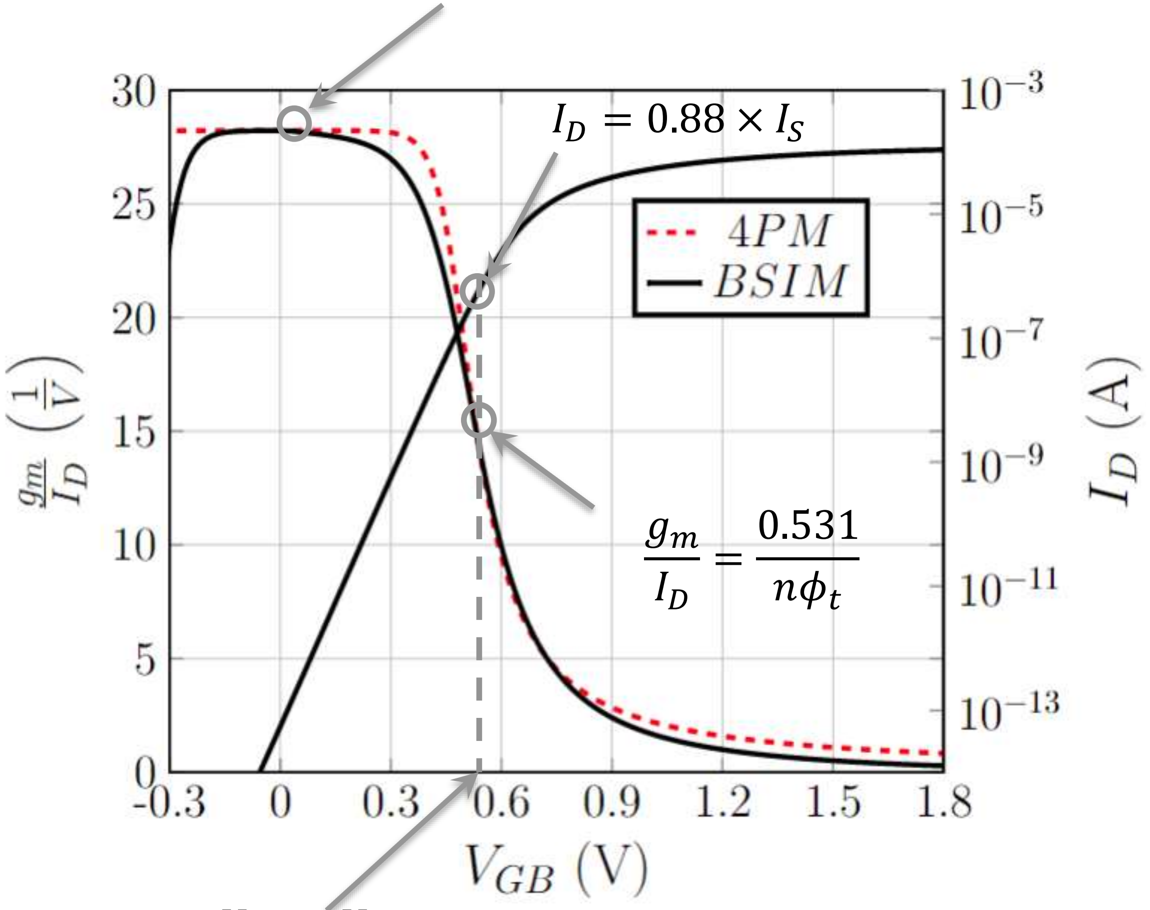
V_{T0}, I_S and n extraction: The g_m/I_D method

$$\boxed{\left.\frac{g_m}{I_D}\right|_{V_{DS}=\frac{\phi_t}{2},i_f=3} = \frac{0.531}{n\phi_t}}$$

$$\left(\frac{g_m}{I_D}\right)_{max} \cong \frac{1}{n\phi_t}$$



$V_{DS} = \frac{\phi_t}{2}$



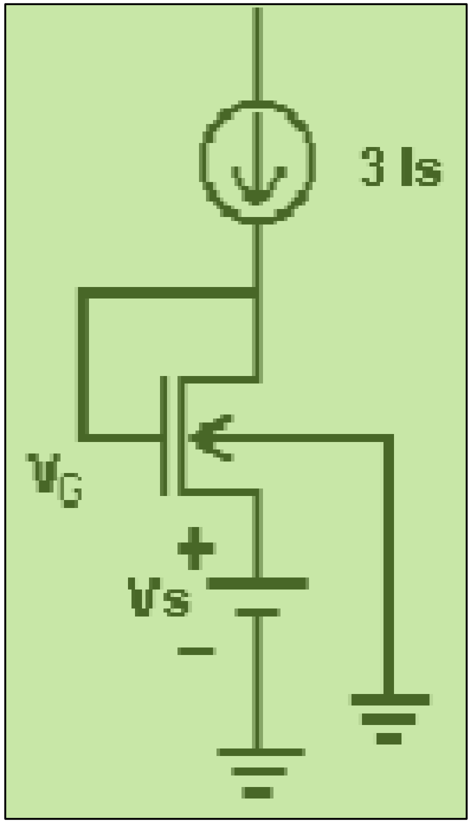
$I_D = 0.88 \times I_S$

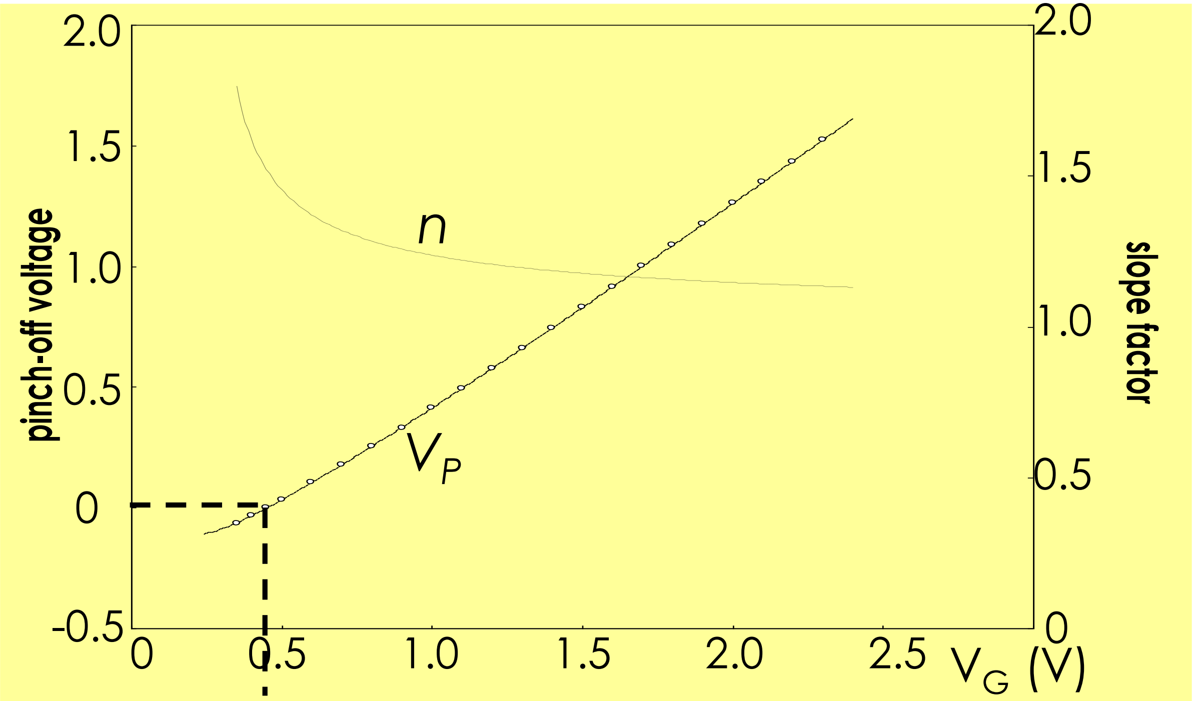
$\frac{g_m}{I_D} = \frac{0.531}{n\phi_t}$

$V_{GB} = V_{T0}$

13. Extraction of parameters

Pinch-off voltage and slope factor vs. gate voltage





V_{T0} (threshold voltage)

$$I_D = I_F - I_R \cong I_F = 3I_S$$

$$i_f = \frac{I_F}{I_S} = 3$$

$$V_P - V_{SB} = \phi_t\left[\sqrt{1+i_f} - 2 + \ln\left(\sqrt{1+i_f} - 1\right)\right]$$

$$(V_P - V_{SB})\Big|_{i_f=3} = 0 \Rightarrow V_P = V_{SB}$$

$$\frac{dV_P}{dV_G} = \frac{1}{n}$$

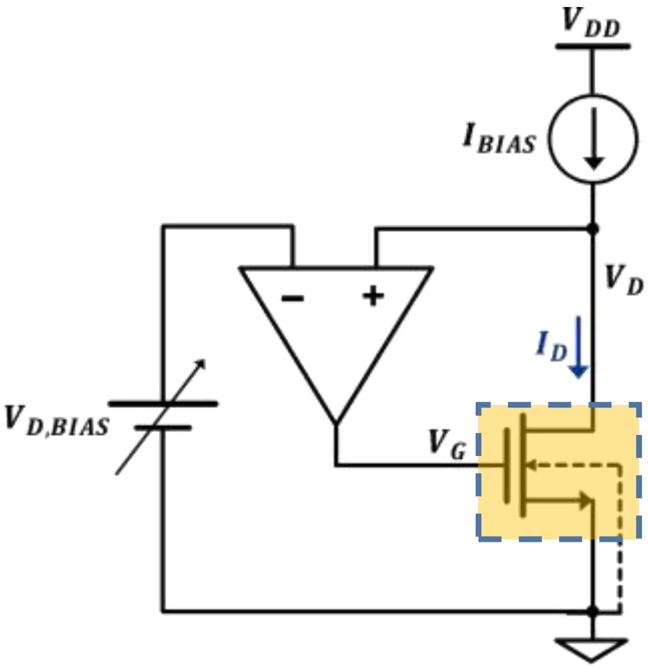
$$V_P \cong \frac{V_G - V_{T0}}{n}$$

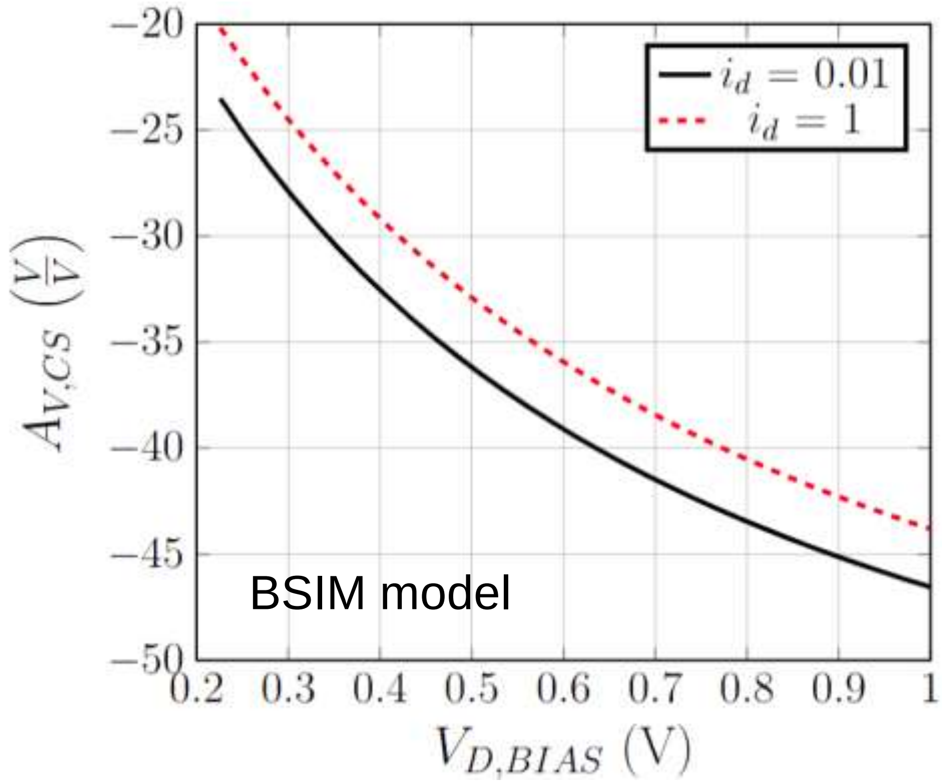
13. Extraction of parameters

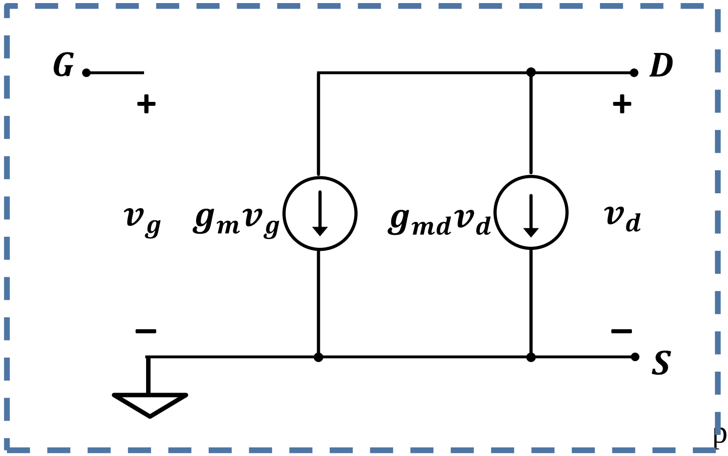
Extraction of σ in WI (MI) & saturation

Common-Source Intrinsic Gain Method

$$A_{V,CS} = \frac{v_d}{v_g} = -\frac{g_m}{g_{md}} = -\frac{\frac{g_m}{I_{D,sat}}}{\frac{g_{md}}{I_{D,sat}}} = -\frac{\frac{1}{\phi_t}\left(\frac{1}{n}\right)\frac{2}{\sqrt{1+i_d}+1}}{\frac{1}{\phi_t}\left(\frac{\sigma}{n}\right)\frac{2}{\sqrt{1+i_d}+1}} = -\frac{1}{\sigma}$$

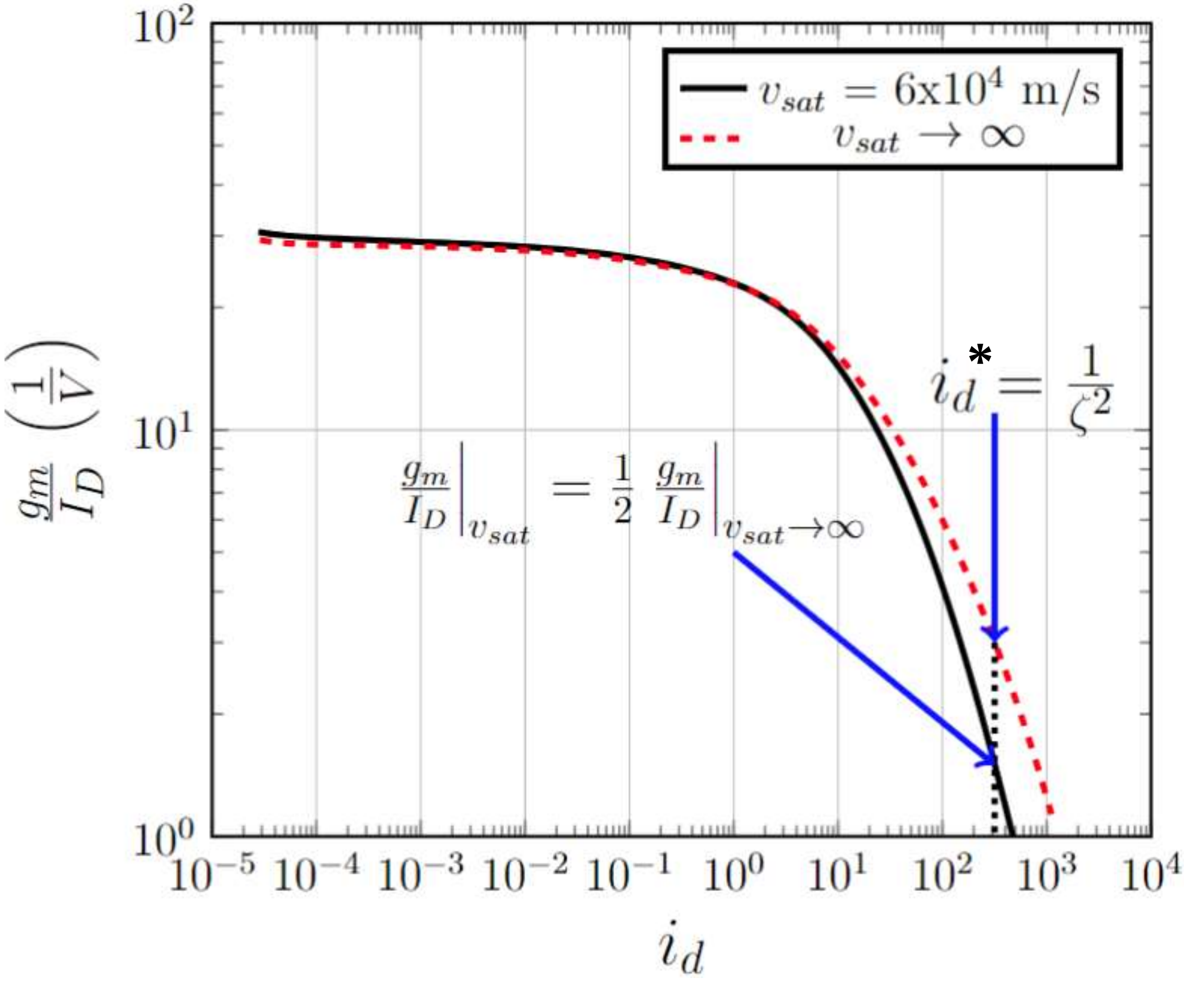






13. Extraction of parameters

Extraction of ξ (velocity saturation parameter)



Extraction of ξ

Simulation – OK
Experiment – to be developed

$i_d^* = 317$

$\zeta = \frac{1}{\sqrt{i_d^*}}$=0.056

REFERENCES

- A. I. A. Cunha, M. C. Schneider and C. Galup-Montoro, "An MOS Transistor Model for Analog Circuit Design", IEEE J. Solid-State Circuits, vol. 33, no. 10, pp. 1510-1519, October 1998.
- C. Galup-Montoro and M. C. Schneider, *MOSFET Modeling for Circuit Analysis and Design*, World Scientific, 2007.
- M. C. Schneider and C. Galup-Montoro, *CMOS Analog Design Using All-Region MOSFET Modeling*, Cambridge, 2010.
- D. G. Alves Neto, C. M. Adornes, G. Maranhão, M. K. Bouchoucha, M. J. Barragan, A. Cathelin, M. C. Schneider, S. Bourdel, C. Galup-Montoro, A 5-DC-Parameter MOSFET Model for Circuit Simulation in QucsStudio and Spectre, Newcas 2023 (Best Paper Award).
- C. M. Adornes, D. G. Alves Neto, M. C. Schneider and C. Galup-Montoro, " Bridging the Gap between Design and Simulation of Low-Voltage CMOS Circuits ," Journal of Low Power Electronics and Applications, vol. 12, issue 2, June 2022.

THANK YOU VERY MUCH FOR YOUR ATTENTION

Lima - September 2024