Analysis, Design and Simulation of analog/RF & Digital Circuits with Open-Source EDA Tools and Process Design Kit

SLIDES >>>>>>>>>> https://github.com/Deni-Alves/MOSFET_model

LASCAS 2025
16th IEEE CASS Latin American Symposium on Circuits and Systems

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“Scan me”

Part 1

Advanced Compact MOSFET Model: ACM2

"Scan me"

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Carlos Galup-Montoro

https://github.com/ACMmodel/MOSFET_model

Outline

- Introduction: ACM timeline
- ACM2 model
- Long-channel: I_D and g_m/I_D models
- Long-channel: MOS basic amplifier design

ACM timeline

- 1993 ϕs-based model (SBMICRO, Campinas, Br)
- 1995 Long-channel charge-based model (SSE, Nov.)
- 1996 gm/ID model (SBMICRO, Aguas de Lindoia, Br)
- 1997 Unified current control model (ISCAS, Hong Kong)
- 1998 Most referenced ACM paper (JSSC, Oct.)
- 2000 ACM model in SMASH simulator (CICC, Orlando)
- 2021 4-parameter single-piece model (NorCAS, Oslo)
- 2023 ACM2 in VERILOG-AMS (NEWCAS, Edinburgh)

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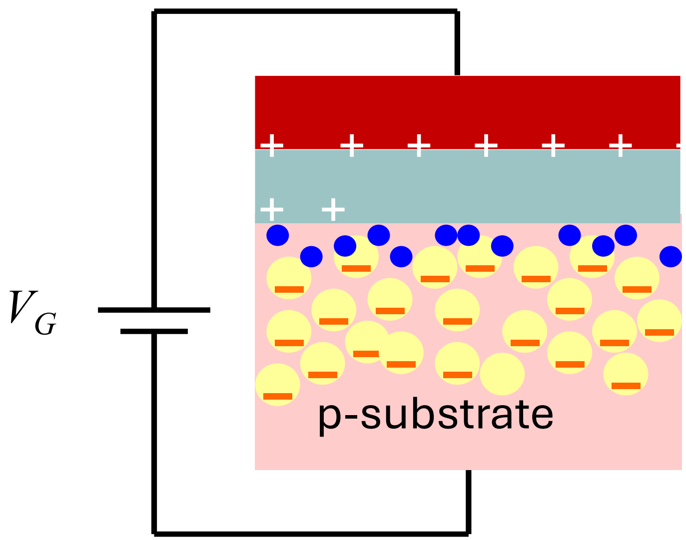
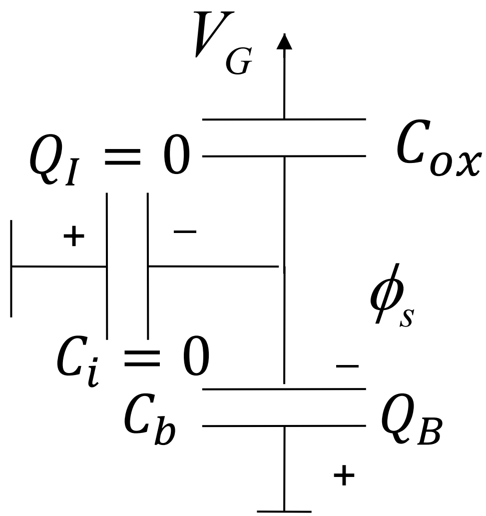
The capacitive model of the MOSFET





$$\frac{\Delta\phi_s}{\Delta V_G} = \frac{C_{ox}}{C_{ox} + C_b} = \frac{1}{n}$$

ϕ_s **surface potential**

$$\phi_s = 2\phi_F + \frac{V_G - V_{T0}}{n} = 2\phi_F + V_P$$

C_{ox} **oxide capacitance per unit area**

C_b **depletion capacitance per unit area**

Q_I **carrier charge density**

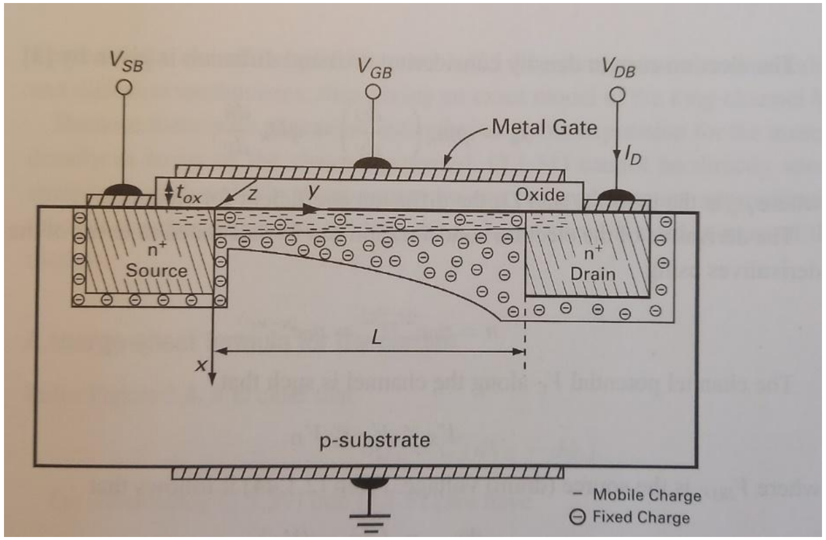
V_{T0} **threshold voltage**

Drain current model: main simplifications

First approximation ACM2 $$dQ_I = nC_{ox}d\phi_s$$

Second approximation ACM2 $$I_D = \mu W \left(-Q_I \frac{d\phi_s}{dy} + \phi_t \frac{dQ_I}{dy} \right)$$

drift Diffusion



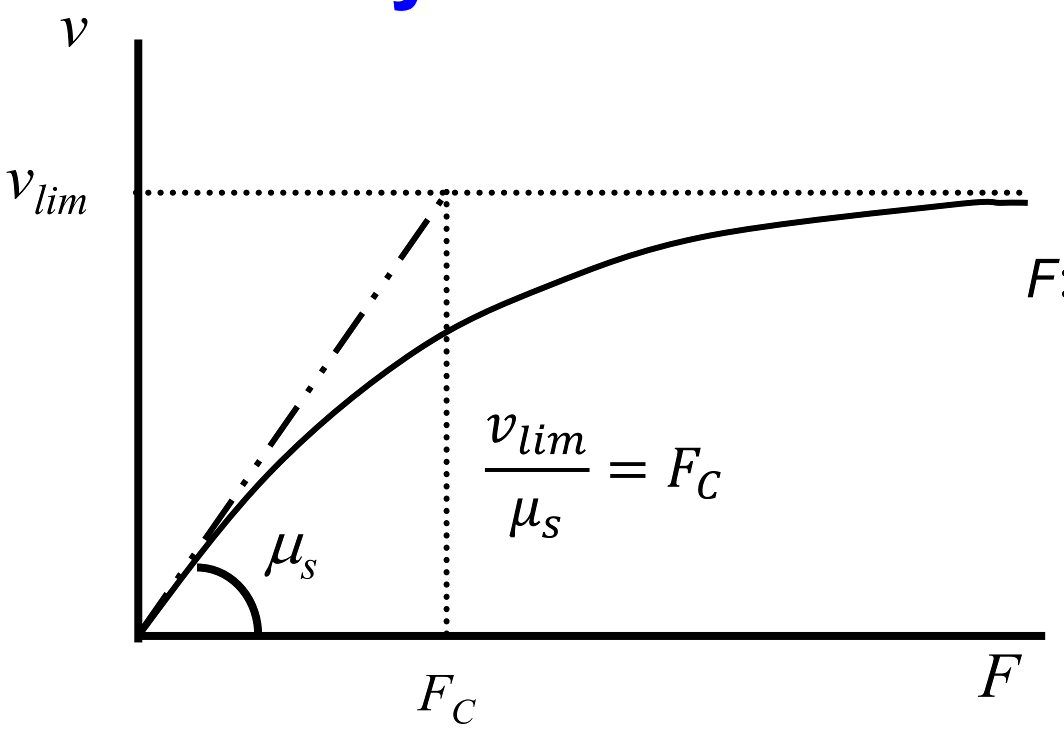
Q_I carrier charge density

W transistor width

μ carrier mobility

ϕ_t thermal voltage
26 mV @ 300K

Velocity saturation



ϕ_S: surface potential

F: longitudinal electrical field

$$\frac{d\phi_S}{dy} = -F$$

Third approximation ACM2

$$\mu = \frac{\mu_s}{1 + \frac{\mu_s}{v_{lim}}\frac{d\phi_S}{dy}}$$

Allows analytical integration for I_D

ACM2 current law

From the 3 approximations:
normalized current vs. normalized charge densities at source and drain

$$i_D = \frac{(q_S + q_D + 2)}{1 + \zeta(q_S - q_D)}(q_S - q_D)$$

$$i_D = I_D/I_S$$

$$I_S = \frac{W}{L}\mu_s n C_{ox}\frac{\phi_t^2}{2}$$

normalization (specific) current

$$q_{S(D)} = Q_{S(D)}/(-nC_{ox}\phi_t)$$

$-nC_{ox}\phi_t$ thermal charge

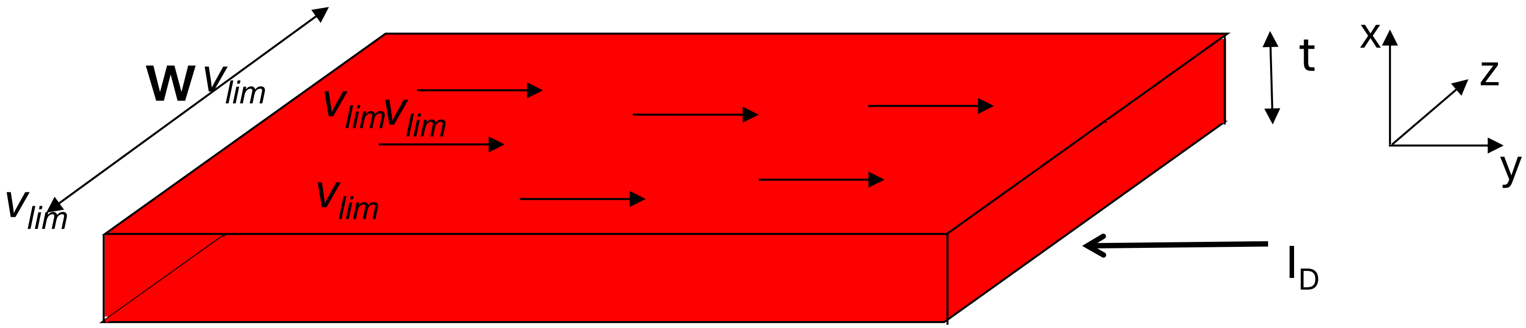
SI : $q_{S(D)} >> 1$ *WI :* $q_{S(D)} << 1$

Short-channel parameter ζ :

$$\zeta = \frac{(\mu_s\phi_t/L)}{v_{lim}}$$

ratio of diffusion-related velocity to saturation velocity

Physics-based saturation



Saturation current due to saturation velocity of the carriers

$$I_{Dsat} = -W Q_{Dsat}\, v_{lim}$$

Q_{Dsat} is the saturation inversion charge per unit area

or, using normalized variables

$$i_{Dsat} = \frac{2}{\zeta} q_{dsat}$$

"Carrier velocity approaches v_{sat}, but never reaches v_{sat}"
Y.Taur TED March 2019

Physics-based saturation: design model

$$i_{Dsat} = \frac{2}{\zeta} q_{dsat} \qquad\qquad i_{Dsat} = \frac{(q_S + q_{Dsat} + 2)}{1 + \zeta(q_S - q_{Dsat})}(q_S - q_{Dsat})$$

$$q_{Dsat} = q_s + 1 + \frac{1}{\zeta} - \sqrt{\left(1 + \frac{1}{\zeta}\right)^2 + \frac{2q_S}{\zeta}}$$

or equivalently

$$q_s = \sqrt{1 + \frac{2}{\zeta} q_{dsat}} - 1 + q_{dsat}$$

The Unified Charge Control Model (UCCM)

$$\frac{V_P - V_C}{\phi_t} = q_I - 1 + \ln q_I$$

$$V_S \le V_C \le V_D$$

$$q_S \le q_I \le q_D$$

$$\Rightarrow \frac{V_{DS}}{\phi_t} = q_S - q_D + \ln \frac{q_S}{q_D}$$

The "Regional" Weak (WI) and Strong Inversion (SI) Approximations

WI

$$q_I \ll 1 \;\rightarrow V_P - V_C \ll -\phi_t$$

$$q_I \cong e^{\frac{V_P - V_C + \phi_t}{\phi_t}}$$

Error <10% for $q_I < 0.22$

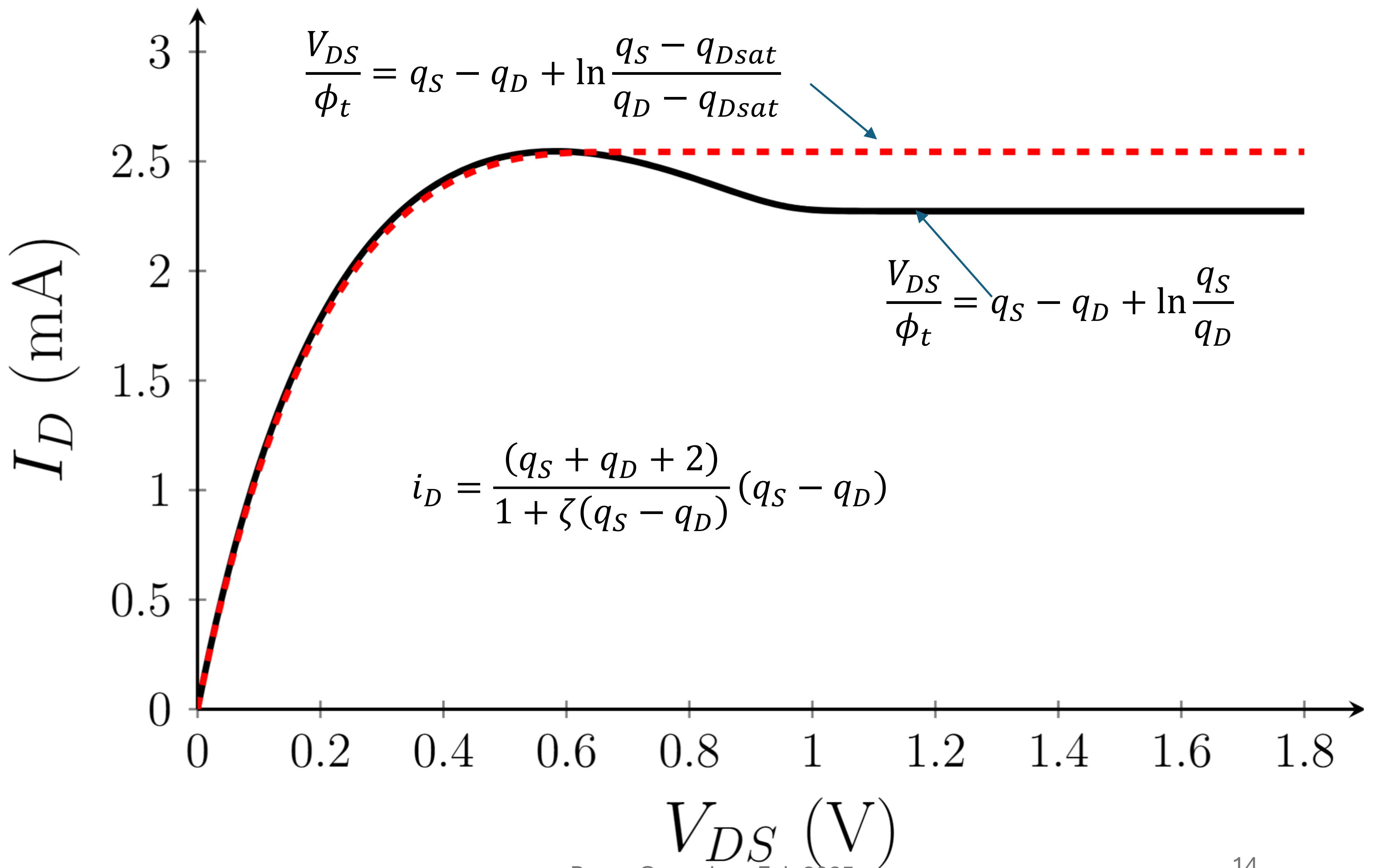
SI

$$q_I \gg 1 \;\rightarrow V_P - V_C \gg \phi_t$$

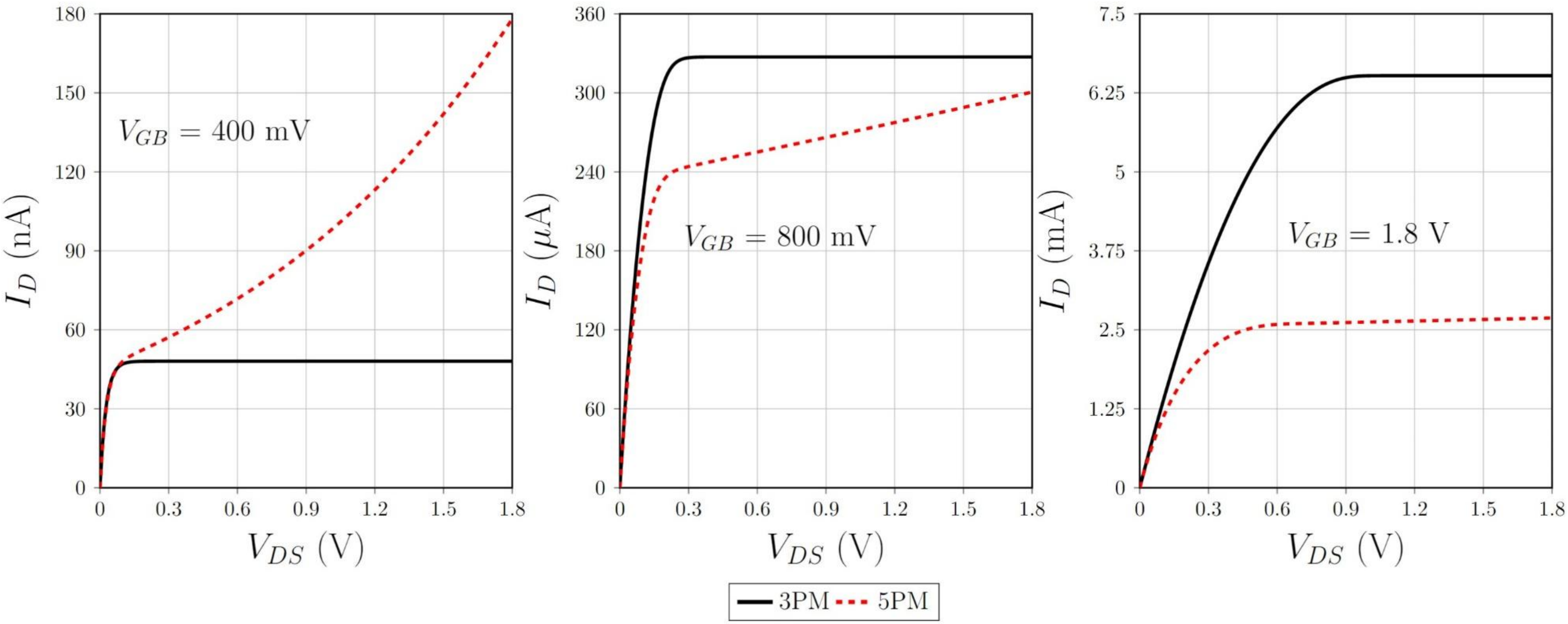
$$q_I \cong \frac{V_P - V_C + \phi_t}{\phi_t}$$

Error <10% for $q_I > 20$

UCCM including the effect of velocity saturation



Output curves including DIBL and v_{sat}



$DIBL\ model$: $V_T = V_{T0} - \sigma(V_S + V_D)$

Transistor	W/L ($\mu m/\mu m$)	V_{T0} (mV)	I_S (μA)	n	σ	ζ
NMOS2V	$\mathbf{5/0.18}$	528	5.52	1.37	0.025	0.056

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- **Introduction: ACM timeline**
- **ACM2 model**
- **Long-channel: I_D and g_m/I_D models**
- **Long-channel: MOS basic amplifier design**

Long-channel charge-based model

$For\ short\ channel\ MOS$ $$I_D = I_S \frac{(q_S + q_D + 2)}{1 + \zeta(q_S - q_D)} (q_S - q_D)$$

$$\frac{V_P - V_S}{\phi_t} = q_S - 1 + \ln q_S \qquad \frac{V_{DS}}{\phi_t} = q_S - q_D + \ln \frac{q_S - q_{Dsat}}{q_D - q_{Dsat}}$$

$For\ long\ channel\ MOS$ ζ=0 → q_{Dsat}=0

$$I_D = I_S(q_S + q_D + 2)(q_S - q_D) = I_S[(q_S^2 + 2q_S) - (q_D^2 + 2q_D)]$$

$$\frac{V_P - V_{S(D)}}{\phi_t} = q_{S(D)} - 1 + \ln q_{S(D)}$$

Obs: $\frac{dq_{S(D)}}{dV_G} = -\frac{1}{n}\frac{dq_{S(D)}}{dV_{S(D)}}$ $\qquad \frac{dq_D}{dV_D} = -\frac{1}{\phi_t}\frac{q_D}{q_D + 1}$ $\qquad \frac{dI_D}{dq_D} = -2I_S(q_D + 1)$

Small-signal transconductances

$$g_{md} = \frac{dI_D}{dV_D} = \frac{dI_D}{dq_D}\frac{dq_D}{dV_D} = 2I_S(q_D + 1)\frac{1}{\phi_t}\frac{q_D}{q_D + 1} = \frac{2I_S}{\phi_t}q_D$$

Symmetry

Amazingly simple (see Appendix)

$$g_{ms} = \frac{2I_S}{\phi_t}q_S$$

$$g_m = \frac{dI_D}{dV_G} = \frac{dI_D}{dq_S}\frac{dq_S}{dV_G} + \frac{dI_D}{dq_D}\frac{dq_D}{dV_G} \qquad \frac{dq_{S(D)}}{dV_G} = -\frac{1}{n}\frac{dq_{S(D)}}{dV_{S(D)}}$$

$$\boxed{g_m = \frac{g_{ms} - g_{md}}{n}}$$

$$g_m = \frac{g_{ms}}{n} \longrightarrow \text{in saturation}$$

Unified Current Control Model (UICM)-I

$$\boxed{I_D = I_S[(q_S^2 + 2q_S) - (q_D^2 + 2q_D)]}$$ (A)

(A) can also be written as

$$\boxed{I_D = I_F - I_R = I_S\left[i_f - i_r\right]}$$ (B)

$\boxed{I_F, I_R}$: forward and reverse currents

$\boxed{i_{f(r)} = q_{S(D)}^2 + 2q_{S(D)}}$: forward (reverse) inversion coefficients

$$\downarrow$$

$$q_{S(D)} = \sqrt{1 + i_{f(r)}} - 1$$

Unified Current Control Model (UICM)-II

$$\frac{V_P - V_{S(D)}}{\phi_t} = q_{S(D)} - 1 + \ln q_{S(D)}$$

$$\boxed{q_{S(D)} = \sqrt{1 + i_{f(r)}} - 1}$$

Normalized UICM

$$\boxed{\frac{V_P - V_{S(D)}}{\phi_t} = \sqrt{1 + i_{f(r)}} - 2 + \ln\left(\sqrt{1 + i_{f(r)}} - 1\right)}$$

$$\frac{V_{DS}}{\phi_t} = q_S - q_D + \ln\frac{q_S}{q_D} = \sqrt{1 + i_f} - \sqrt{1 + i_r} + \ln\left(\frac{\sqrt{1 + i_f} - 1}{\sqrt{1 + i_r} - 1}\right)$$

g_m/I_D

$$g_{ms(d)} = \frac{2I_S}{\phi_t}\left(\sqrt{1+i_{f(r)}}-1\right) = \frac{W}{L}\mu C_{ox} n\phi_t\left(\sqrt{1+i_{f(r)}}-1\right)$$

$$g_m = \frac{g_{ms}-g_{md}}{n}$$

$$\boxed{\frac{g_m}{I_D} = \frac{2}{n\phi_t\left(\sqrt{1+i_f}+\sqrt{1+i_r}\right)}}$$

For V_{DS}/ϕ_t<<1 we have $i_f \cong i_r$

$$\boxed{\frac{g_m}{I_D} \cong \frac{1}{n\phi_t\sqrt{1+i_f}}}$$

In saturation $i_f >> i_r$

$$\boxed{\frac{g_m}{I_D} \cong \frac{2}{n\phi_t\left(\sqrt{1+i_f}+1\right)}}$$

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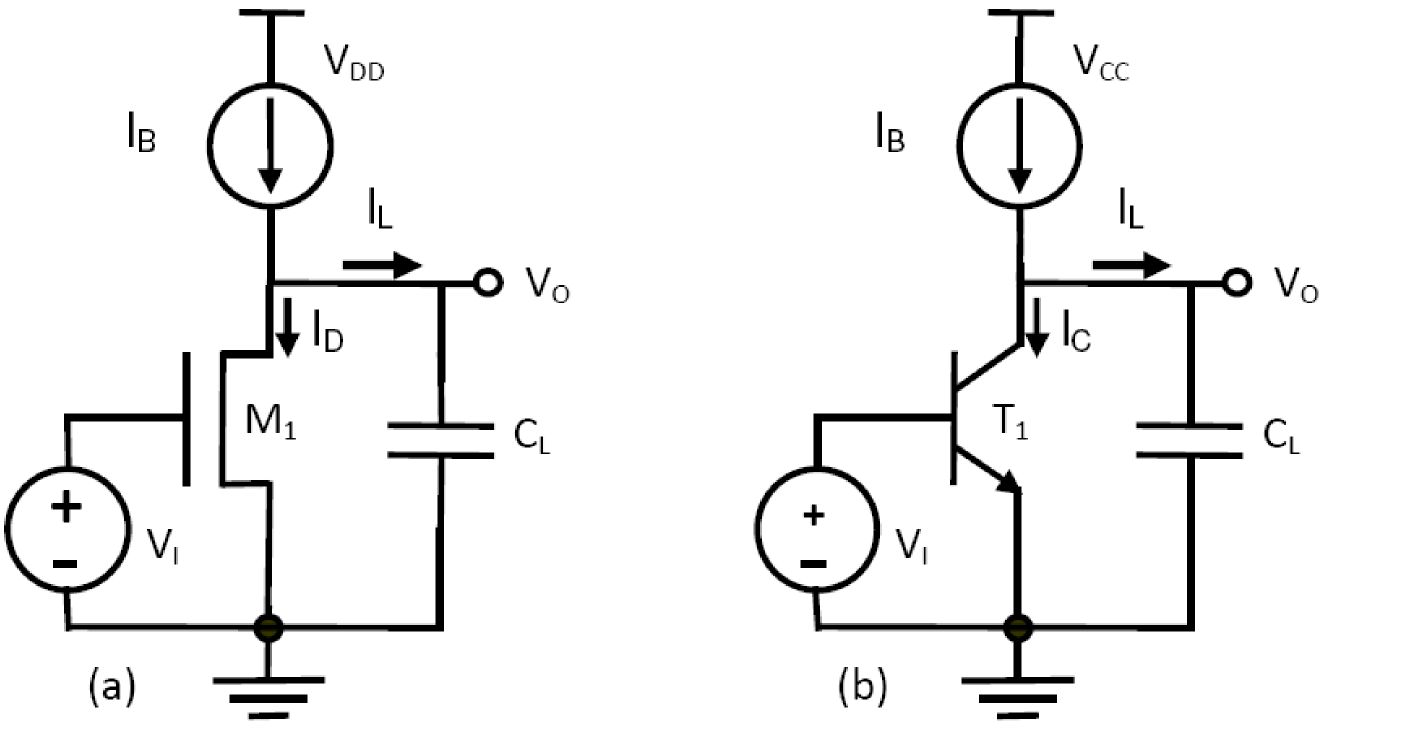
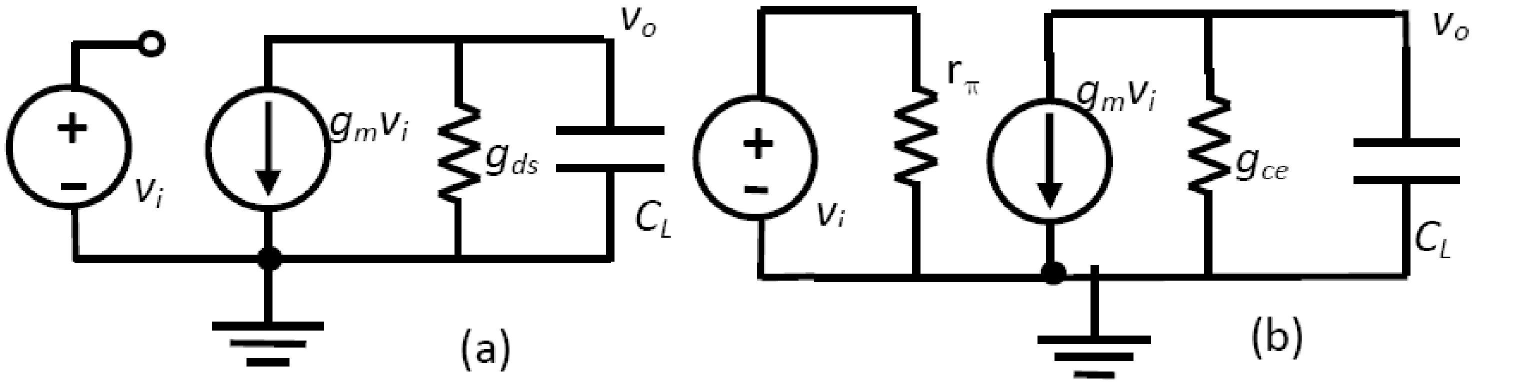
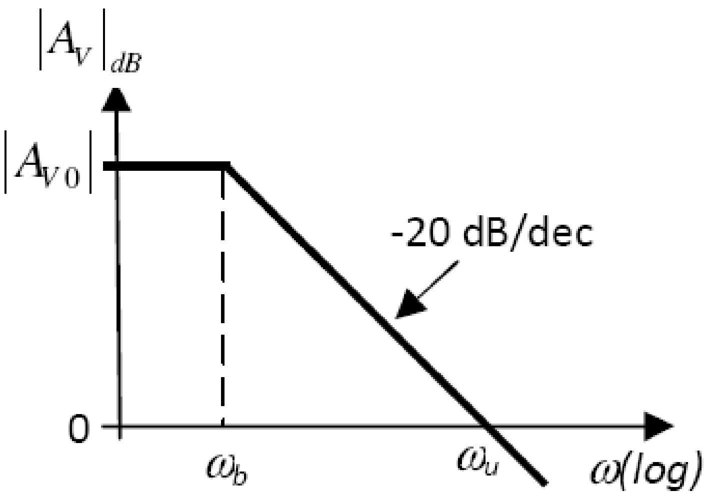
Intrinsic gain stages: common-source and common-emitter amplifiers



Small-signal circuit and frequency response of the CS and CE amplifiers





$$v_o \cong -\frac{g_m}{j\omega C_L} v_i; \qquad \omega >> \omega_b$$

$$\boxed{\omega_u = \frac{g_m}{C_L}}$$

Design of the CE and CS amplifiers

$$\left|A_v\left(\omega_u\right)\right| = 1 \qquad g_m = \omega_u C_L = 2\pi \cdot GB \cdot C_L$$

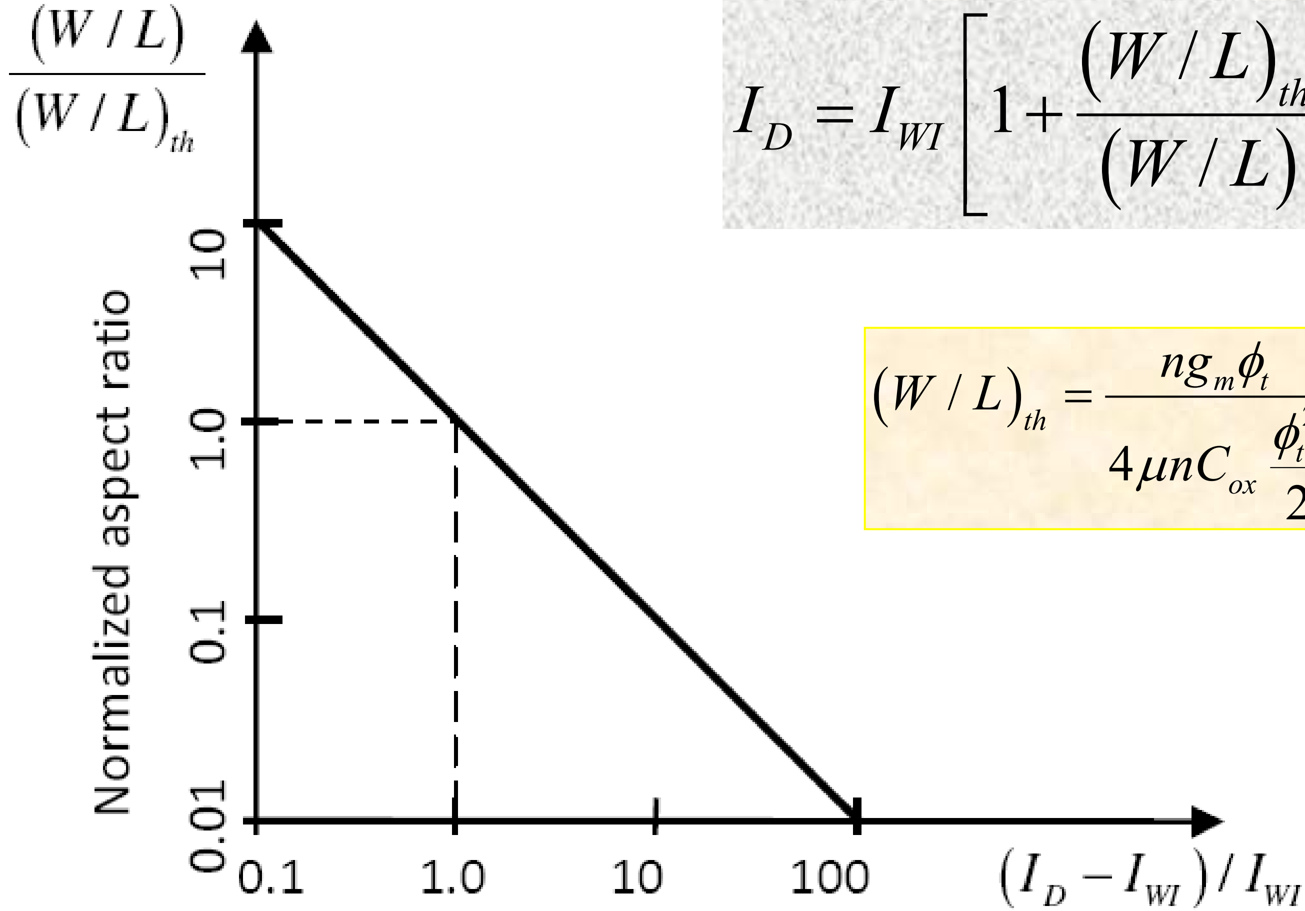
BJT in the direct active region

$$I_C = I_S e^{V_{BE}/\phi_t} \Rightarrow I_C = g_m \phi_t = 2\pi \cdot GB \cdot C_L \cdot \phi_t$$

MOSFET in saturation

$$I_D = n g_m \phi_t \frac{\left(\sqrt{1+i_f}+1\right)}{2} = n g_m \phi_t \left[1 + \frac{g_m}{2\mu C_{ox}\phi_t (W/L)}\right]$$

Aspect ratio vs. current excess in MOSFET design



$$I_D = I_{WI}\left[1 + \frac{(W/L)_{th}}{(W/L)}\right]$$

$$(W/L)_{th} = \frac{n g_m \phi_t}{4\mu n C_{ox} \frac{\phi_t^2}{2}}$$

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- C. Galup-Montoro and M. C. Schneider, *MOSFET Modeling for Circuit Analysis and Design*, World Scientific, 2007.

- C. M. Adornes, D. G. Alves Neto, M. C. Schneider and C. Galup-Montoro, " Bridging the Gap between Design and Simulation of Low-Voltage CMOS Circuits ," Journal of Low Power Electronics and Applications, June 2022.

- D. G. Alves Neto *et al,* “Design-oriented single-piece 5-DC parameter MOSFET model,” *IEEE Access*, 2024.

Appendix: the exact model of the long-channel MOSFET[1]

$$I_D = -\frac{W}{L}\int_{V_S}^{V_D} \mu Q_I\,(V_C) d\,V_C$$

Consequently, the **exact** expressions for g_{ms} and g_{md} are

$$g_{md} = \frac{dI_D}{dV_D} = -\frac{W}{L}\mu Q_D = \frac{2I_S}{\phi_t} q_D$$

$$g_{ms} = -\frac{dI_S}{dV_S} = -\frac{W}{L}\mu Q_S = \frac{2I_S}{\phi_t} q_S$$

[1] H. C. Pao and C. T. Sah, ‘Effects of diffusion current on characteristics of metal-oxide (insulator)-semiconductor transistors” Solid-State Electronics, Oct 1966

GRENOBLE INP UGA

TiMA

UFSC

Part 2
Advanced Compact MOSFET Model: Parameter extraction

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- ACM2 :
  - Parameter Extraction
    - VT0, IS and n
    - Sigma & Zeta
  - DC characteristics
  - Transconductances in Saturation
  - Example: Inverter CMOS
- Overview of Open-source environment
  - Automatic parameter extraction

ACM2: A simple 5-DC-parameter MOSFET model

$$V_P = \frac{V_{GB} - \boldsymbol{V_{T0}} + \boldsymbol{\sigma}(V_{DB} + V_{SB})}{\boldsymbol{n}}$$

$$\frac{V_P - V_{SB}}{\phi_t} = q_s - 1 + \ln(q_s)$$

Used to calculate q_s

$$q_{dsat} = q_s + 1 + \frac{1}{\boldsymbol{\zeta}} - \sqrt{\left(1 + \frac{1}{\boldsymbol{\zeta}}\right)^2 + \frac{2q_s}{\boldsymbol{\zeta}}}$$

$$\frac{V_{DS}}{\phi_t} = q_s - q_d + \ln\left(\frac{q_s - q_{dsat}}{q_d - q_{dsat}}\right)$$

Used to calculate q_d

$$I_D = \boldsymbol{I_S} \frac{(q_s + q_d + 2)}{1 + \boldsymbol{\zeta}(q_s - q_d)}(q_s - q_d)$$

Specific current I_S ***(W,L)***	Threshold voltage V_{T0} ***(W,L)***	Slope factor n ***(W,L)***	DIBL factor σ ***(W,L)***	V_{sat} effect ζ ***(W,L)***

3PM-ACM model in a nutshell

$$I_D = I_S\left[i_f - i_r\right] \qquad \text{where} \qquad I_S = \mu C_{ox} n \frac{\phi_t^2}{2}\frac{W}{L} = I_{SH}\frac{W}{L}$$

$$\frac{V_P - V_{S(D)B}}{\phi_t} = \sqrt{1+i_{f(r)}} - 2 + \ln\left(\sqrt{1+i_{f(r)}} - 1\right) \qquad V_P \cong \frac{V_{GB} - V_{T0}}{n}$$

DC eqs

If we choose $i_f = 3$ $\Longrightarrow$ $RHS = 0$ $\Longrightarrow$ $V_{GB} = \boldsymbol{V_{T0}}$

$$\frac{V_{DS}}{\phi_t} = \sqrt{1+i_f} - \sqrt{1+i_r} + \ln\left(\frac{\sqrt{1+i_f} - 1}{\sqrt{1+i_r} - 1}\right)$$

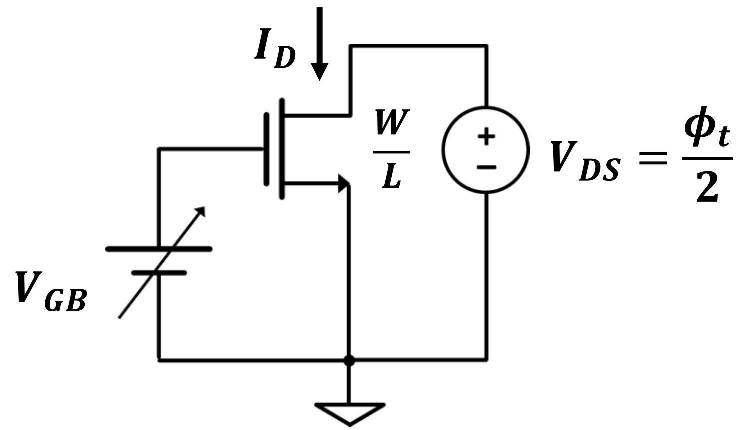
$$g_{ms(d)} = \frac{2I_S}{\phi_t}\left(\sqrt{1+i_{f(r)}} - 1\right) \Longrightarrow \frac{W}{L} = \frac{g_{ms(d)}\phi_t}{2I_{SH}\left(\sqrt{1+i_{f(r)}} - 1\right)}$$

$$g_m = \frac{g_{ms} - g_{md}}{n} \qquad \frac{g_m}{I_D} = \frac{d(\ln I_D)}{dV_G} = \frac{2}{n\phi_t\left(\sqrt{1+i_f} + \sqrt{1+i_r}\right)}$$

Small –signal eqs

I_S, V_{T0} and n extraction

The g_m/I_D method



Let us choose: $V_{DS} = {}^{\phi_t}/_2$ and $i_f = 3$

$$\frac{V_{DS}}{\phi_t} = \sqrt{1+i_f} - \sqrt{1+i_r} + \ln\left(\frac{\sqrt{1+i_f}-1}{\sqrt{1+i_r}-1}\right)$$

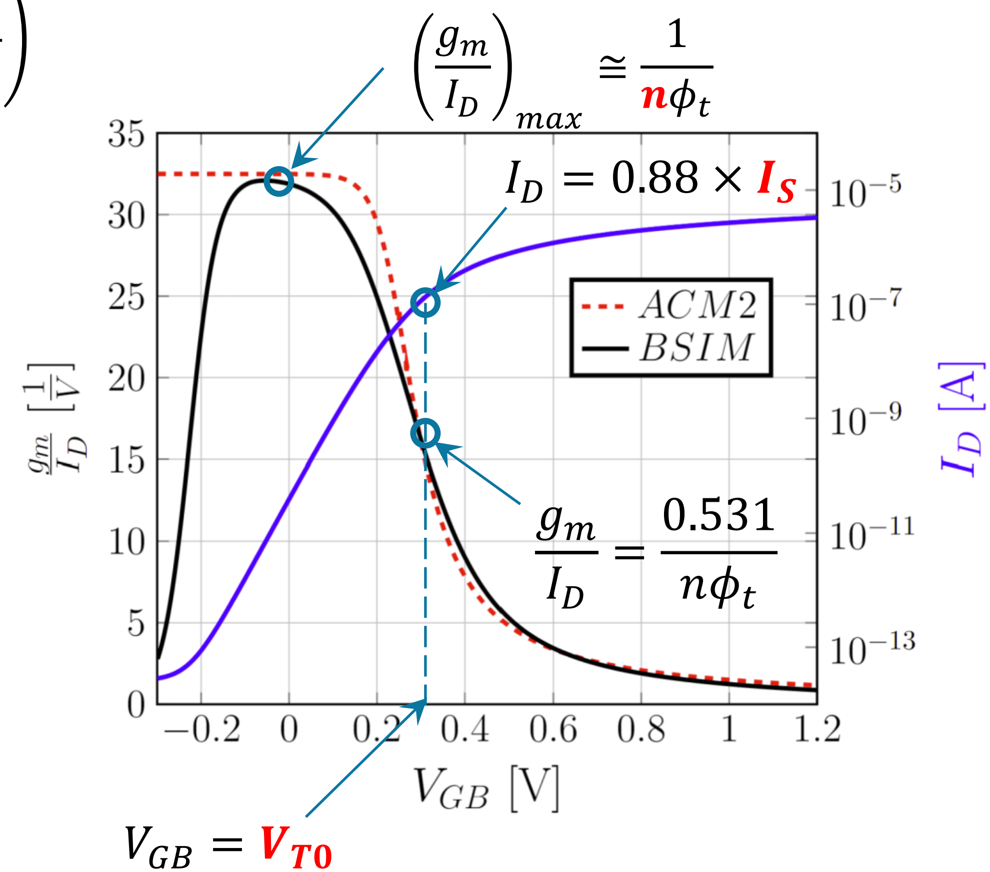
Thus : $i_r = 2.12$

$$\frac{g_m}{I_D} = \frac{d(\ln I_D)}{dV_G} = \frac{2}{n\phi_t\left(\sqrt{1+i_f}+\sqrt{1+i_r}\right)}$$

$$\boxed{\frac{g_m}{I_D} = \frac{0.531}{n\phi_t} = 0.531\left(\frac{g_m}{I_D}\right)_{max}}$$

$$I_D = I_S(i_f - i_r)$$

$$\boxed{I_D = (3-2.12)\,I_S = 0.88\,I_S}$$



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ACM2 : Transconductances in saturation

$$I_{Dsat} = \frac{2I_S}{\zeta} q_{dsat} \quad \text{where} \quad \begin{cases} I_S = \mu C_{ox} n \dfrac{\phi_t^2}{2} \dfrac{W}{L} = I_{SH} \dfrac{W}{L} \\ q_{dsat} = q_s + 1 + \dfrac{1}{\zeta} - \sqrt{\left(1 + \dfrac{1}{\zeta}\right)^2 + \dfrac{2q_s}{\zeta}} \end{cases}$$

Definitions

$$g_m \triangleq \frac{\partial I_{Dsat}}{\partial V_G} \qquad g_d \triangleq \frac{\partial I_{Dsat}}{\partial V_D} \qquad g_{msat3} \triangleq \frac{\partial^3 I_{Dsat}}{\partial V_G^3}$$

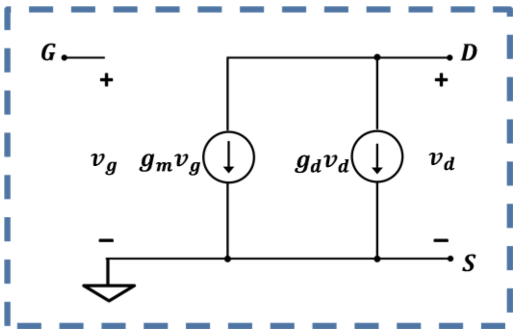
Transconductances in terms of q_s:

$$g_{msat} = \frac{2I_S}{n\phi_t} \frac{q_s}{1 + \zeta(q_s + 1)} \qquad g_{dsat} = \sigma \frac{2I_S}{n\phi_t} \frac{q_s}{1 + \zeta(q_s + 1)} \Rightarrow g_{dsat} = \sigma g_{msat}$$

$$g_{msat3} = \frac{16 I_S}{(n\phi_t)^3} \frac{q_s}{(q_s + 1)^3} \frac{2 - 2\zeta q_s - 3\zeta q_s^2}{(\zeta q_s + 2)^4}$$

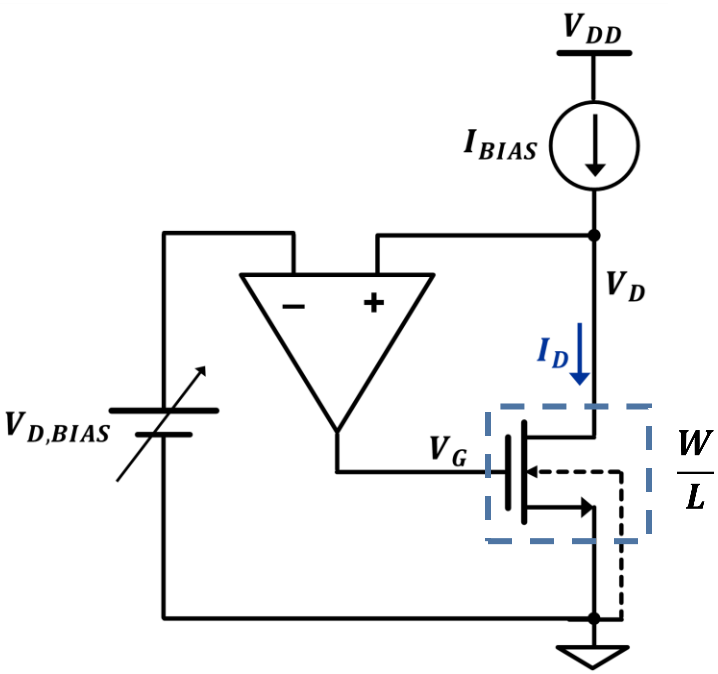
Extraction of σ

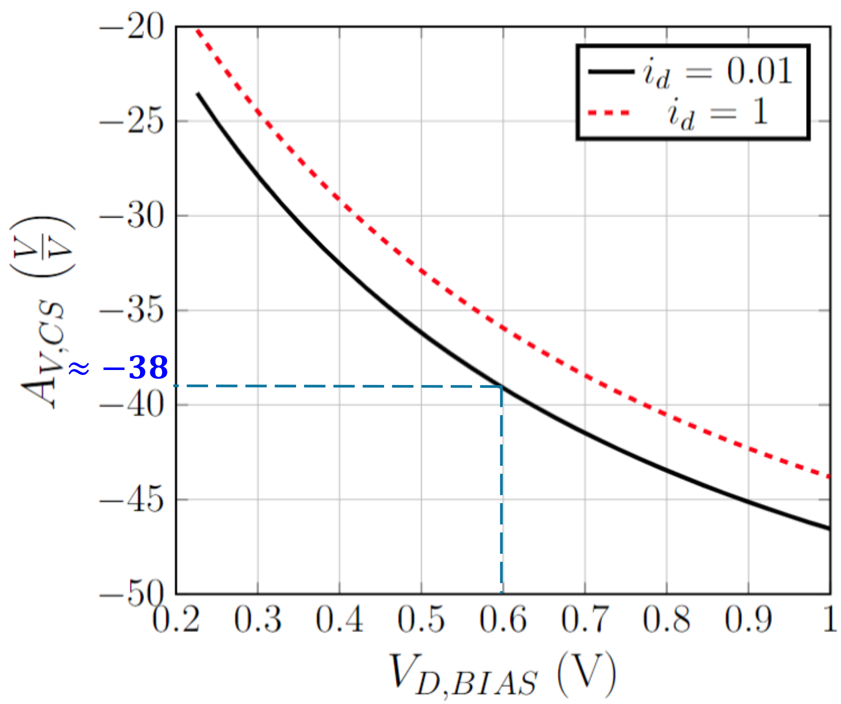
Common-Source Intrinsic-Gain method



In saturation : $g_{dsat} = \boldsymbol{\sigma} g_{msat}$

$$A_{V,CS} = \frac{\Delta v_D}{\Delta v_G} = -\frac{g_{msat}}{g_{dsat}} = \frac{\frac{\partial I_{Dsat}}{\partial V_G}}{\frac{\partial I_{Dsat}}{\partial V_D}} = -\frac{\frac{2I_S}{n\phi_t}\frac{q_s}{1+\zeta(q_s+1)}}{\sigma\frac{2I_S}{n\phi_t}\frac{q_s}{1+\zeta(q_s+1)}} = -\frac{1}{\sigma}$$





Example:

$$A_{V,CS} = -\frac{1}{\sigma}$$

$$\sigma = -\frac{1}{(-38)}$$

$$\boxed{\sigma = 0.026}$$

ζ extraction

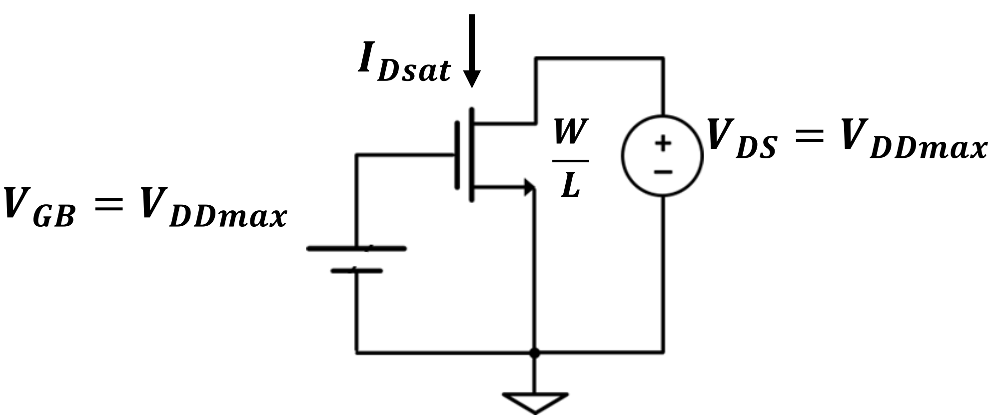
$$i_{dsat} = \frac{2}{\zeta} q_{dsat} \qquad q_s = \sqrt{1 + \frac{2}{\zeta} q_{dsat}} - 1 + q_{dsat}$$

$$\boxed{\zeta = \frac{2\left(q_s + 1 - \sqrt{1 + i_{dsat}}\right)}{i_{dsat}}}$$

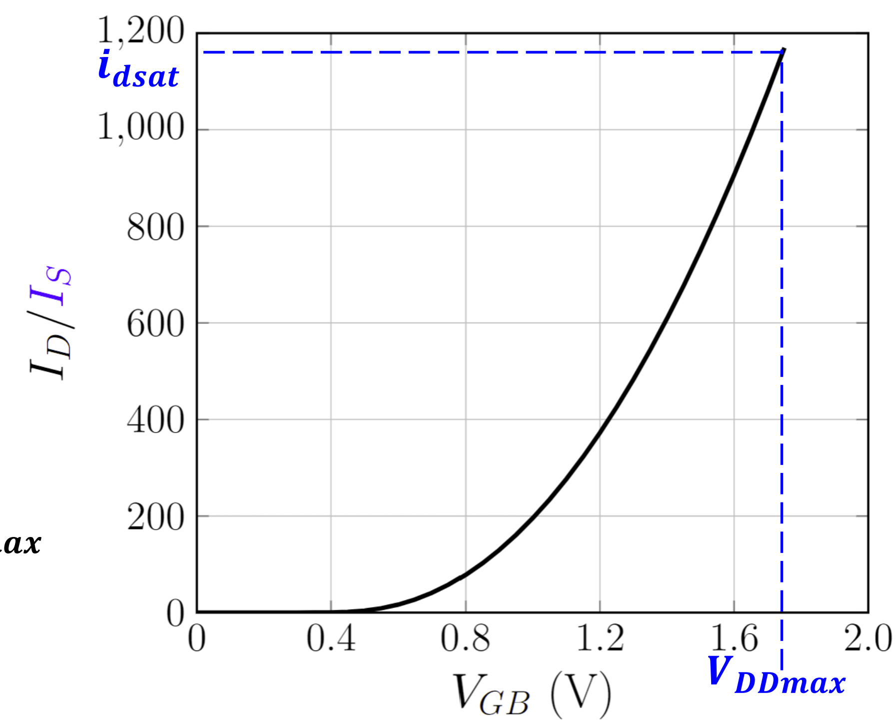
- q_s calculated using parameters ($\boldsymbol{V_{T0}}$, $\boldsymbol{n}$, $\boldsymbol{\sigma}$) and UCCM.

$$V_P = \frac{V_{GB} - \boldsymbol{V_{T0}} + \boldsymbol{\sigma}(V_{DB} + V_{SB})}{\boldsymbol{n}}$$

$$\frac{V_P - V_{S(D)B}}{\phi_t} = q_s - 1 + \ln(q_s)$$



- Measure
  $I_{Dsat} = I_D(V_G = V_D = V_{DDmax}$ and $V_S = V_B)$
  $i_{dsat} = I_{Dsat}/I_S$.



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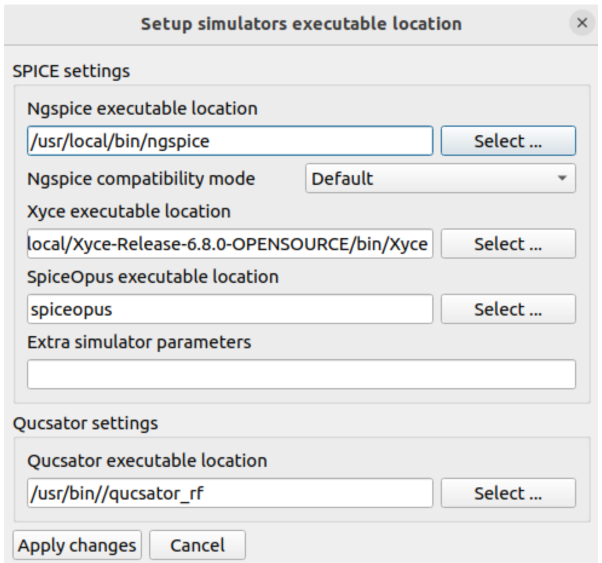
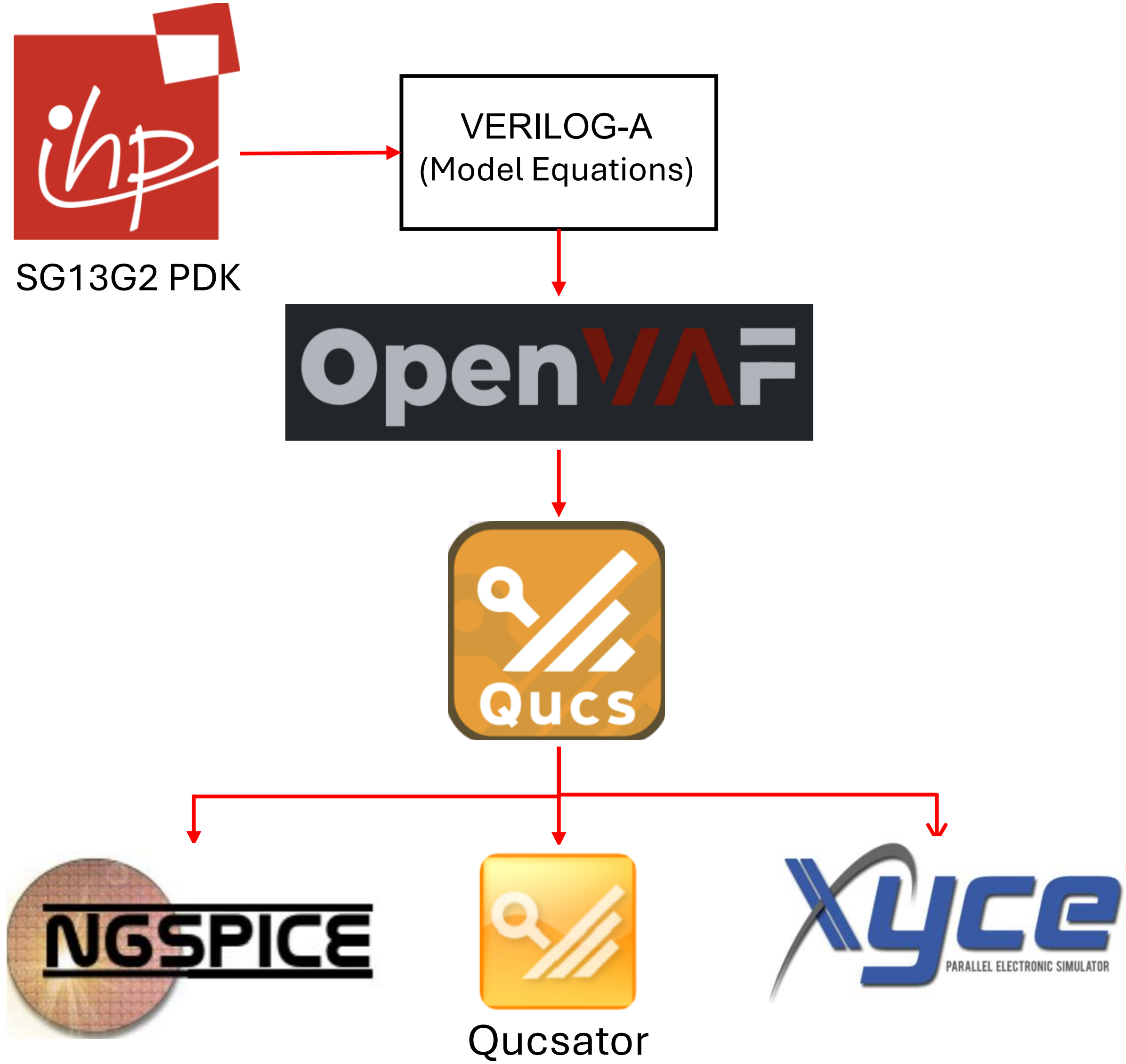
        - VT0, IS and n
        - Sigma & Zeta
    - DC characteristics
    - Transconductances in Saturation
    - Example: Inverter CMOS
- Overview of Open-source environment
    - Automatic parameter extraction

Qucs-S: Quite universal circuit simulator with SPICE

Simulation setup:



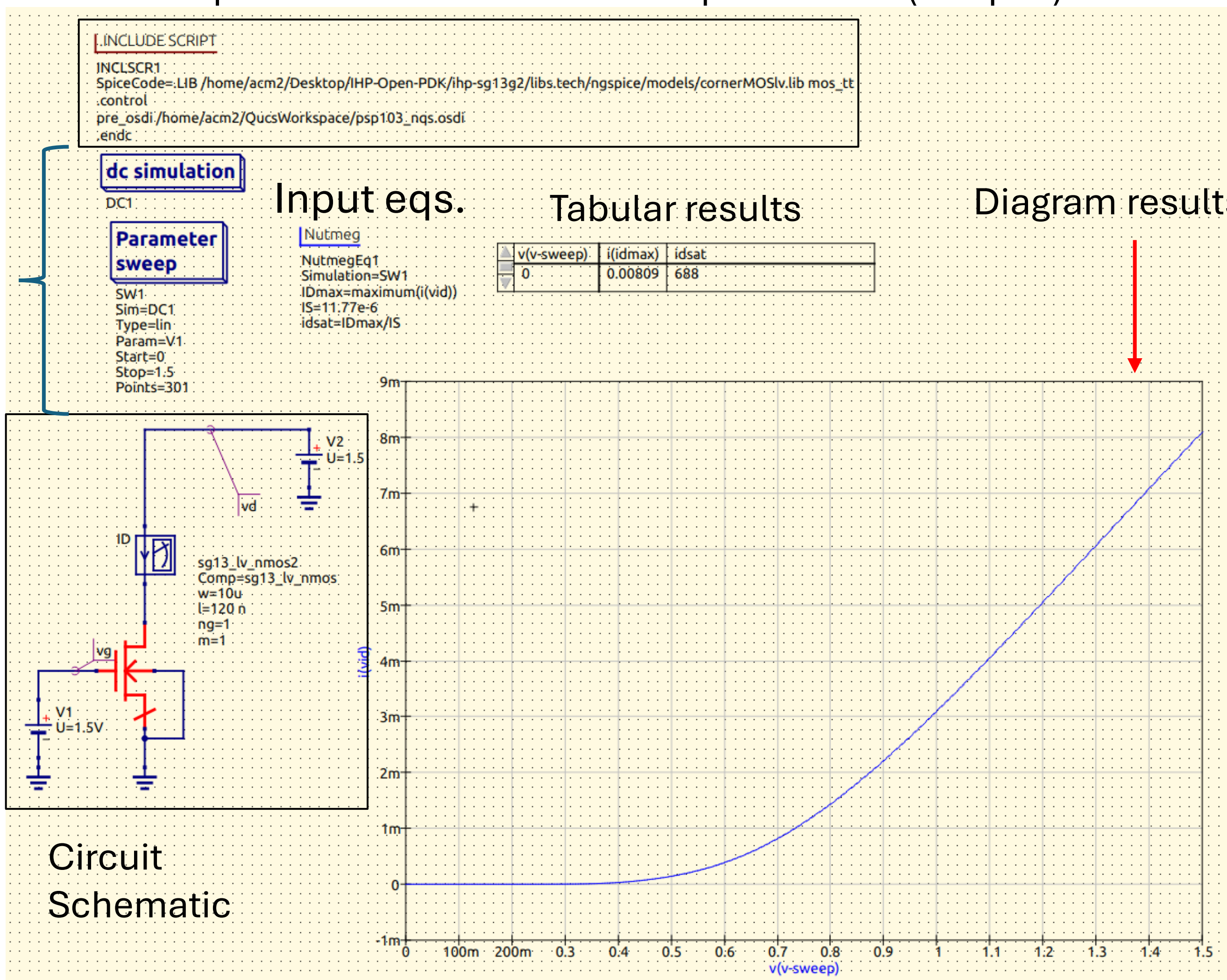


Qucs-S: Quite universal circuit simulator with SPICE

Device path for the MOS model and parameters (IHP pdk)

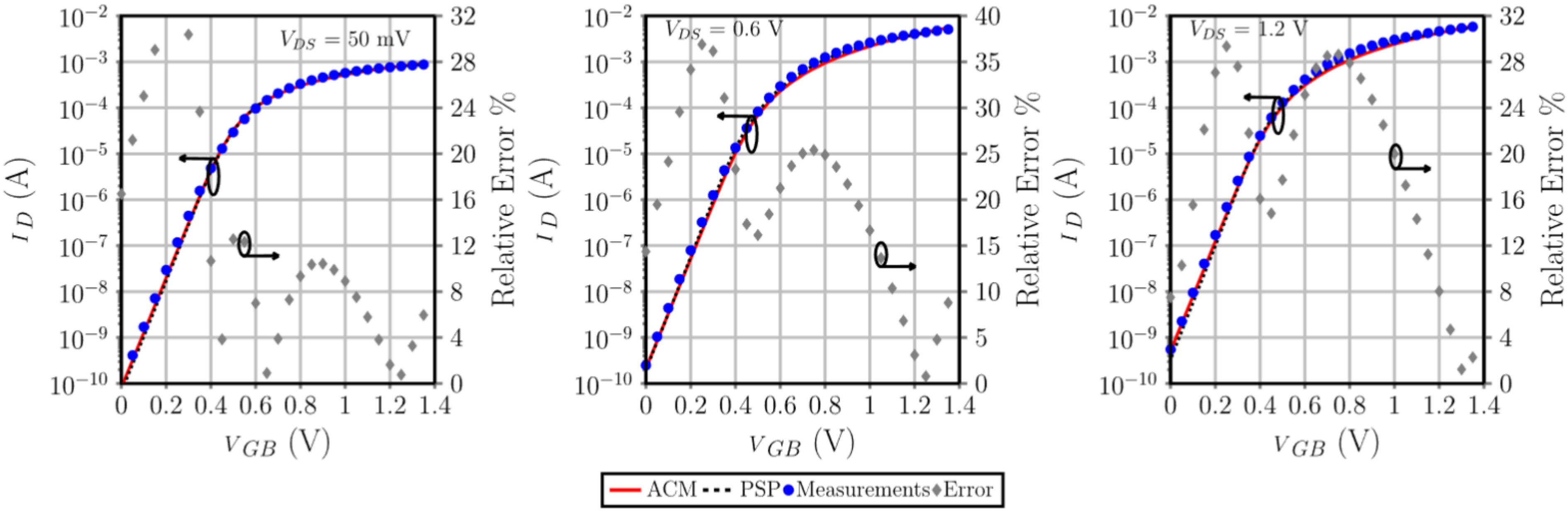
Simulations Control

- Ngspice simulations:
  - DC
  - AC
  - TRAN
  - S-parameters
  - Noise
  - Fourier



ACM2[1] vs PSP – 130 nm SiGe IHP[2]

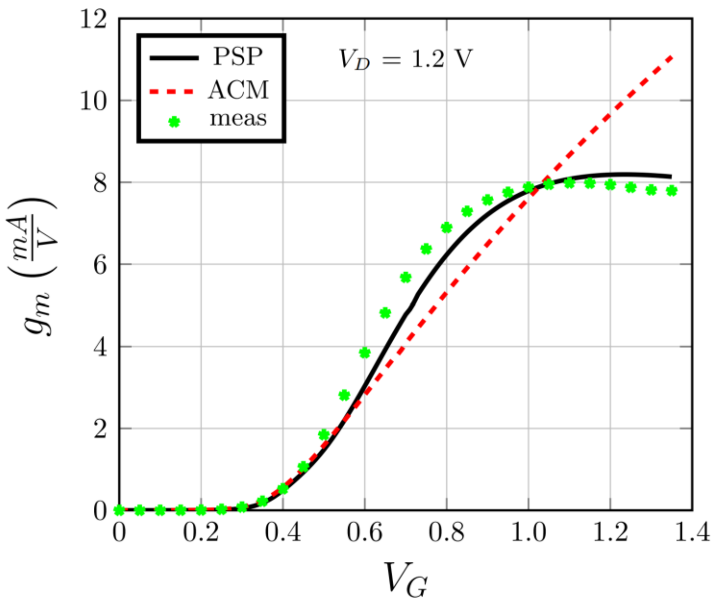
I_D vs V_{GB}

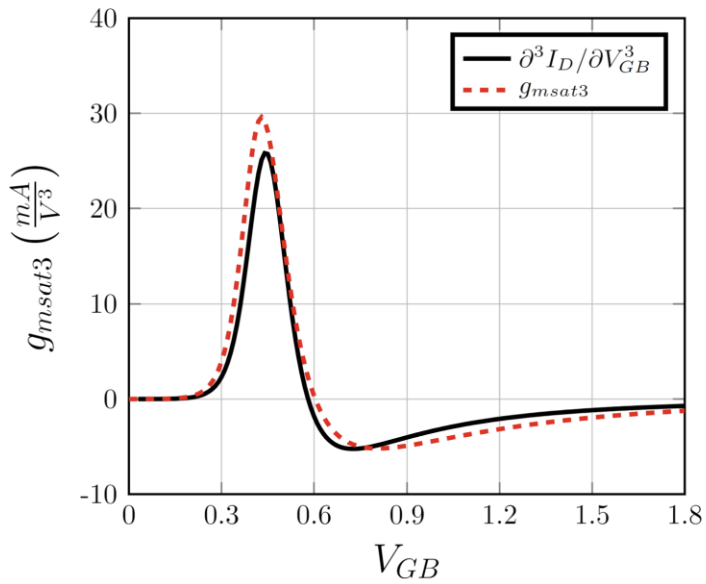


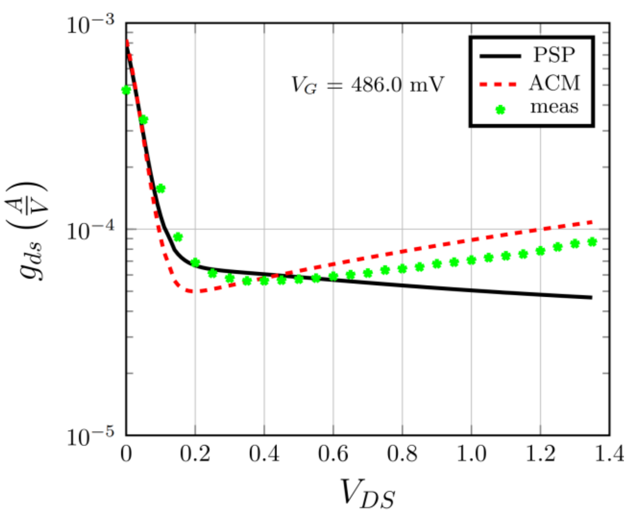
Characteristics of a LVT NMOS bulk transistor with W /L = 10µm/ 120 nm.

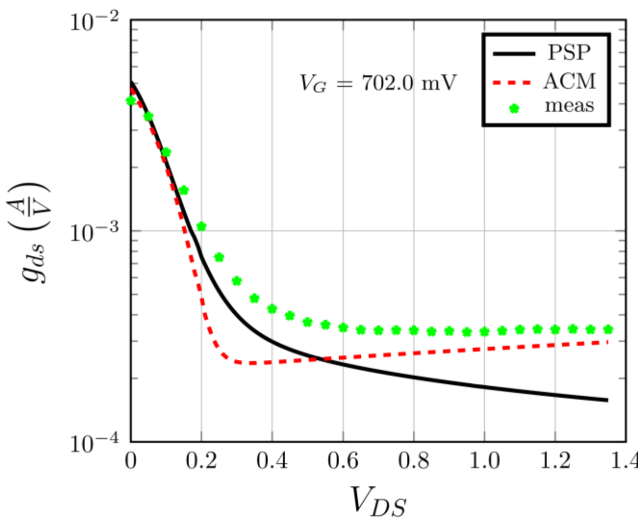
[1] ACM2 : implemented in verilog-A, compiled by OPENVAF, simulated in Ngspice
[2] Institut for High-Performance Microelectronics (IHP) open-source PDK

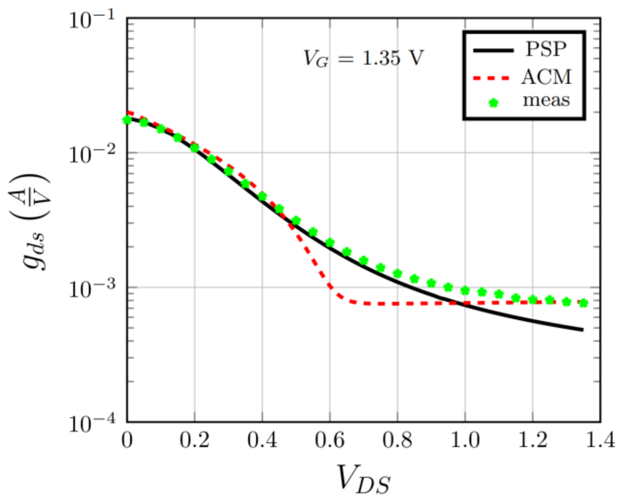
5PM-ACM2 : Transconductance gm, gm3 and gds



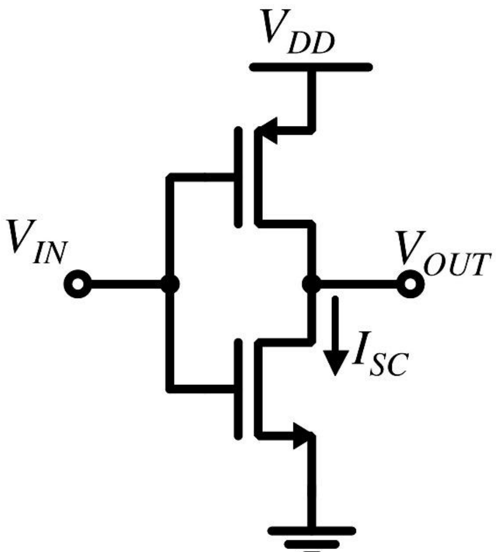


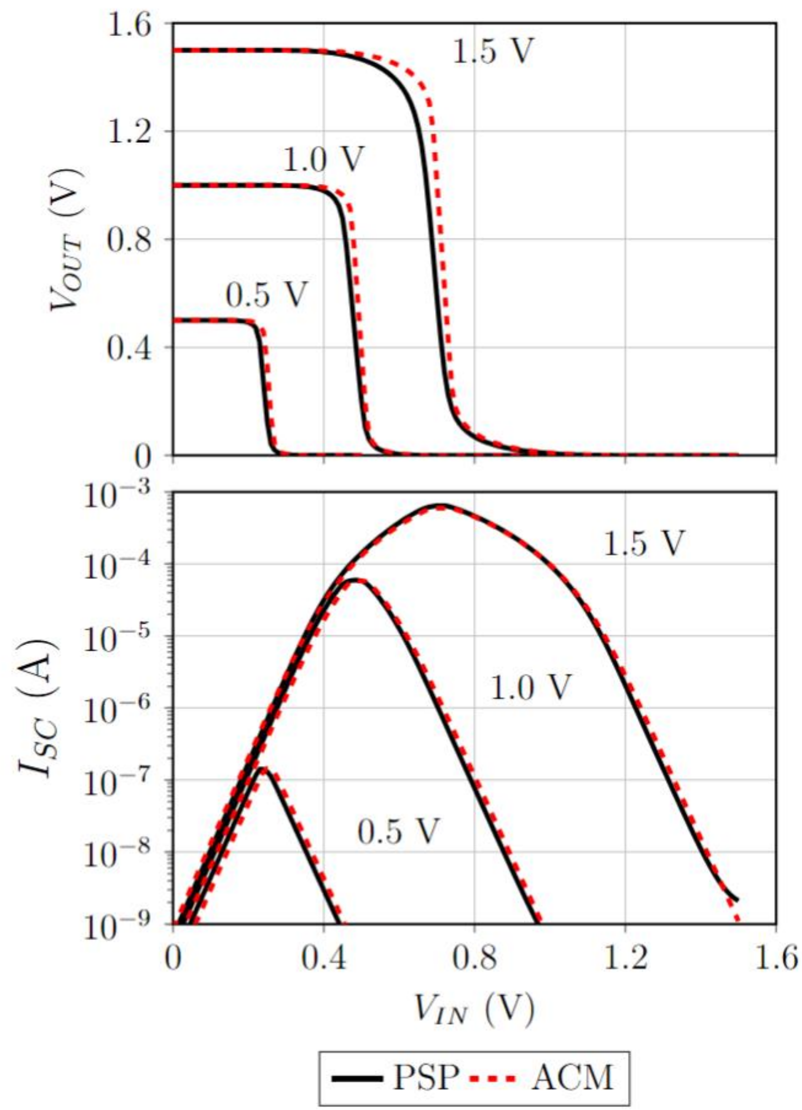




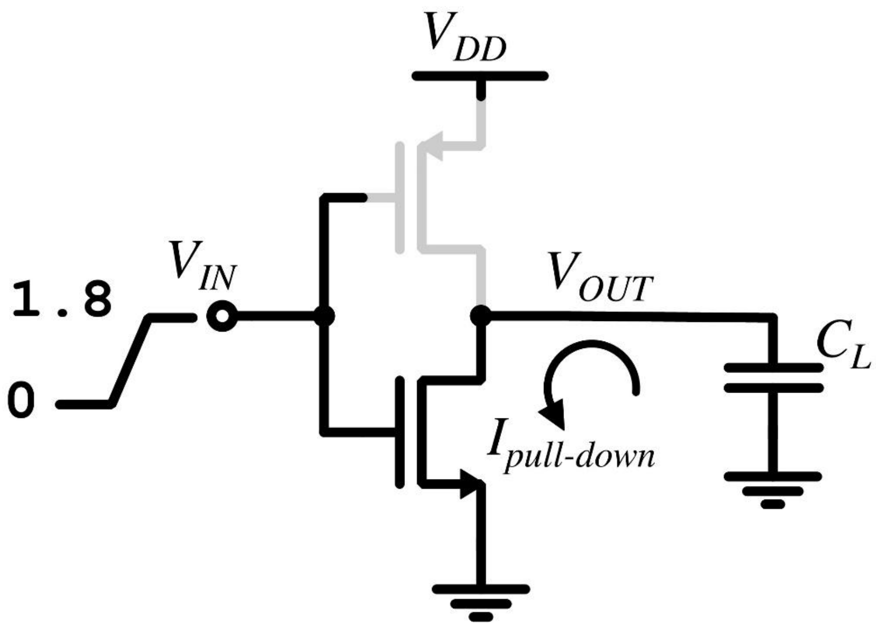


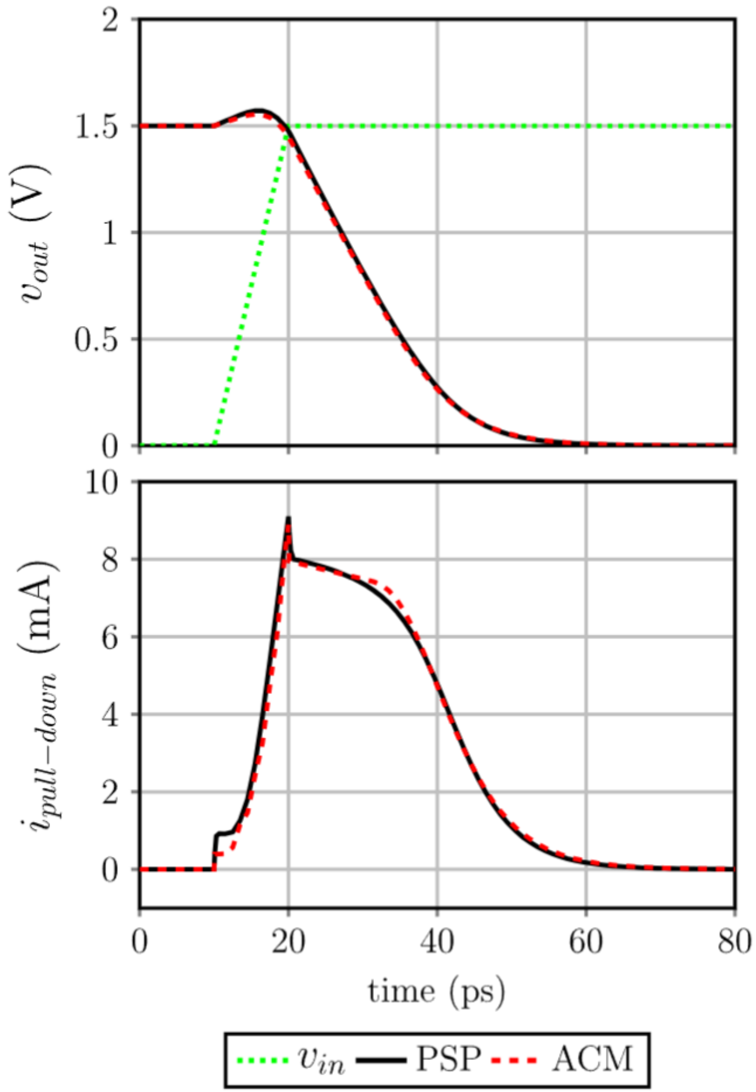
CMOS Inverter in 130 nm bulk
VTC and short-circuit current





CMOS Inverter in 130 nm bulk
Output Voltage and pull-down current





Outline

- ACM2 :
  - Parameter Extraction
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  - Transconductances in Saturation
  - Example: Inverter CMOS
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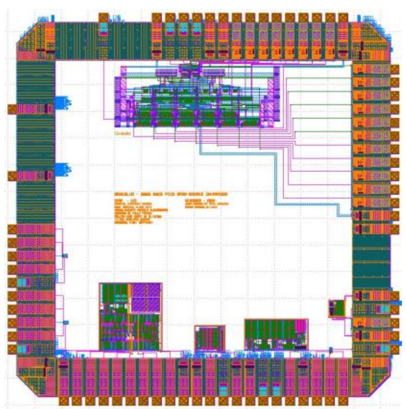
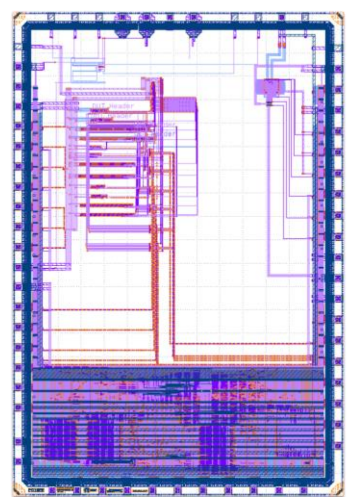
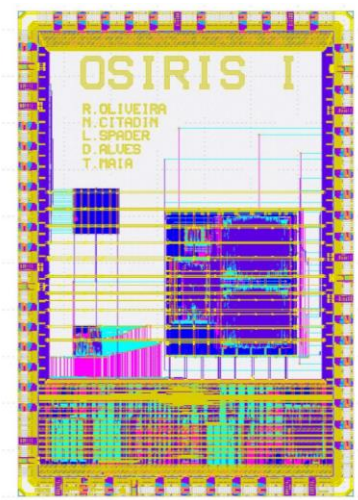
Open-Source IC design

- Chipathon - SSCS 2021 :)
- Analog-front-end for Biosignals – AFEbio
- Chipathon-SSCS 2023 & UNIC-CASS 2023
    - Analog IC design
- Mentor in **Universalization of IC Design from CASS (UNIC-CASS)** 2024

ODIN







Open-Source **D**esign of **I**ntegrated **N**etworks

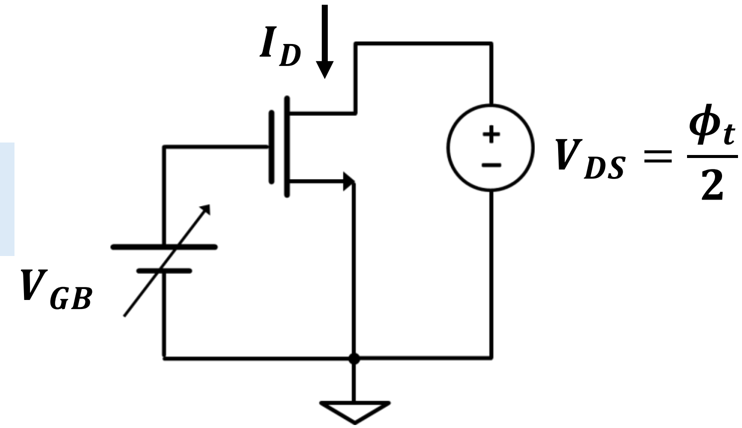
Let's go to Qucs-S!

Useful links:

- Qucs-S oficial page: https://ra3xdh.github.io/
- Qucs-S iterative doc: https://qucs-s-help.readthedocs.io/
- Ngspice oficial page : https://ngspice.sourceforge.io/index.html
- Google Colab: ACM2 & LNA design:
  https://colab.research.google.com/drive/1s3PKF6pf3zIhlTj6jc-qhCLIcGfJ_UEE?usp=sharing

I_{S0}, V_{T0} and n extraction

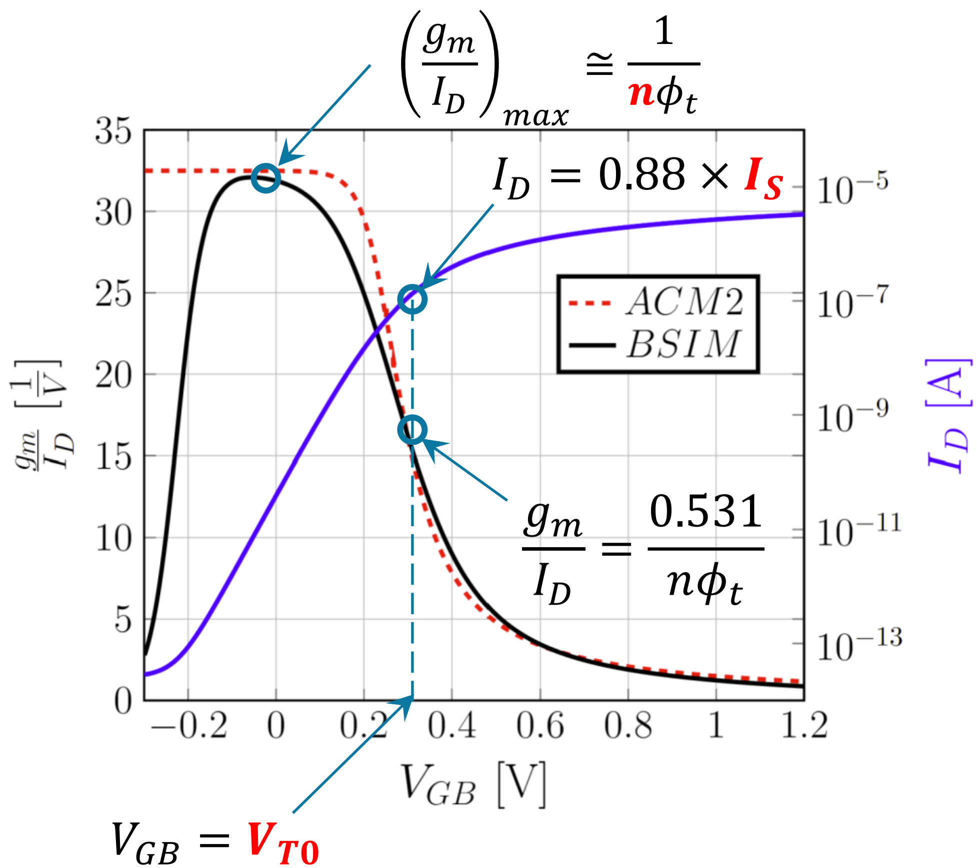
The g_m/I_D method



We identify the $\left.\frac{g_m}{I_D}\right|_{max}$ → n

We calculate $0.531\left.\frac{g_m}{I_D}\right|_{max}$ → V_{T0}

We read the value of I_D → I_S



Practical part → Go to QuCS !

Github – ACM2

“Scan me”

Github - Content

ACMmodel Merge pull request #26 from gabrielmaranhao/main — 71ee7cd · 6 months ago

Examples	Update SKY130 and GF180 using ACM examples on xschem
Verilog-A	Update PMOS_ACM_2V0.va
docs	Delete 5PM_NewCAS.pdf
LICENSE	Update LICENSE
README.md	Update README.md

README   ECL-2.0 license

Advanced Compact MOSFET model (ACM)

ACM is a simple MOSFET model to design and simulate Analog, Mixed-Signal, and RF circuits

Verilog-A code Available!

MOSFET_model / Verilog-A / NMOS_ACM_2V0.va

ACMmodel Update NMOS_ACM_2V0.va

Code   Blame   291 lines (245 loc) · 12.3 KB

```
//***************************************************************************
// *  ACM NMOS model (Verilog-A)                                            *
// *  07/2023    V2.0.0                                                     *
//***************************************************************************

// **************************************************************************
// * Copyright under the ECL-2.0 license                                    *
// * Universidade Federal de Santa Catarina                                 *
// *                                                                        *
// * Current developers:  Deni Germano Alves Neto (Doctoral student, UFSC)  *
// *                      Cristina Missel Adornes (Doctoral student, UFSC)  *
// *                      Gabriel Maranhao        (Doctoral student, UFSC)  *
// *                                                                        *
// * Project Supervisors:  Prof. Carlos Galup-Montoro                       *
// *                       Prof. Marcio Cherem Schneider                    *
// **************************************************************************

`include "constants.vams"
`include "disciplines.vams"

// function of the algorithm 443 to calculate de normalize charge densities
`define algo_443(Z,qn) \
        if(Z < 0.7385) begin \
                numeratorD = Z + (4.0/3.0)*Z*Z; \
                denominatorD = 1.0 + (7.0/3.0)*Z+(5.0/6.0)*Z*Z; \
                WnD = numeratorD/denominatorD; \
        end     else begin \
                numeratorD = ln(Z)*ln(Z)+2.0*ln(Z)-3.0; \
                denominatorD = 7.0*ln(Z)*ln(Z) + 58.0*ln(Z) +127.0; \
                WnD = ln(Z) - 24.0*(numeratorD/denominatorD); \
```

Examples of PDKs and circuit simulators using the ACM model

NGSPICE & XSCHEM:
- GF180MCU
- IHP-SG13
- SkyWater130

Qucs:
- IHP-SG13

Part 3
Analog IC design

“Scan me”

Márcio Cherem Schneider

https://github.com/ACMmodel/MOSFET_model

Outline

Analog circuit design

1. Current mirrors
2. High-swing cascode current mirror
3. Current gain schemes
4. Current and voltage references
5. Single-stage amplifiers

ACM2 applied to weak inversion

ACM2 parameters: V_{T0}, I_S, n, σ, ζ

$$q_{S(D)} = Q_{S(D)}/(-nC_{ox}\phi_t)$$

$$q_{S(D)} = e^{\left(\frac{V_P - V_{S(D)B}}{\phi_t}+1\right)}$$

UCCM

$$I_D/I_S = i_f - i_r = (I_F - I_R)/I_S$$

$$V_P = \frac{V_{GB} - \left(V_{T0} - \sigma(V_{DB} + V_{SB})\right)}{n}$$

$$\boxed{i_D = I_D/I_S = 2(q_S - q_D)}$$

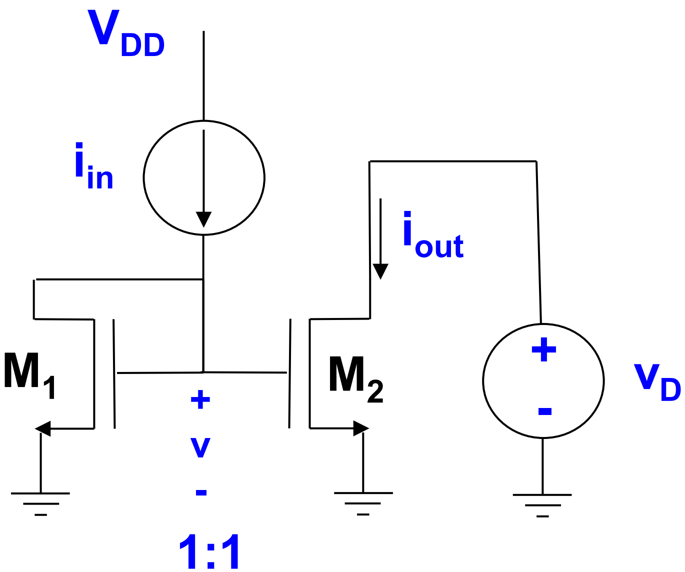
$$\boxed{I_S = \frac{W}{L}\mu_s n C_{ox}\frac{\phi_t^2}{2} = S I_{SH}}$$

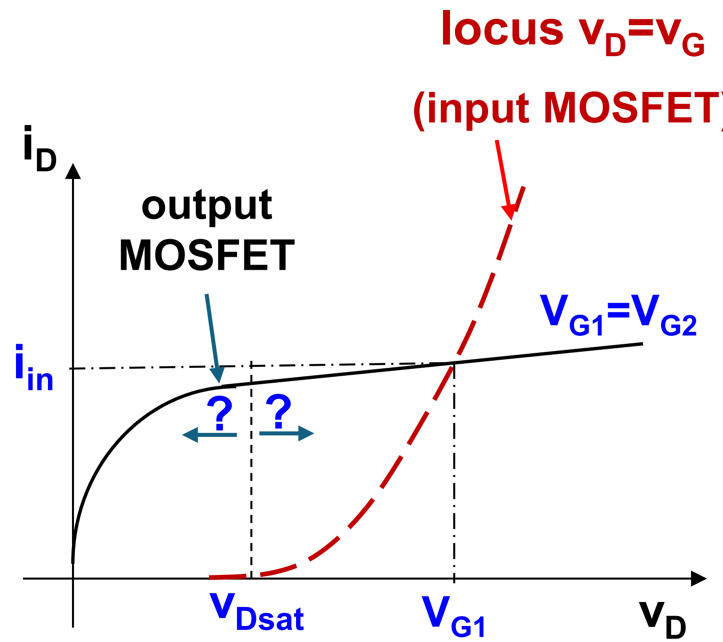
normalization (specific) current

***WI* : $q_{S(D)} \ll 1$**

ratio of diffusion-related velocity to saturation velocity

1. Current mirrors





M_1=M_2

M_1: i→v converter

M_2: v→i converter

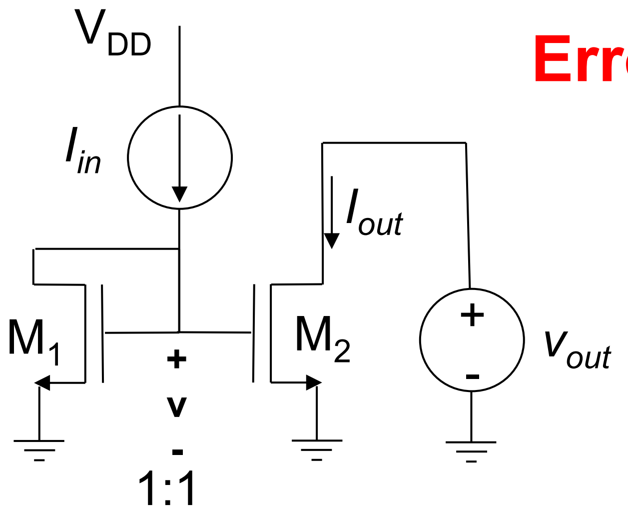
Basic principle $V_{G1}=V_{G2}$; $V_{S1}=V_{S2}$; $V_{B1}=V_{B2}$;
$v_{out}>V_{Dsat} \rightarrow i_{out} \cong i_{in}$

What's this saturation voltage V_{Dsat}? No clear definition.

An approximation for the saturation voltage:

$$\boxed{V_{DSsat} \cong \phi_t\left(\sqrt{1+i_f}+3\right)}$$

1. Current mirrors



Error due to difference in drain voltages

V_A is non-physical

A simple case: error for weak inversion using ACM2

$$I_{in} = I_{F1} - I_{R1} = I_{F1}\left[1 - e^{-V_{in}/\varphi_t}\right]$$

$$I_{out} = I_{F2} - I_{R2} = I_{F2}\left[1 - e^{-V_{out}/\varphi_t}\right]$$

$$I_{F2} = I_{F1} e^{\sigma(V_{out}-V_{in})/n\varphi_t}$$

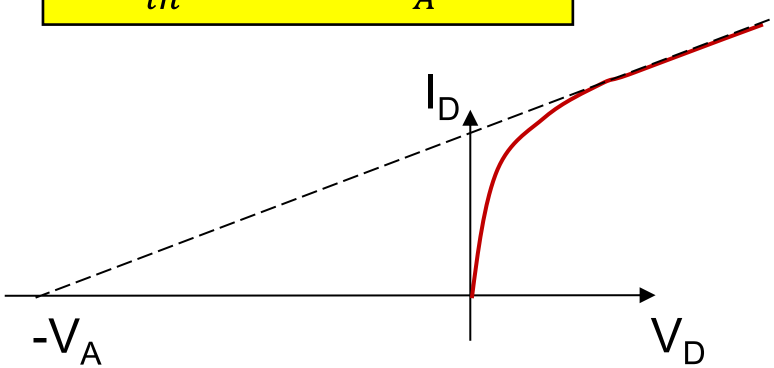
$$\frac{I_{out}}{I_{in}} = e^{\frac{\sigma(V_{out}-V_{in})}{n\varphi_t}} \frac{1-e^{-V_{out}/\varphi_t}}{1-e^{-V_{in}/\varphi_t}}$$

$$\frac{I_{out}}{I_{in}} \cong e^{\frac{\sigma(V_{out}-V_{in})}{n\varphi_t}} \quad \text{for } V_{out} \,\&\, V_{in} \gg \varphi_t$$

Linear approximation

$$\frac{I_{out}}{I_{in}} = \frac{I_S f(V_G - V_T, V_S)(1 + V_{out}/V_A)}{I_S f(V_G - V_T, V_S)(1 + V_{in}/V_A)}$$

$$\frac{I_{out} - I_{in}}{I_{in}} \cong \frac{V_{out} - V_{in}}{V_A}$$



1. Current mirrors

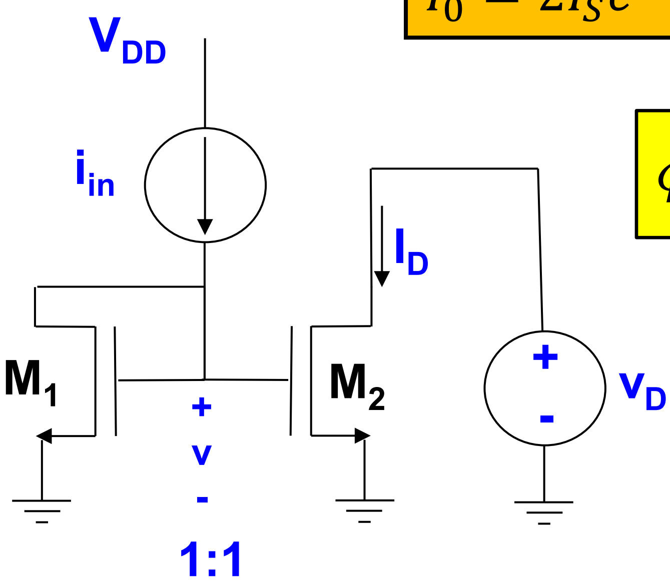
Dependence of the output current (conductance) on the output voltage

Weak inversion
i_f<1

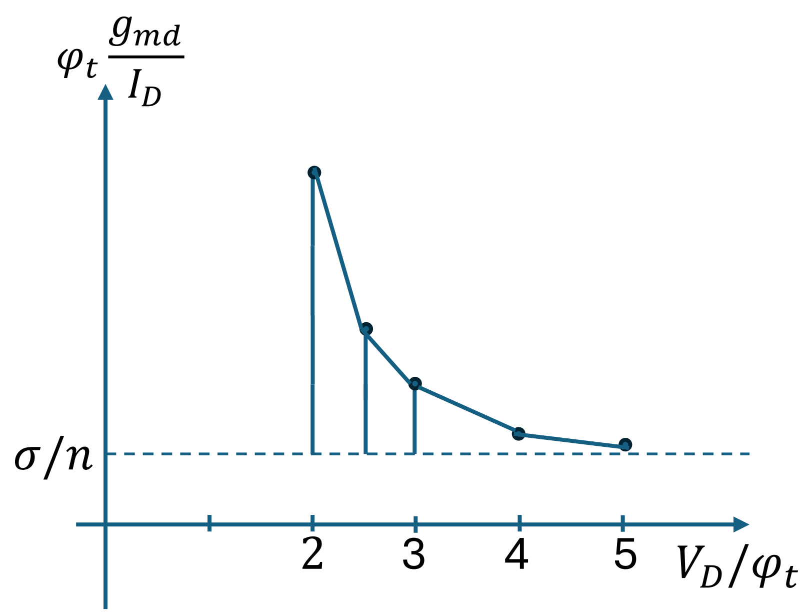
$$I_D = \underbrace{I_0 e^{\left(\frac{V_G - V_T}{n}\right)/\varphi_t}}_{I_F}\left[1 - e^{-V_D/\varphi_t}\right] = I_F\left[1 - \frac{I_R}{I_F}\right]$$

$$I_0 = 2 I_S e^1$$

$$V_T \cong V_{T0} - \sigma\left[V_{SB} + V_{DB}\right]$$



$$\varphi_t \frac{g_{md}}{I_D} = \frac{1}{I_D}\frac{dI_D}{dV_D} = \frac{d\ln I_D}{dV_D} = \frac{\sigma}{n} + \frac{I_F}{I_D} e^{-V_D/\varphi_t} \qquad \textbf{(A)}$$

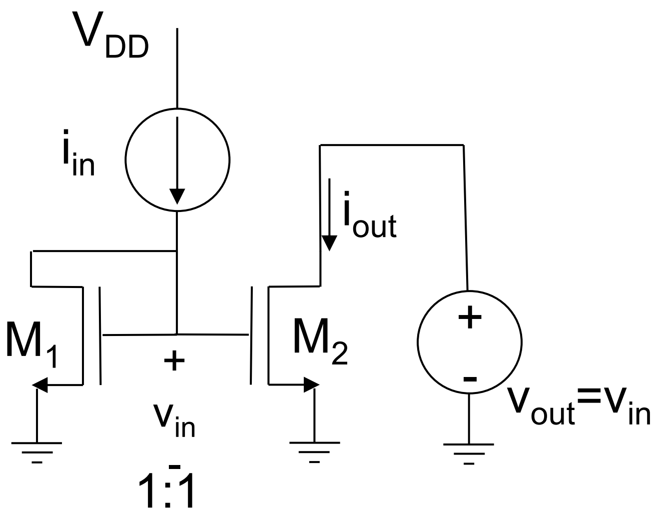


1. Current mirrors

Error due to mismatch

Main contributors to mismatch: I_S & V_T

$$I_D = I_S f(V_G - V_T) \qquad \textbf{(B)}$$



$$\Delta I_D \cong \frac{dI_D}{dI_S}\Delta I_S + \frac{dI_D}{dV_T}\Delta V_T$$

$$\frac{dI_D}{dV_T} = -\frac{dI_D}{dV_G} = -g_m$$

$$\frac{\Delta I_D}{I_D} \approx \frac{\Delta I_S}{I_S} - \frac{g_m}{I_D}\Delta V_T \qquad \textbf{(C)}$$

For uncorrelated mismatch sources

$$\frac{\sigma^2(I_D)}{I_D^2} \approx \frac{\sigma^2(I_S)}{I_S^2} + \left(\frac{g_m}{I_D}\right)^2 \sigma^2(V_T) \qquad \textbf{(D)}$$

Using Pelgrom's model

g_m/I_D

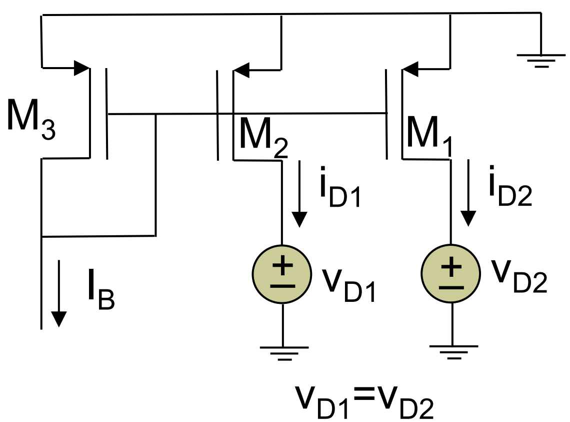
$$\frac{\sigma^2(I_D)}{I_D^2} \approx \frac{2}{WL}\left\{A_\beta^2 + \left(\frac{A_{VT}}{n\phi_t}\right)^2\left[\frac{2}{\left(\sqrt{1+i_f}+1\right)}\right]^2\right\}$$

In general, this is the prevailing term

1. Current mirrors

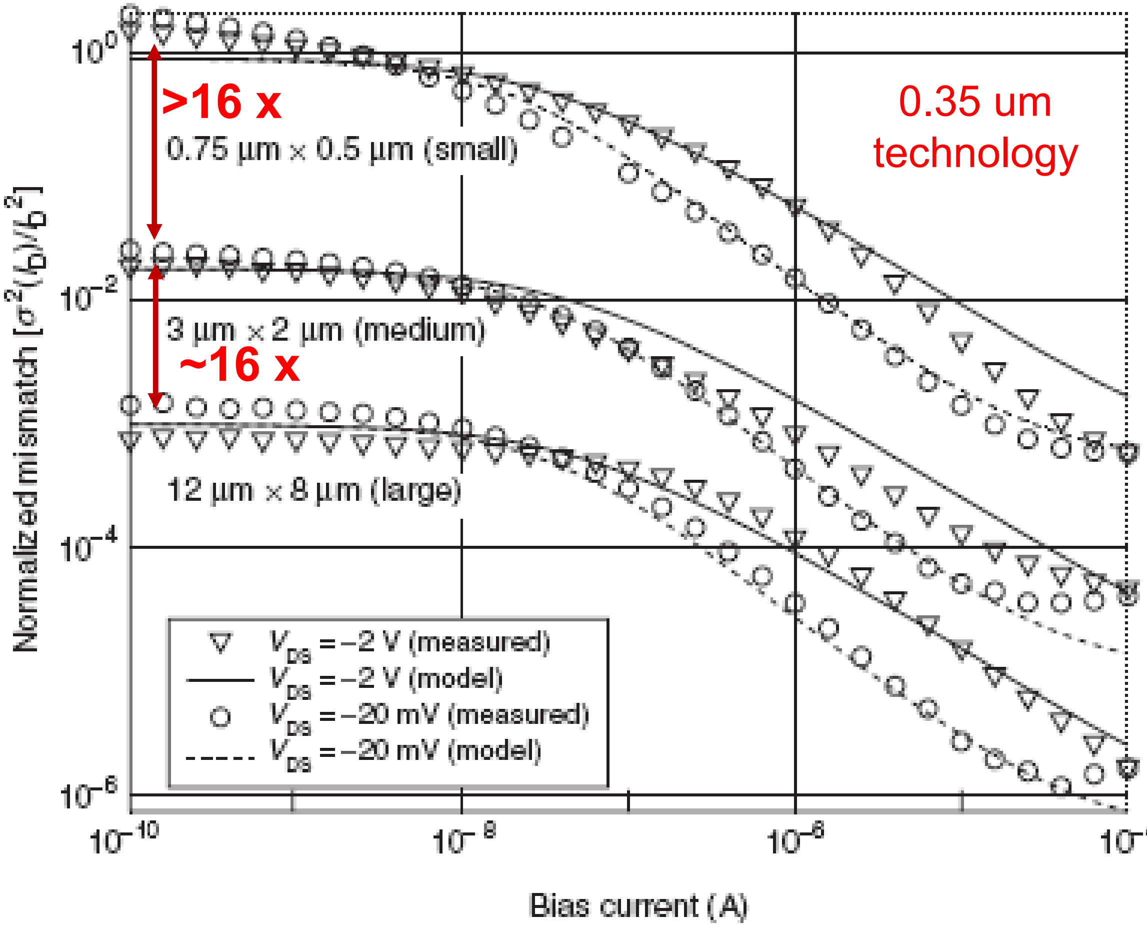
Error due to mismatch

$$\frac{\sigma^2(I_D)}{I_D^2} \approx \frac{2}{WL}\left\{A_{ISH}^2 + \left(\frac{A_{VT}}{n\phi_t}\right)^2 \left[\frac{2}{\left(\sqrt{1+i_f}+1\right)}\right]^2\right\}$$



$$\epsilon_i = \left.\frac{i_{D1}-i_{D2}}{(i_{D1}+i_{D2})/2}\right|_i$$

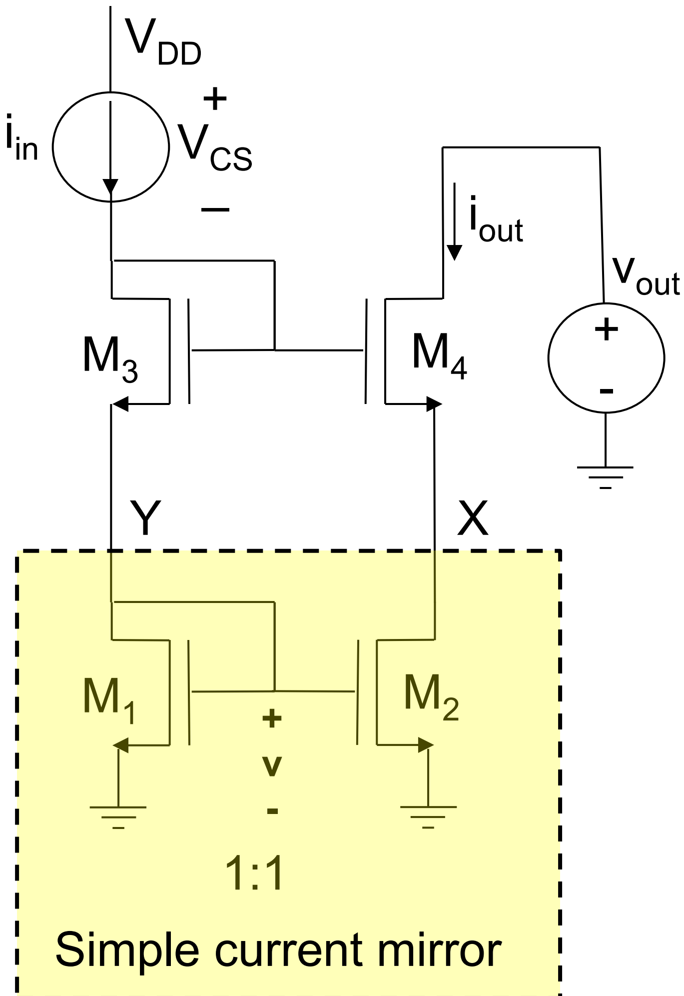
$$\frac{\sigma^2}{I_D^2} = \frac{1}{N}\sum_{i=1}^{N} \varepsilon_i^2$$



Dependence of current matching on inversion level in linear and saturation regions $|V_{DS}|$ = 20 mV and $|V_{DS}|$ = 2 V, respectively, for the large, medium-size, and small PMOS transistor pairs. Statistics determined for 18 pairs of transistors.

2. Cascode current mirrors

Self-biased cascode current mirror (SBCCM)



Assume $M_1 \equiv M_2 \equiv M_3 \equiv M_4$

- If M_4 operates in saturation, then $V_X \cong V_Y$ and $I_{out} \cong I_{in}$
- V_{out} is transferred to V_X with attenuation $\left(\frac{g_{md4}}{g_{ms4}}\right)$ of common-gate gain
- Input constraint: $V_{DD} > V_{CS,min} + V_{GS3} + V_{GS1}$
- Output constraint: $V_{out} > V_{GS1} + V_{DS4,sat}$ for saturation of M_4 (In most cases, $V_{GS} > V_{DS,sat}$)
- The output conductance:

$$y_o = \frac{i_{out}}{v_{out}} \approx g_{md2} \frac{g_{md4}}{g_{ms4}}$$

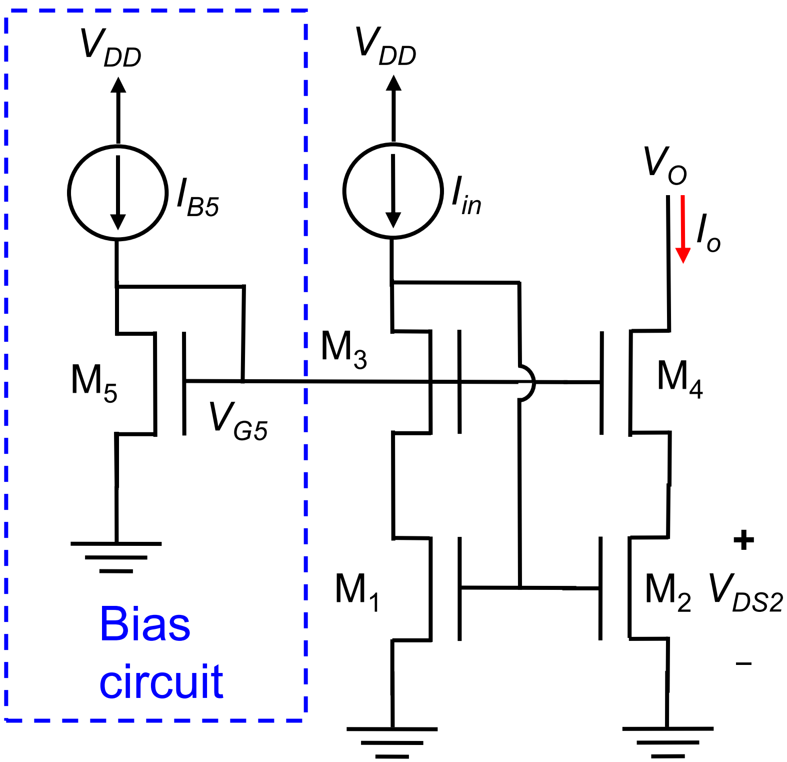
SBCCM is not a low-voltage current mirror

Node X follows approximately node Y

2. Cascode current mirrors

Low-voltage cascode current mirror: lower VDD

Assume $M_1 \equiv M_2 \equiv M_3 \equiv M_4$



Goal: Design V_{G5} to bias M2 (M1) at the edge of saturation

$$V_{S4} = V_{DS2} = V_{DSsat_2} + \Delta V$$

$$f2 = i_{f4} = \frac{I_o}{I_{S4}} \cong \frac{I_{in}}{I_{S4}}$$

$$\Delta V = \alpha \varphi_t$$

$$V_{DSsat} = \varphi_t (\sqrt{1 + i_{f2}} + 3)$$

$$V_{P4} = V_{S4} + \varphi_t \left[\sqrt{1 + i_{f4}} - 2 + \ln\left(\sqrt{1 + i_{f4}} - 1 \right) \right] \quad \text{(I)}$$

$$V_{P5} = \varphi_t \left[\sqrt{1 + i_{f5}} - 2 + \ln\left(\sqrt{1 + i_{f5}} - 1 \right) \right] \quad \text{(II)}$$

Equate (I) to (II) to find i_{f5}

Choose I_{S5} &I_{B5} to comply with $i_{f5} \cong \frac{I_{B5}}{I_{S5}}$

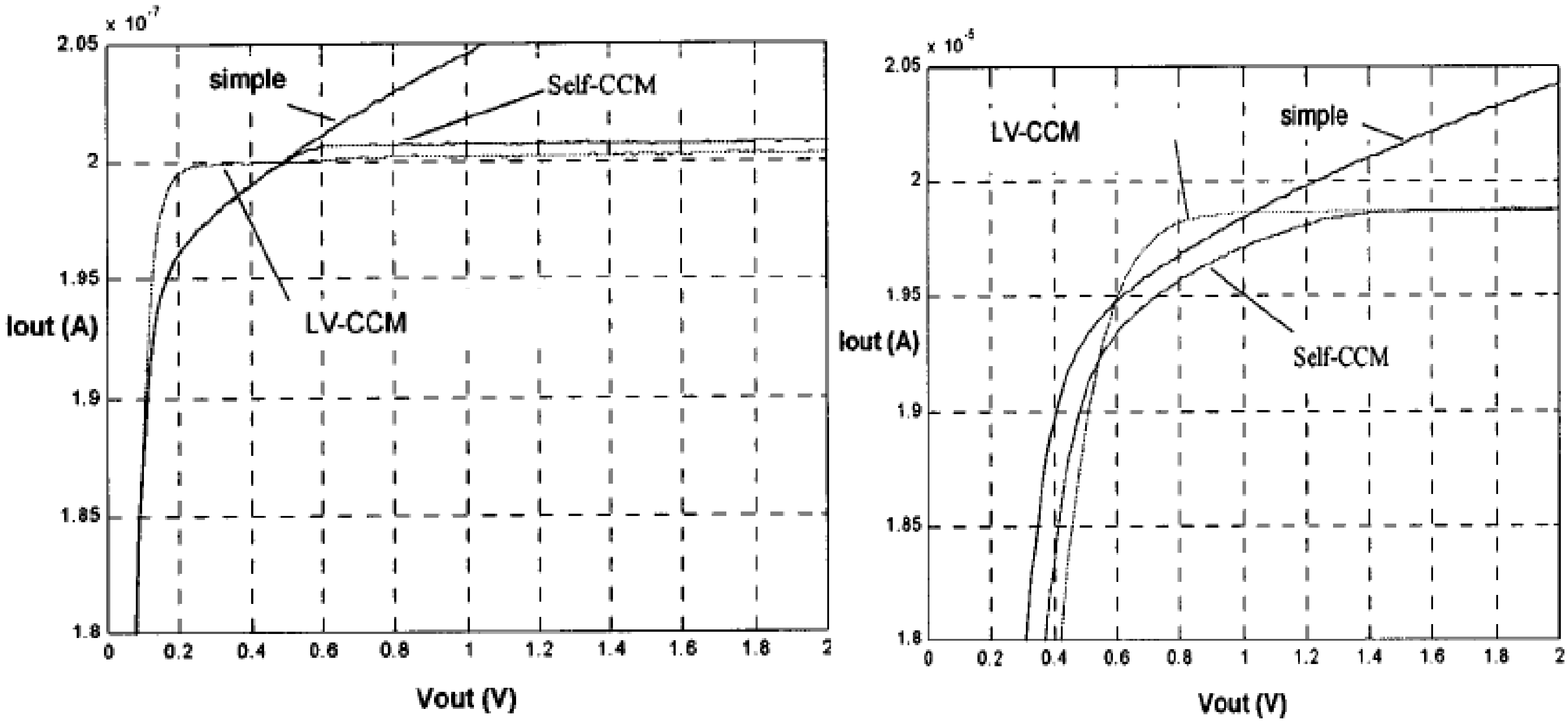
$$I_{S5} = I_{SH} \frac{W}{L}$$

$$y_o = \frac{i_{out}}{v_{out}} \approx g_{md2} \frac{g_{md4}}{g_{ms4}}$$

- Input constraint: $V_{DD} > V_{CS,min} + V_{DS3,sat} + V_{GS1}$
- Output constraint: $V_{out} > V_{DS2,sat} + \Delta V + V_{DS4,sat}$ for saturation of M_4

2. Cascode current mirrors

Low-voltage cascode current mirror - 3



$(i_f = 1)$. $(i_f = 100)$.

Fig. 7. Detail of experimental output characteristics of the current mirrors

2 μm CMOS technology

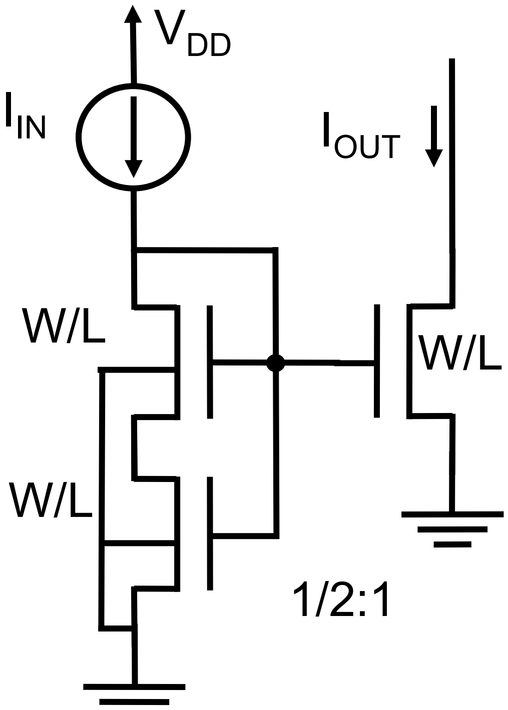
$V_{T0N} \cong 0.55$ V

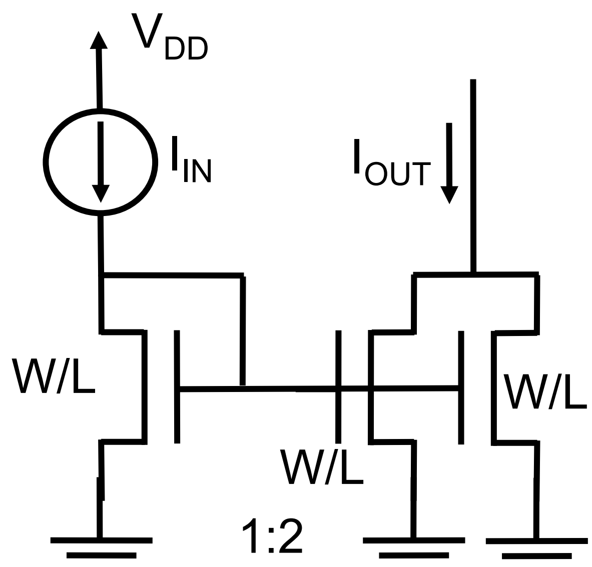
•V. C. Vincence, C. Galup-Montoro and M. C. Schneider, "A high-swing MOS cascode bias circuit," *IEEE Trans. Circuits Syst. II*, vol. 47, no. 11, pp. 1325-1328, Nov. 2000.

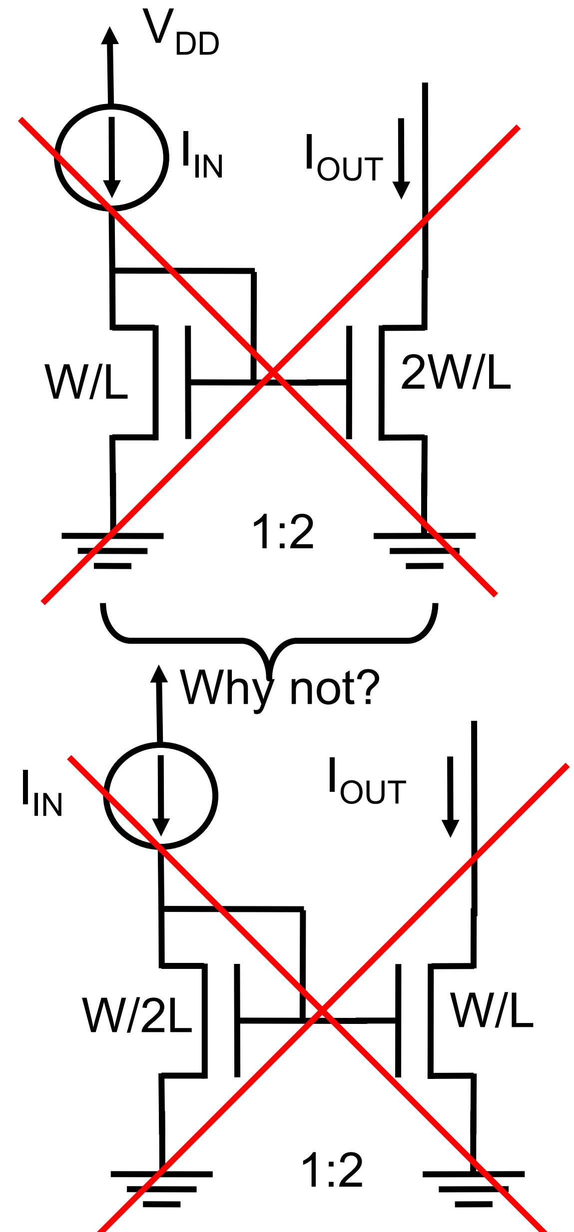
• P. Aguirre and F. Silveira, "Bias circuit design for low-voltage cascode transistors," *Proc. of SBCCI 2006*, pp. 94-98, Sep. 2006.

3. Current gain schemes

Gain-of-2 current mirror



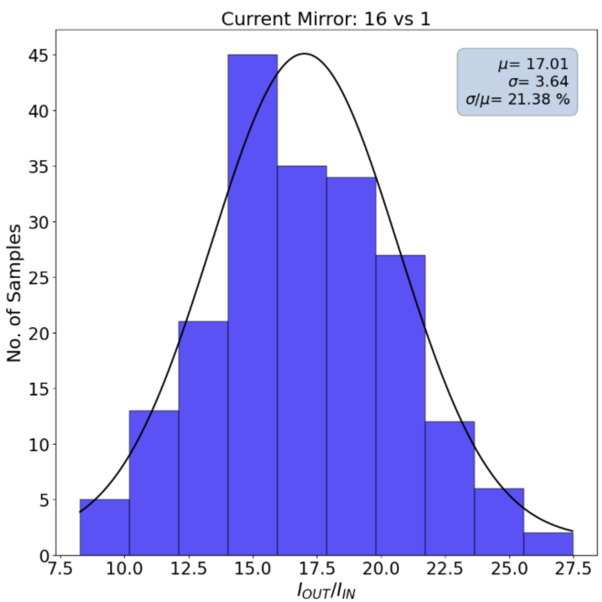


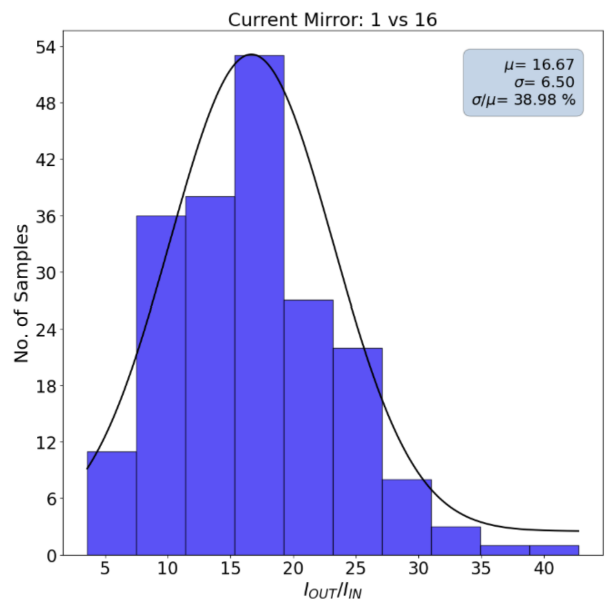


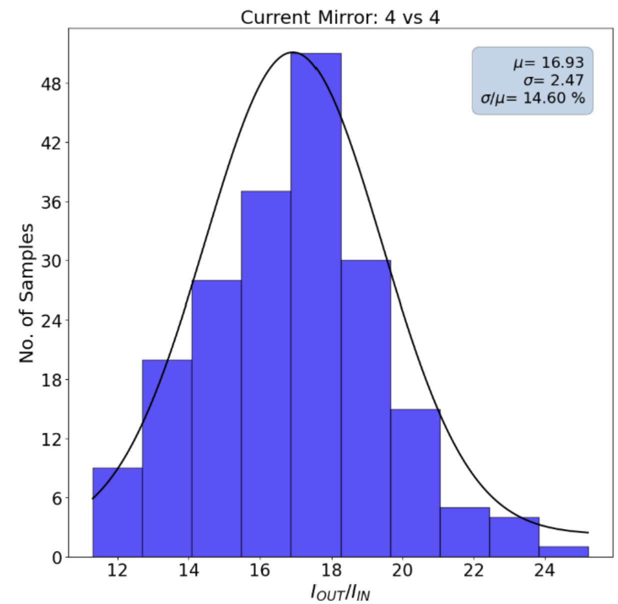
Choose equally-sized components for good matching

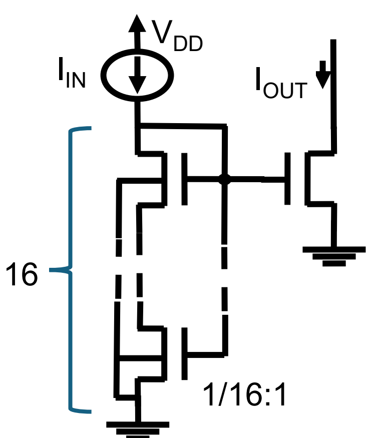
3. Current gain schemes

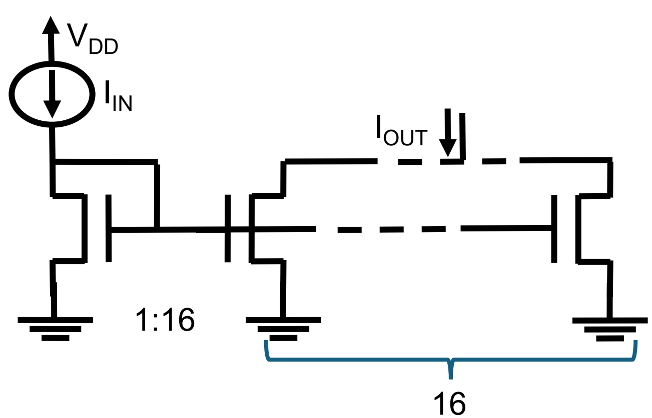
Example: Gain-of-16 current mirror

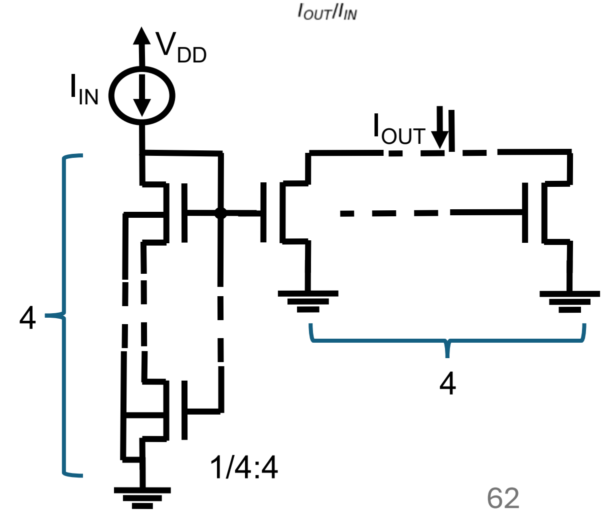








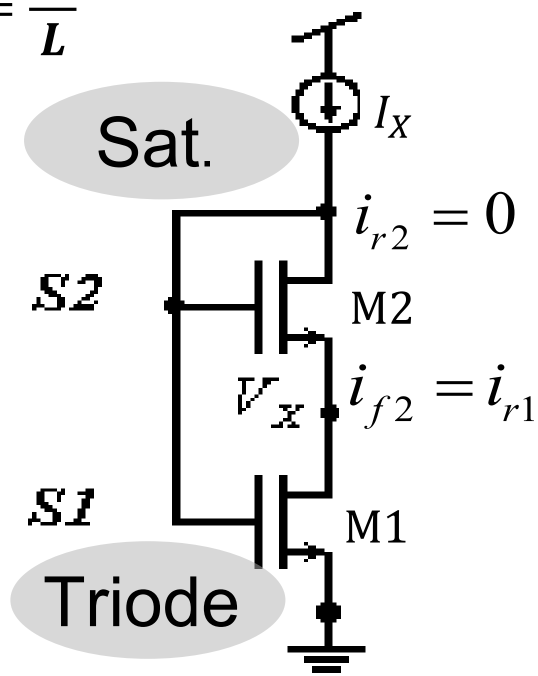




4. Current and voltage references

The self-cascode MOSFET (SCM)

$$S = \frac{W}{L}$$



$$I_X = I_{S2} i_{f2} = I_{S1}(i_{f1} - i_{f2})$$

$$\Downarrow$$

$$i_{f1} = \left(1 + \frac{I_{S2}}{I_{S1}}\right) = \left(1 + \frac{S_2}{S_1}\right) i_{f2} = \alpha i_{f2}$$

Applying UICM to M1

$$\boxed{\frac{V_X}{\phi_t} = \sqrt{1+\alpha i_{f2}} - \sqrt{1+i_{f2}} + \ln\left(\frac{\sqrt{1+\alpha i_{f2}} - 1}{\sqrt{1+i_{f2}} - 1}\right)}$$

V_X is PTAT if i_{f2} is independent of temperature

In other words, V_X is PTAT if i_{f2} is a scaled replica of I_S

In weak inversion,

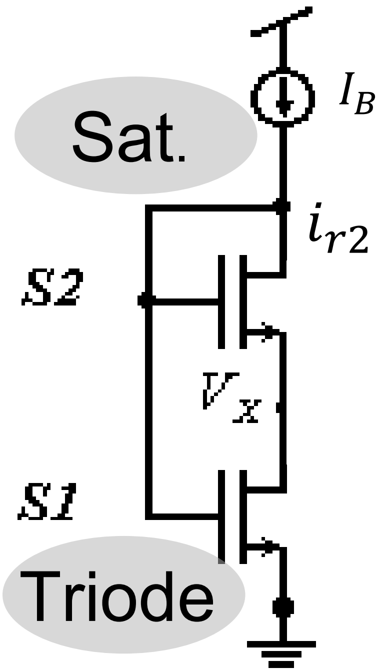
$i_{f1} = \alpha i_{f2} \ll 1$

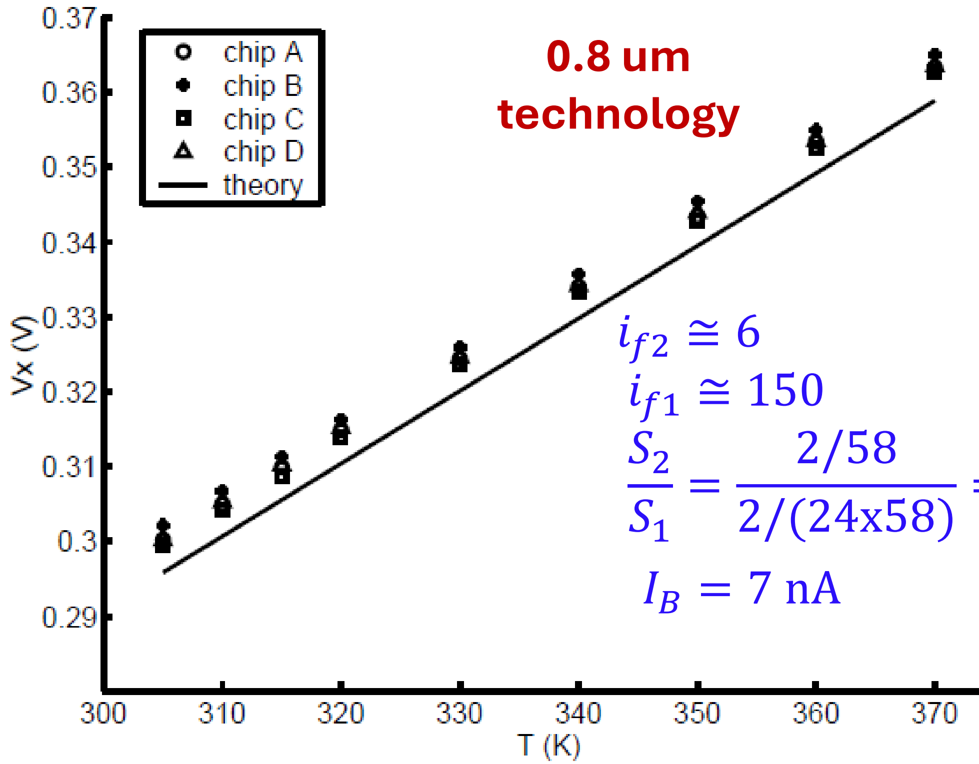
$$\boxed{\frac{V_X}{\phi_t} \to \ln \alpha} \Rightarrow$$

V_X is PTAT and independent of the current coefficient

4. Current and voltage references

The self-cascode MOSFET (SCM)





0.8 um technology

$i_{f2} \cong 6$

$i_{f1} \cong 150$

$$\frac{S_2}{S_1} = \frac{2/58}{2/(24\text{x}58)} = 24$$

$I_B = 7\ \text{nA}$

$$I = I_{S2} i_{f2} = I_{S1}(i_{f1} - i_{f2})$$

$$i_{f1} = \left(1 + \frac{I_{S2}}{I_{S1}}\right) = \left(1 + \frac{S_2}{S_1}\right) i_{f2} = \alpha i_{f2}$$

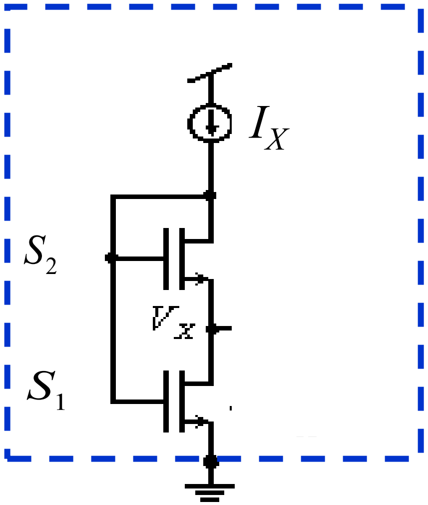
Applying UICM to M1 ⇨

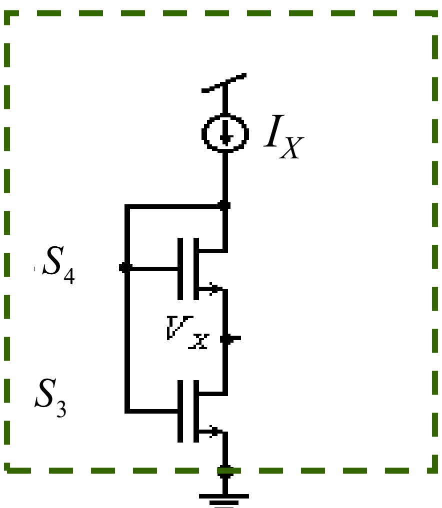
$$\frac{V_X}{\phi_t} = \sqrt{1+\alpha i_{f2}} - \sqrt{1+i_{f2}} + \ln\left(\frac{\sqrt{1+\alpha i_{f2}} - 1}{\sqrt{1+i_{f2}} - 1}\right)$$

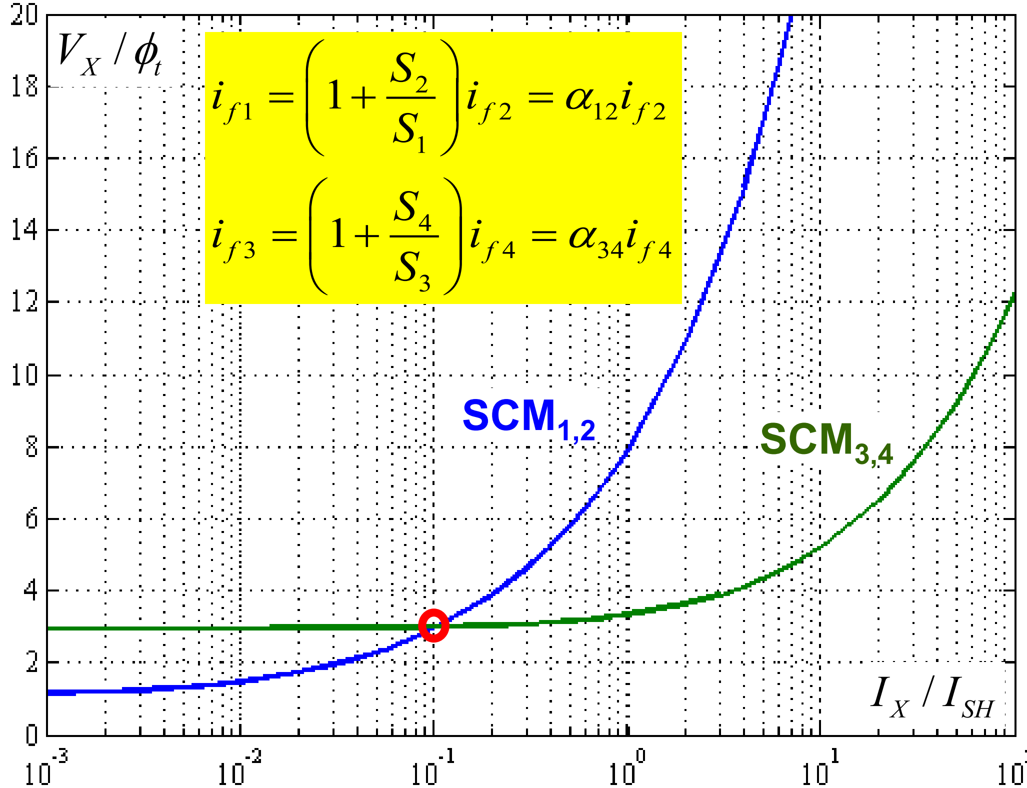
C. Rossi, C. Galup-Montoro and M.C. Schneider, "PTAT voltage generator based on an MOS voltage divider", Proceedings of Nanotech 2007, pp. 626- 629, May 2007.

4. Current and voltage references

The self-cascode MOSFET (SCM)







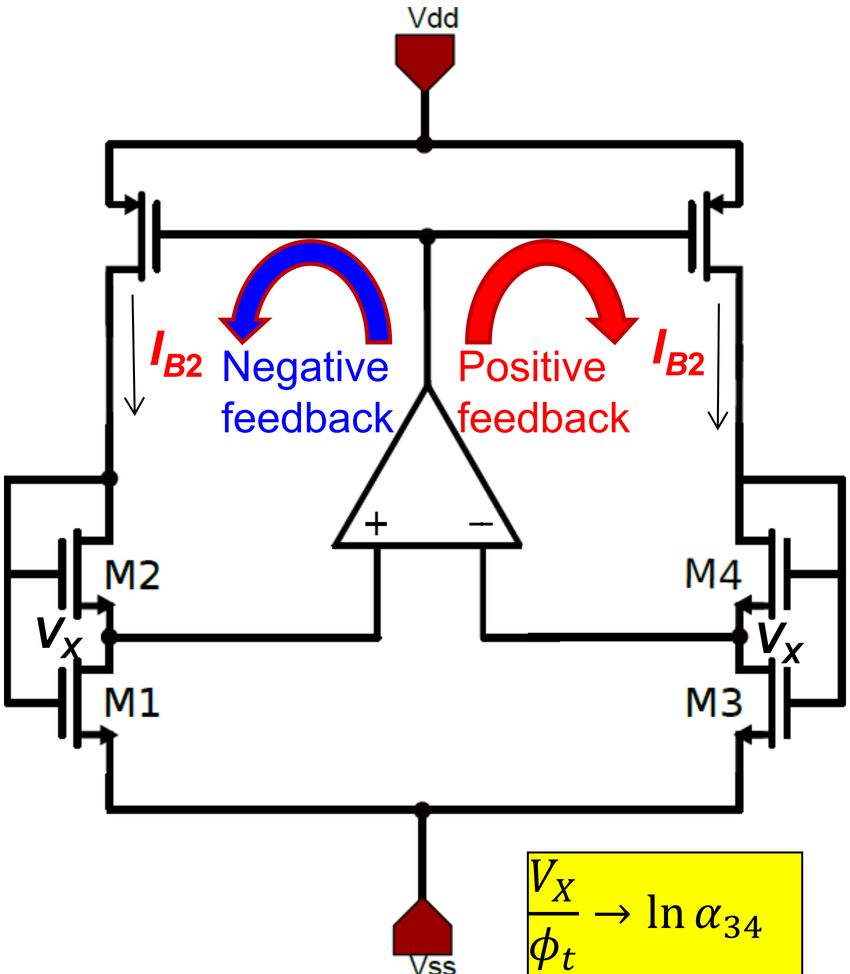
$$i_{f1} = \left(1 + \frac{S_2}{S_1}\right) i_{f2} = \alpha_{12} i_{f2}$$

$$i_{f3} = \left(1 + \frac{S_4}{S_3}\right) i_{f4} = \alpha_{34} i_{f4}$$

$$\frac{V_X}{\phi_t} = \sqrt{1 + \alpha \frac{I_X}{SI_{SH}}} - \sqrt{1 + \frac{I_X}{SI_{SH}}} + \ln\left(\frac{\sqrt{1 + \alpha \frac{I_X}{SI_{SH}}} - 1}{\sqrt{1 + \frac{I_X}{SI_{SH}}} - 1}\right)$$

4. Current and voltage references

A self-biased current source (SBCS)



$$\frac{V_X}{\phi_t} \rightarrow \ln \alpha_{34}$$

If M_3 and M_4 operate in WI :

$$\ln \alpha_{34} = \sqrt{1+\alpha_{12} i_{f2}} - \sqrt{1+i_{f2}} + \ln\left(\frac{\sqrt{1+\alpha_{12} i_{f2}}-1}{\sqrt{1+i_{f2}}-1}\right);$$

$$\alpha_{12} = 1 + \frac{S_2}{S_1} \qquad \alpha_{34} = 1 + \frac{S_4}{S_3}$$

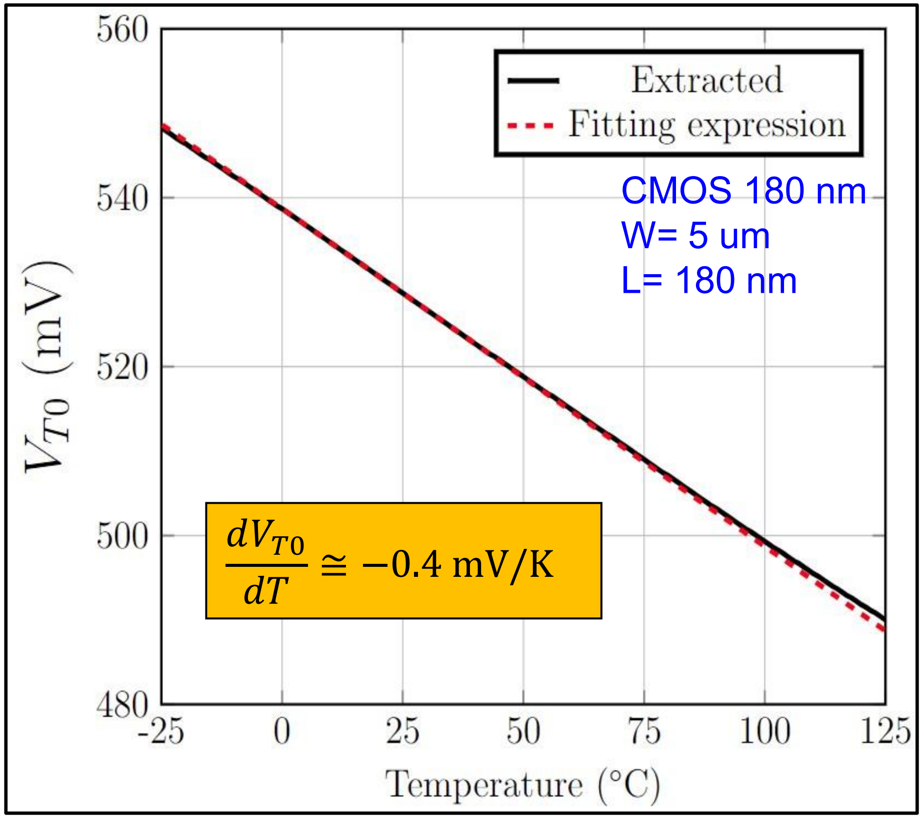
Thus, i_{f2} (the inversion level of M_2) is constant (it depends only on the geometrical ratios α_{12} and α_{34})

The reference current $I_{B2} = I_{S2} i_{f2}$ is proportional to the specific current of M_2. $I_{S2} = I_{SH}(W/L)_2 = I_{SH} S_2$

- **Stability at the operating point: Negative feedback>positive feedback**

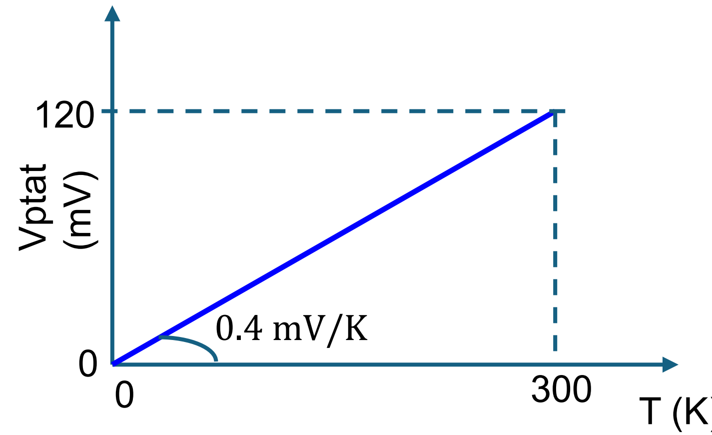
4. Current and voltage references

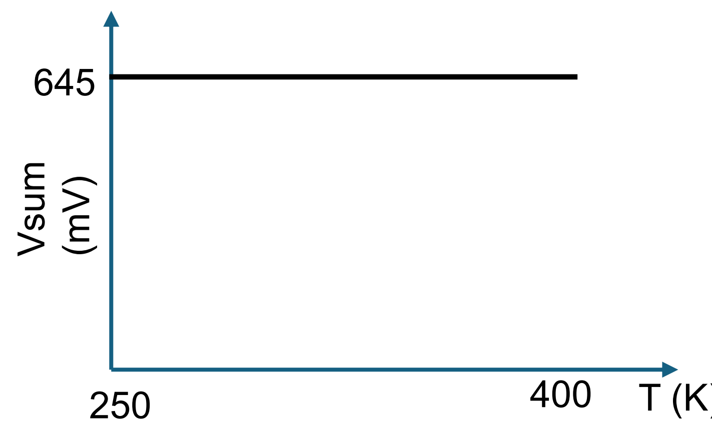
MOS-only voltage reference



Temperature dependence of the threshold voltage (CTAT)

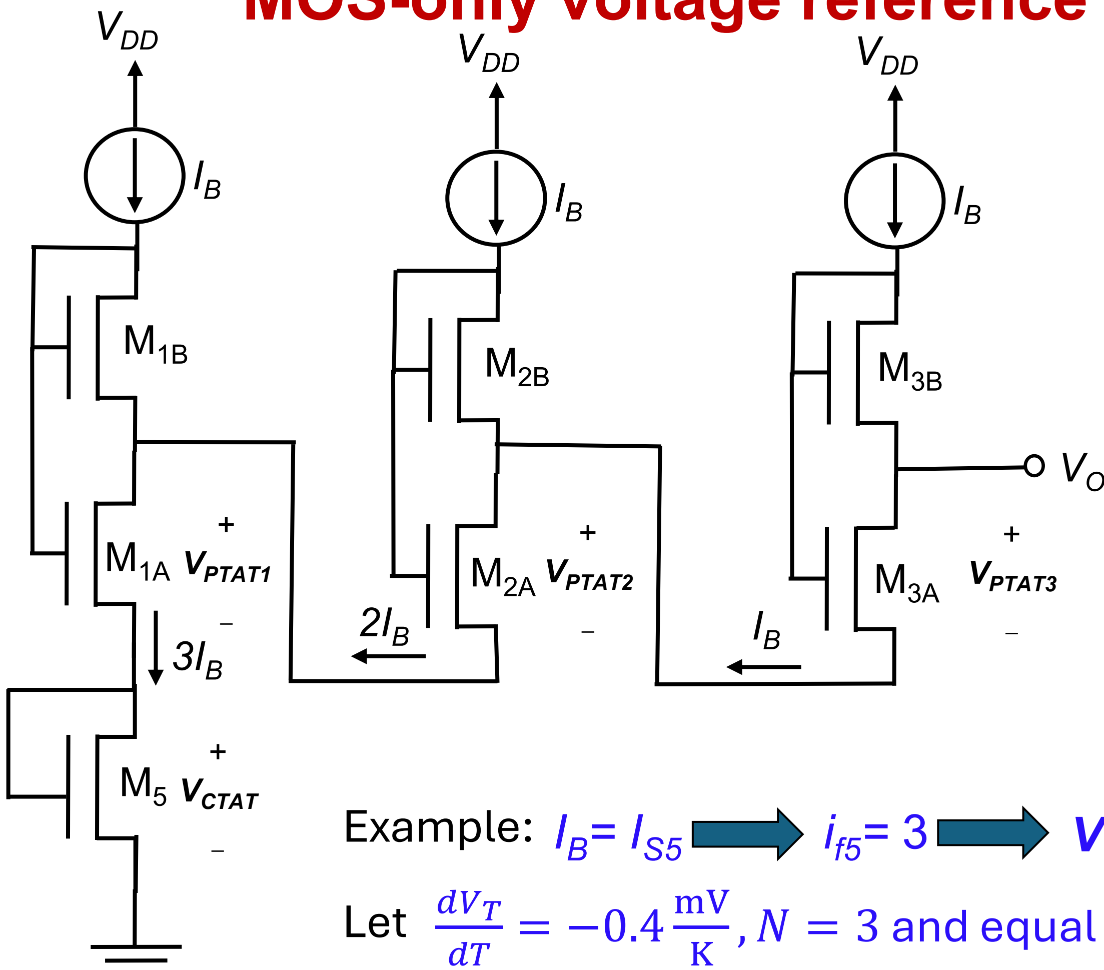
+





4. Current and voltage references

MOS-only voltage reference



$$V_O = V_{CTAT} + \sum_{i=1}^{N} V_{PTATi}$$

	W/L (μm/μm)	i_f	i_r
M5	1/1	3	<<3
M1A	20/1	19/100	1/25
M1B	25/1	1/25	<<1/25
M2A	20/1	4.7/37	1/37
M2B	37/1	1/37	<<1/37
M3A	20/1	4.7/74	1/74
M3B	74/1	1/74	<<1/74

Example: $I_B = I_{S5}$ ➔ $i_{f5} = 3$ ➔ $V_{CTAT} = V_T$

Let $\frac{dV_T}{dT} = -0.4\frac{\text{mV}}{\text{K}}$, $N = 3$ and equal V_{PTATi}

$$\frac{dV_O}{dT} = 0 \rightarrow 3\frac{dV_{PTAT}}{dT} = -\frac{dV_{CTAT}}{dT}$$

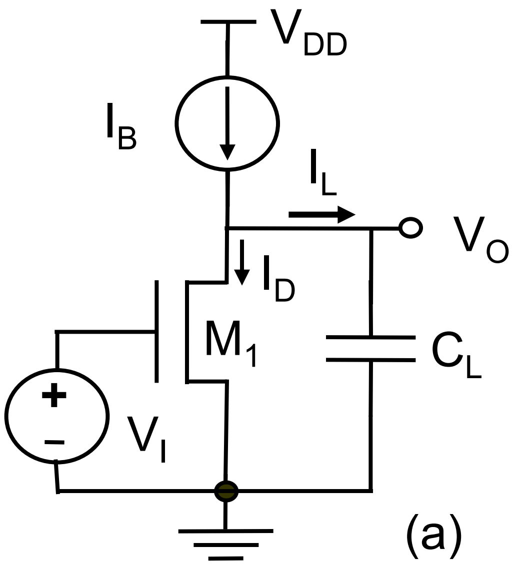
$$\frac{dV_O}{dT} = 0 \rightarrow \frac{dV_{PTAT}}{dT} = 133\ \mu\text{V/K}$$

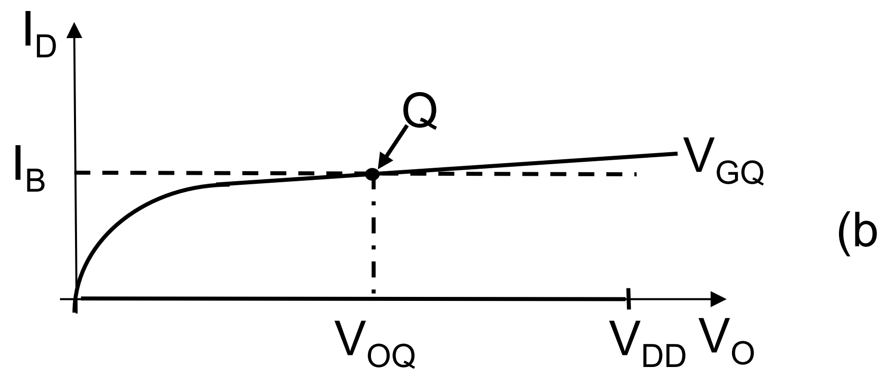
E. Vittoz and O. Neyroud, “A low-voltage CMOS bandgap reference,” Solid-State Circuits, IEEE Journal of, vol. 14, no. 3, pp. 573–579, 1979.

5. Single-stage amplifiers

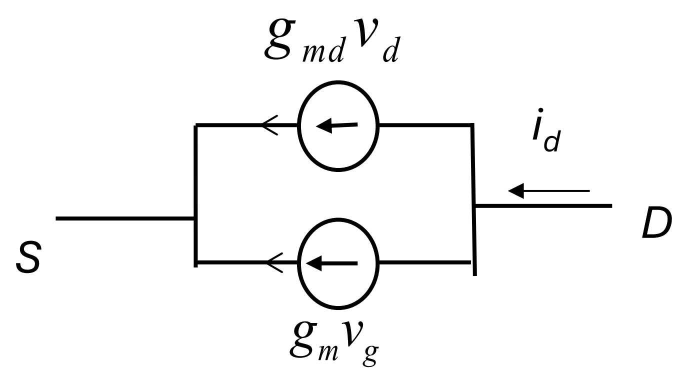
Common-source amplifier

The intrinsic gain





$$\boxed{A_V = \frac{-g_m}{g_{md}}}$$

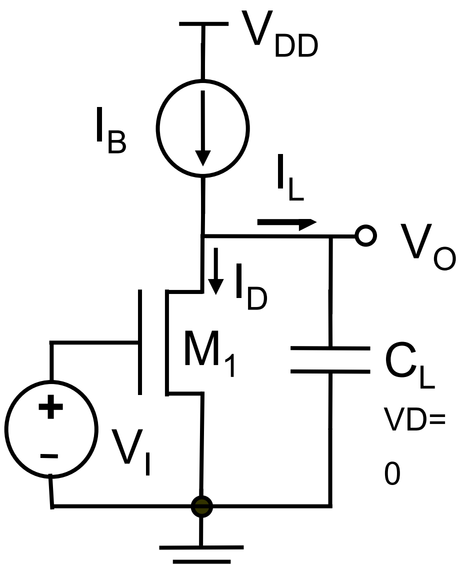


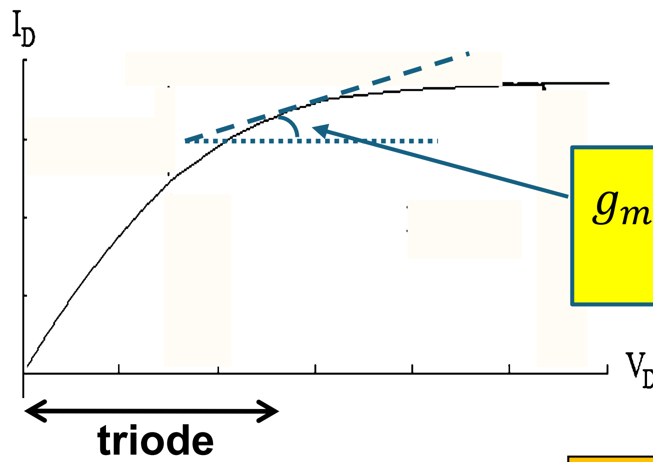
The gain is a function of technology, transistor channel length, bias current, and output voltage

5. Single-stage amplifiers

Common-source amplifier

Velocity saturation not accounted for :

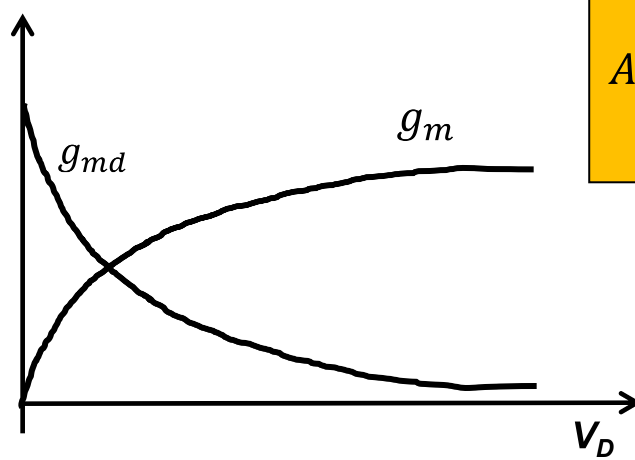




$$g_m = \frac{2I_S}{n\phi_t}(q_s - q_d)$$

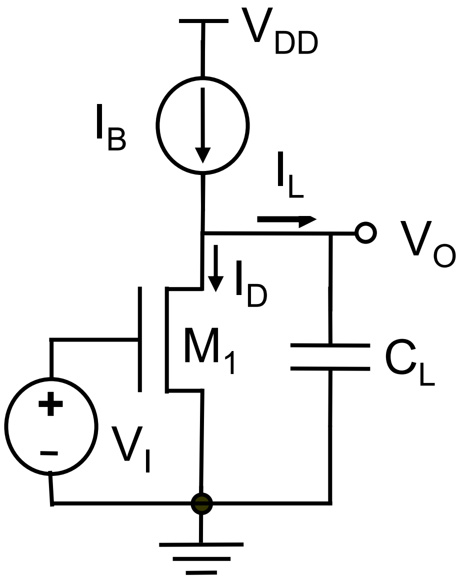
$$g_{md} = \frac{2I_S}{n\phi_t}(q_s - q_d)\sigma + \frac{2I_S}{\phi_t}q_d$$

$$A_V = -\frac{g_m}{g_{md}} = -\frac{\frac{q_s}{q_d} - 1}{\sigma\left(\frac{q_s}{q_d} - 1\right) + n}$$



5. Single-stage amplifiers

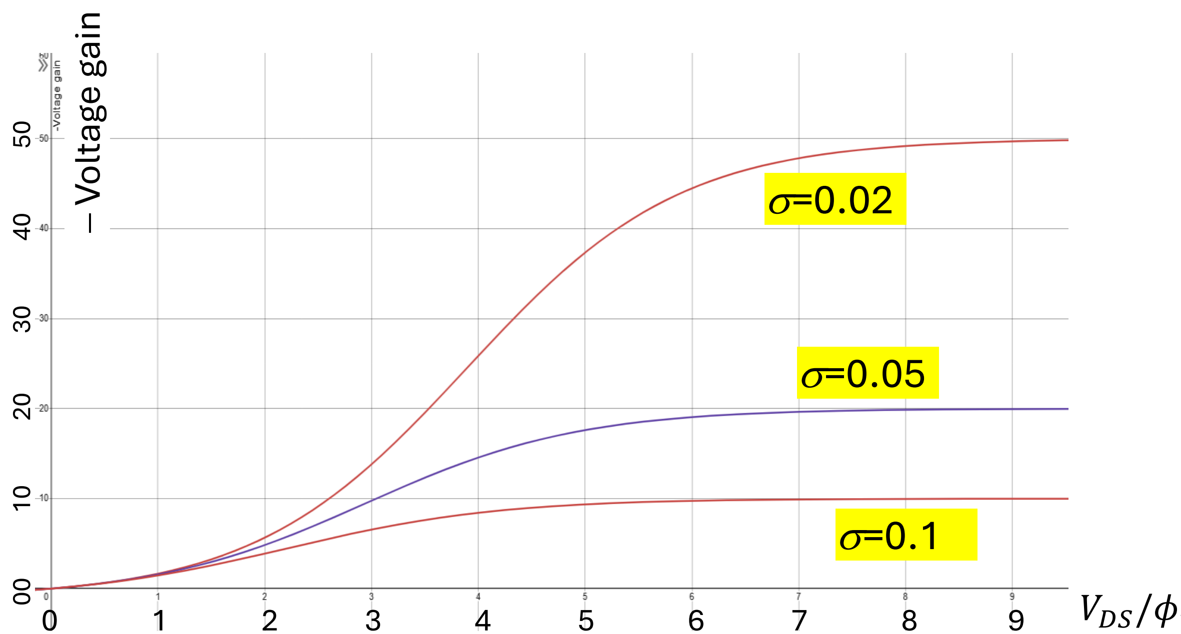
Common-source amplifier



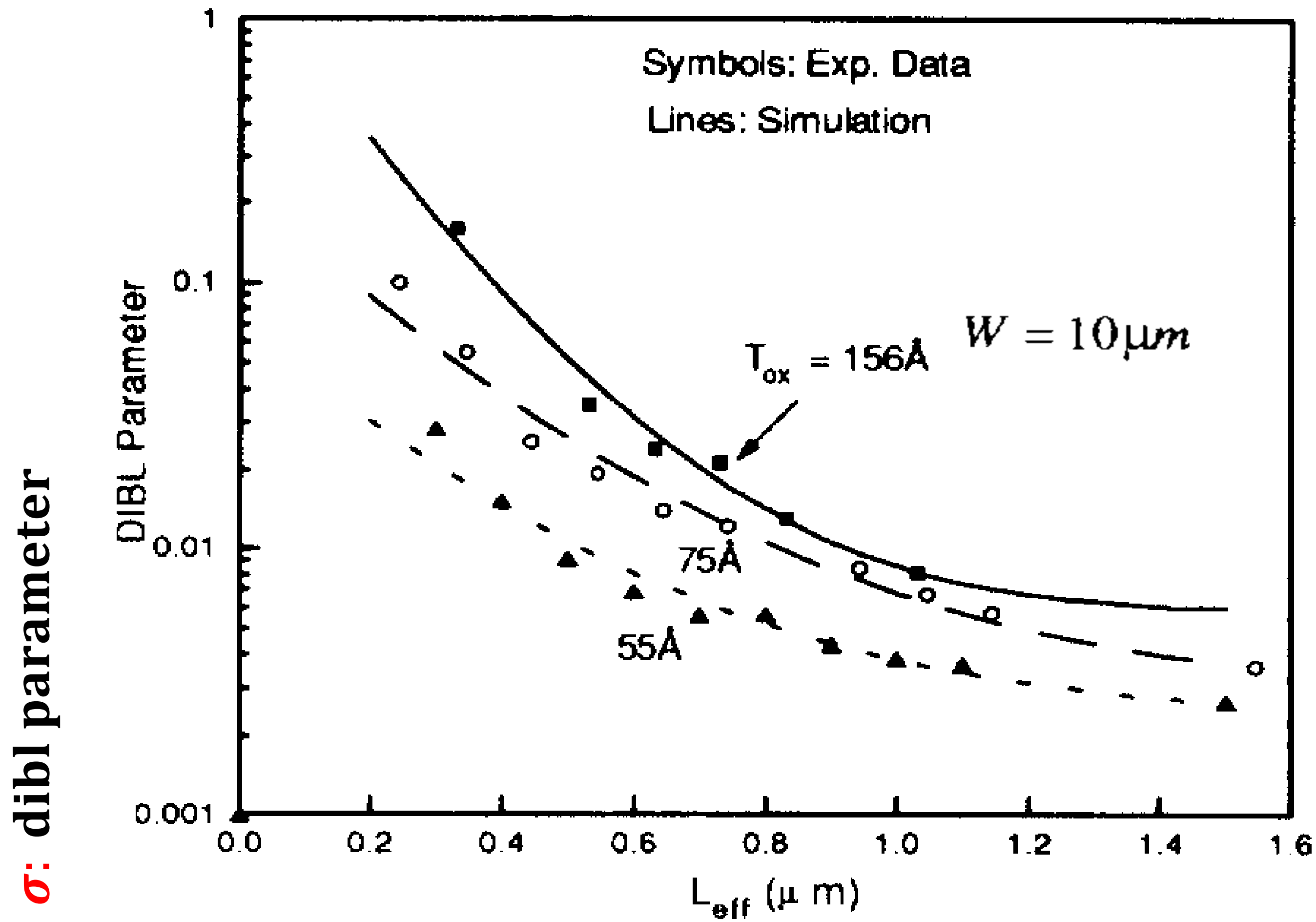
$$A_V = -\frac{g_m}{g_{md}} = -\frac{\frac{q_s}{q_d} - 1}{\sigma\left(\frac{q_s}{q_d} - 1\right) + n}$$

Weak inversion

$$A_V = -\frac{e^{\frac{V_{DS}}{\phi_t}} - 1}{\sigma\left(e^{\frac{V_{DS}}{\phi_t}} - 1\right) + n}$$



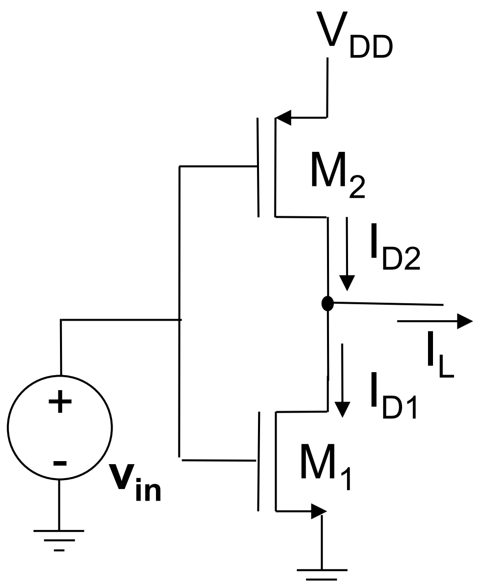
DIBL coefficient versus channel length

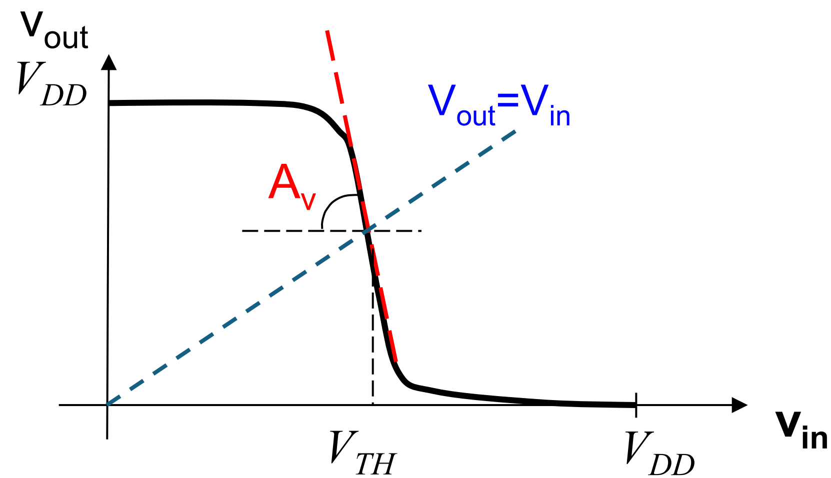


J. H. Huang et al., A physical model for MOSFET output resistance, IEDM 1992

5. Single-stage amplifiers

Push-pull amplifier (static CMOS inverter)





Voltage gain: $A_V = -\dfrac{g_{m1} + g_{m2}}{g_{md1} + g_{md2}}$ $\quad g_{m1(2)} = \dfrac{I_{TH}}{n_{1(2)}\varphi_t} \dfrac{2}{1+\sqrt{1+i_{f1(2)}}}$ $\quad g_{md1(2)} = \sigma_{1(2)} g_{m1(2)}$

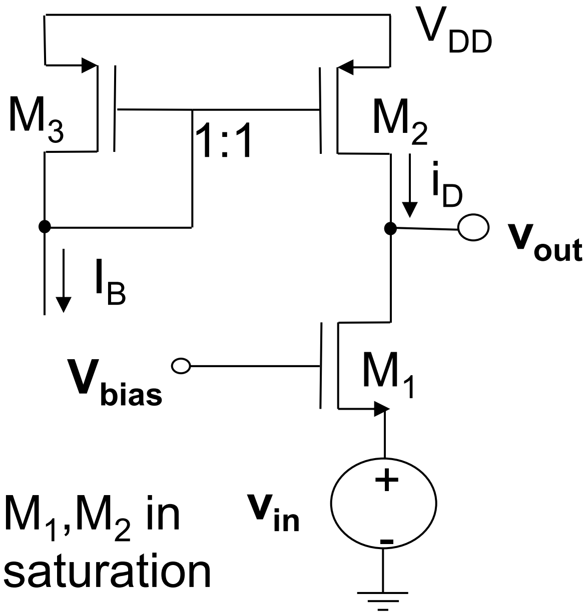
For "deep" saturation:

$$\frac{1}{A_V} = -\left(\frac{g_{m1}\sigma_1}{g_{m1}+g_{m2}} + \frac{g_{m2}\sigma_2}{g_{m1}+g_{m2}}\right)$$

$$A_V = -\frac{2}{\sigma_1+\sigma_2} \text{ for } g_{m1} = g_{m2}$$

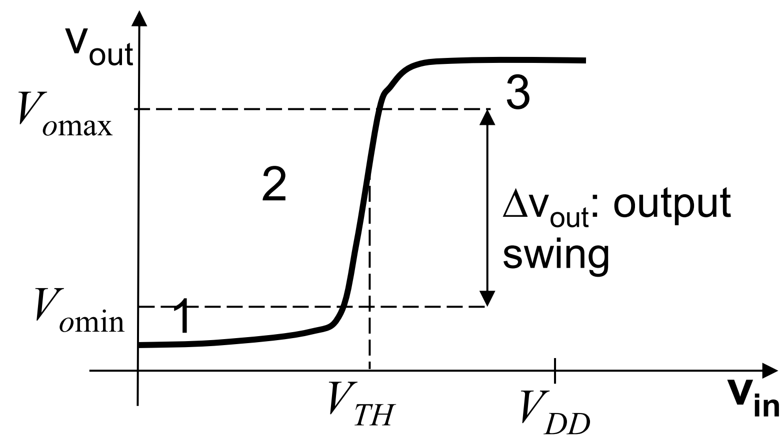
5. Single-stage amplifiers

Common-gate amplifier



M_1,M_2 in saturation

$$I_{D1} = I_B \approx I_{F1} \quad i_{f1} \approx \frac{I_B}{I_{S1}}$$

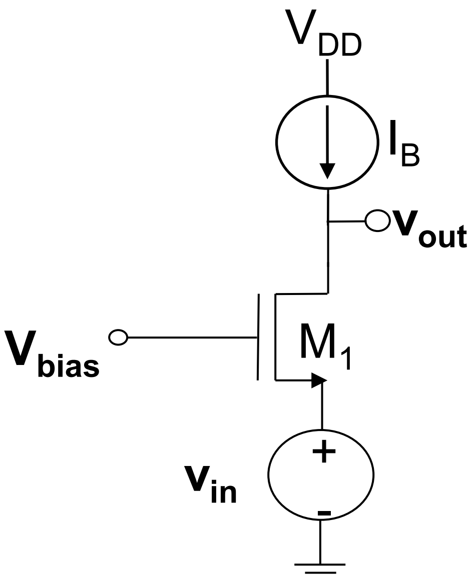


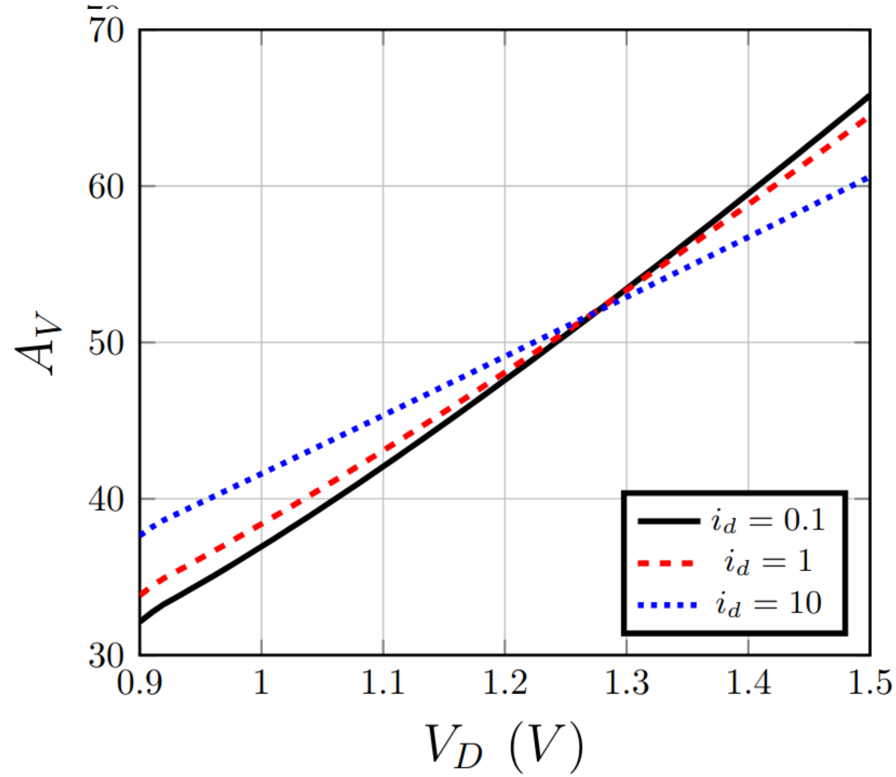
UICM

$$\boxed{V_{TH} = \frac{V_{bias} - V_{T0N}}{n_N} - \phi_t\left[\sqrt{1+i_{f1}} - 2 + \ln\left(\sqrt{1+i_{f1}} - 1\right)\right]}$$

5. Single-stage amplifiers

Common-gate amplifier





$I_B \approx$ 0.5 uA, 5 uA, 50 uA

Voltage gain – weak inversion

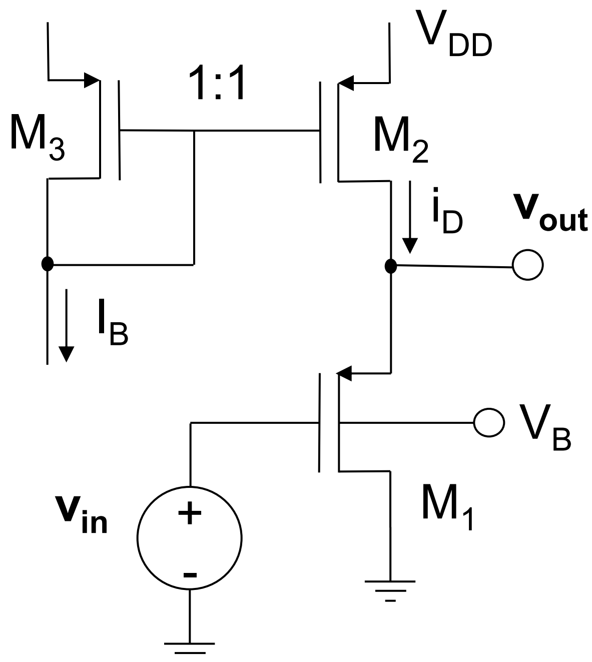
$$A_V = \frac{g_{ms}}{g_{md}} = \frac{\dfrac{1}{1 - e^{\frac{-V_{DS}}{\phi_t}}} - \dfrac{\sigma}{n}}{\dfrac{\sigma}{n} + \dfrac{1}{e^{\frac{V_{DS}}{\phi_t}} - 1}}$$

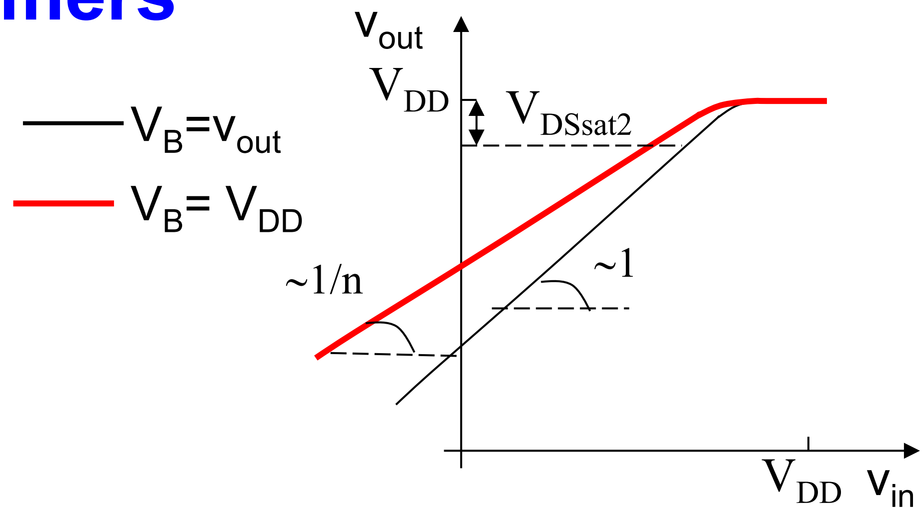
$$e^{\frac{V_{DS}}{\phi_t}} \gg 1 \;\Rightarrow\; A_V = \frac{g_{ms}}{g_{md}} = \frac{n}{\sigma} - 1$$

For n=1.25, $\sigma = 0.025$ $\Rightarrow$ $A_V = \frac{n}{\sigma} - 1 = 49$

5. Single-stage amplifiers

Source follower





$$V_{out,max} = V_{DD} - |V_{DS,sat2}|$$

$$V_{out,min} = |V_{DS,sat1}|$$

Weak inversion
Saturation

$V_B = v_{out}$

$$\frac{v_{out}}{v_{in}} = \frac{1}{1 + \frac{g_{md1} + g_{md2}}{g_{m1}}} = \frac{1}{1 + \sigma_1 + \frac{g_{m2}}{g_{m1}}\sigma_2}$$

$V_B = V_{DD}$

$$\frac{v_{out}}{v_{in}} = \frac{1}{1+\frac{g_{mb1}+g_{md1}+g_{md2}}{g_{m1}}} = \frac{1}{n+\sigma_1+\frac{g_{m2}}{g_{m1}}\sigma_2}$$

THANKS FOR ATTENDING THE ANALOG SECTION OF THE TUTORIAL

QUESTIONS?

Part 4
Advanced Compact MOSFET Model: Design Methodology-Application to Low Noise Amplifier

"Scan me"

LASCAS 2025
16th IEEE CASS Latin American Symposium on Circuits and Systems

Sylvain Bourdel

https://github.com/ACMmodel/MOSFET_model
https://colab.research.google.com/drive/1s3PKF6pf3zIhlTj6jc-qhCLIcGfJ_UEE?usp=sharing#scrollTo=EMGo7aUzyukW

Agenda

- Overview of Design Methods for RFIC
- LNA Design Considerations
- Resistive Feedback LNA
- What we need in ACM-2
- Inversion Level Based Method for R-Feedback LNA with ACM-2

Agenda

- Overview of Design Methods for RFIC
- LNA Design Considerations
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- What we need in ACM-2
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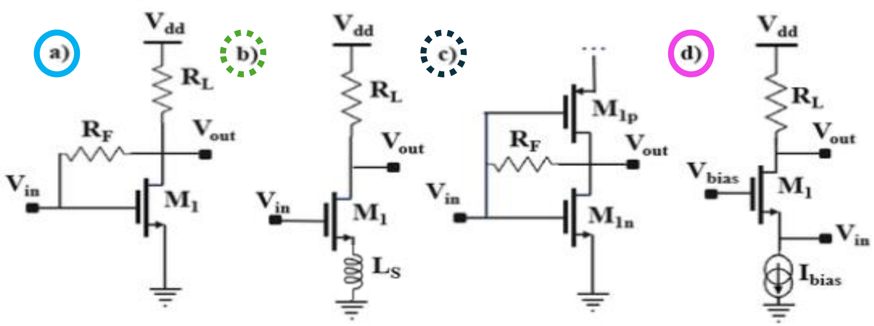
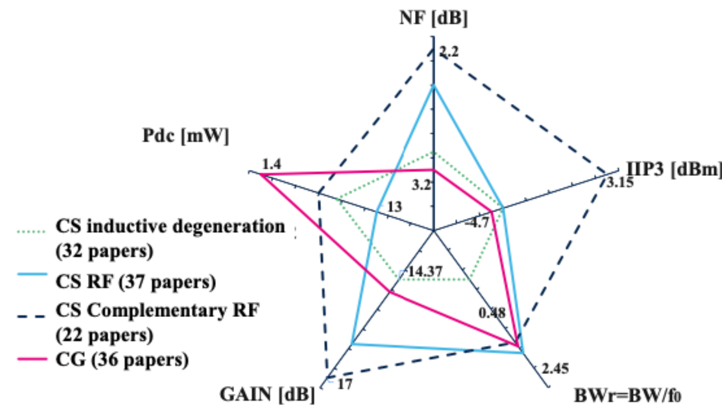
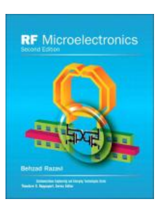
Overview of Design Methods for RFIC General Principle

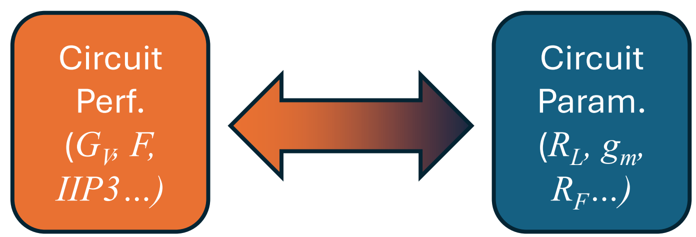
- 1^{st} Step: Architecture Choice





- 2^{nd} Step: Circuit Analysis

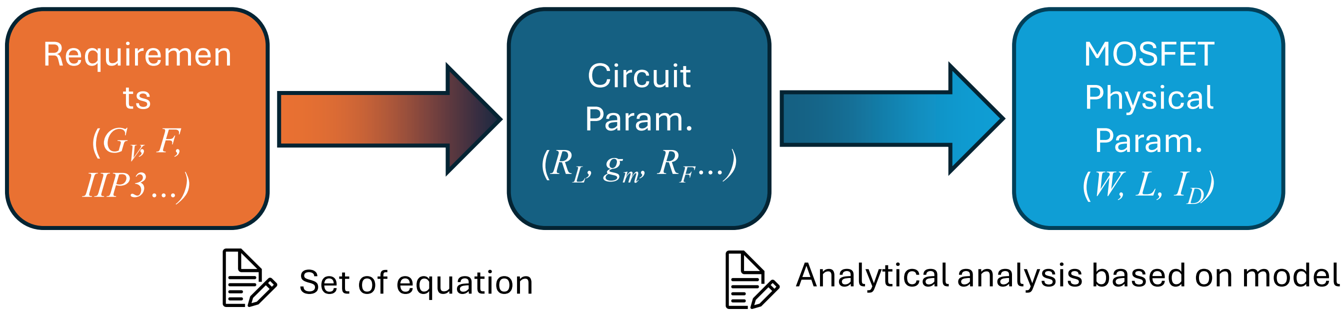




$$|G_T| = |G_v| Q_{IN} = \frac{(G_m R_F - 1) R_O}{(R_O + R_F)} \sqrt{1 + Q_P^2}$$

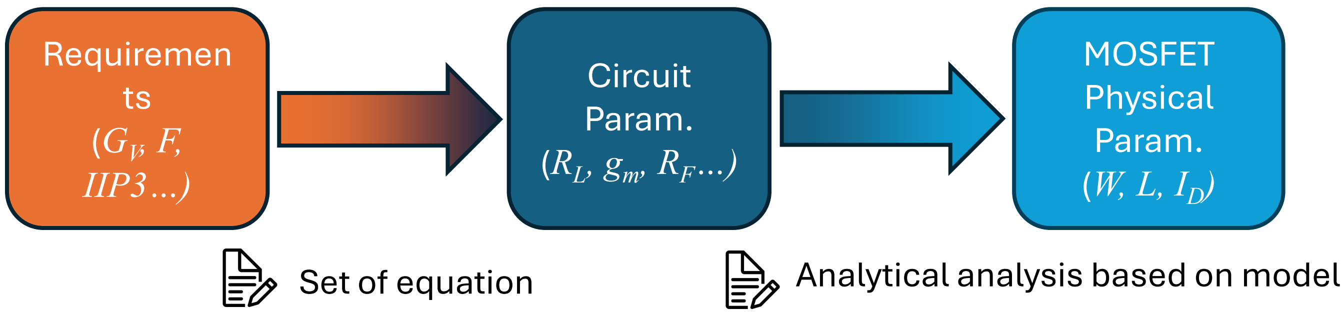
Overview of Design Methods for RFIC General Principle

- 3rd Step: Circuit Sizing



Overview of Design Methods for RFIC General Principle

- 3rd Step: Circuit Sizing



Region based model

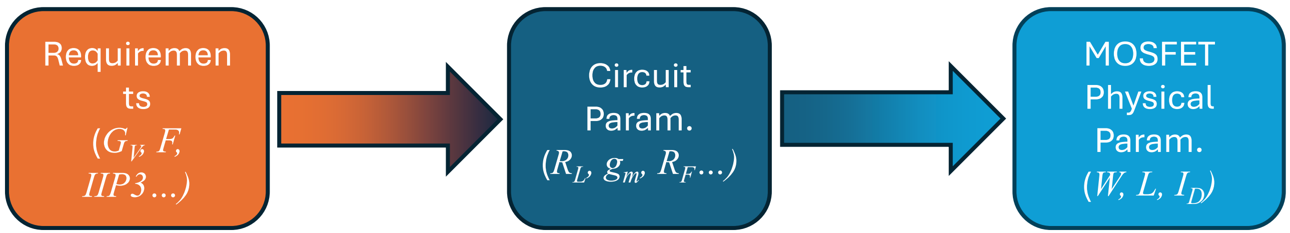
sat. $$I_d = 2.K_n \frac{W}{L}\left[(V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2}\right]$$

lin. $$I_d = K_n \frac{W}{L}(V_{gs} - V_t)^2\left(1 + \frac{k_{en}}{L}V_{ds}\right)$$

PROS: simple
CONS: Inaccurate with short channel MOS

Overview of Design Methods for RFIC
General Principle

- 3rd Step: Circuit Sizing



Set of equation

Analytical analysis based on model

Electrical simulation based on model

BSIM3 / UTSOI compact model

PROS:

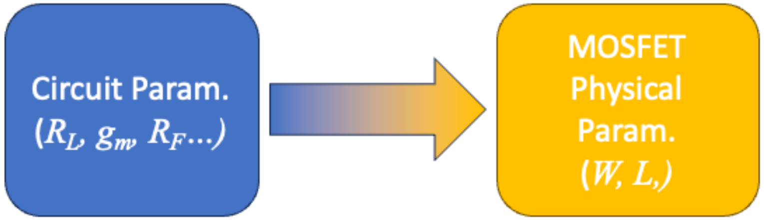
- *Accurate*
- *Direct relationship between requirements and physical parameters*

CONS:

- *Increases the gap between Physic and design*
- *Long optimization*

Overview of Design Methods for RFIC New Trends

- **Issue in the sizing step**



?

  - How to maintain simplicity **and** accuracy with the scaling and especially Short Channel Effects (SCE) at the sizing step.

?

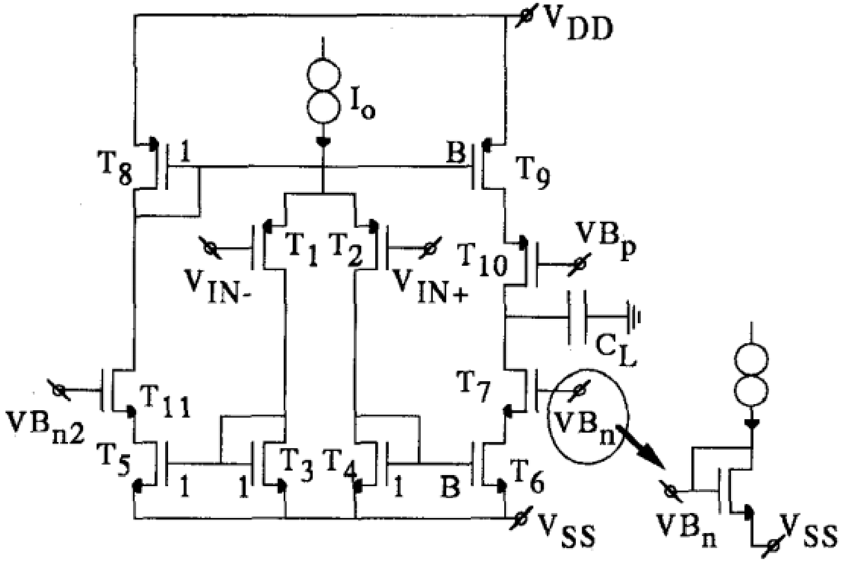
- **A possible solution**
  - g_m/Id design approaches
    - LUT based
    - ACM or EKV based

Overview of Design Methods for RFIC g_m/Id approach based on LUT

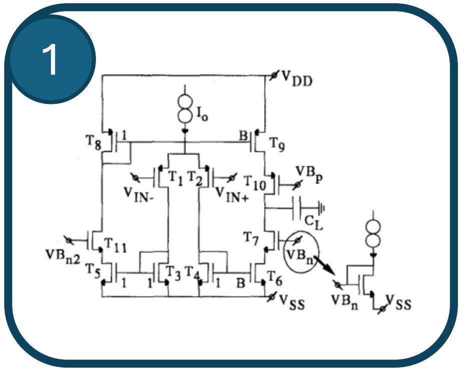
[Silveira, Flandre, Jespers – JSSC 1996]

General Principle

- For a given structure



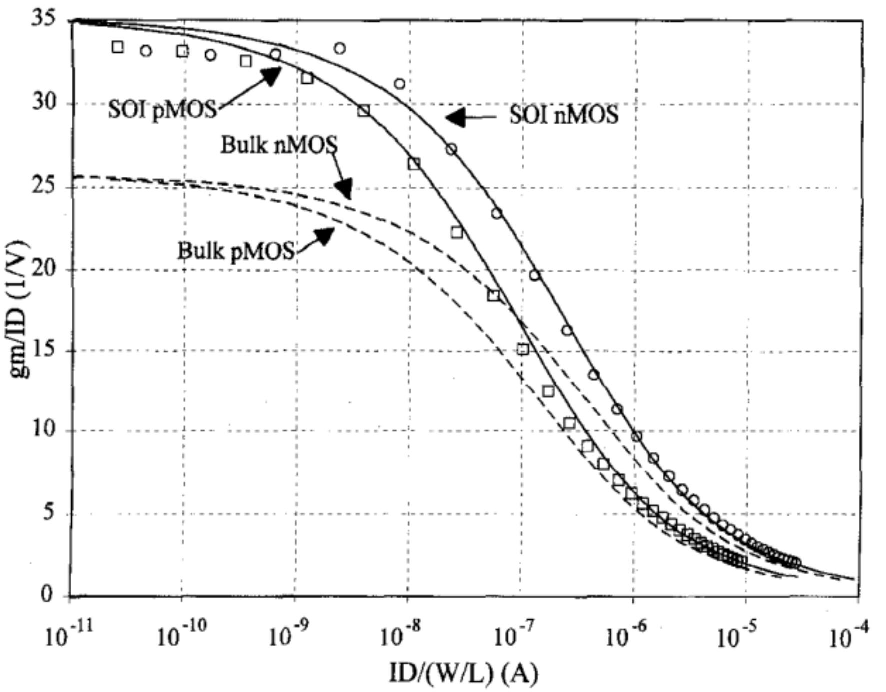
Overview of Design Methods for RFIC
g_m/Id approach based on LUT



General Principle

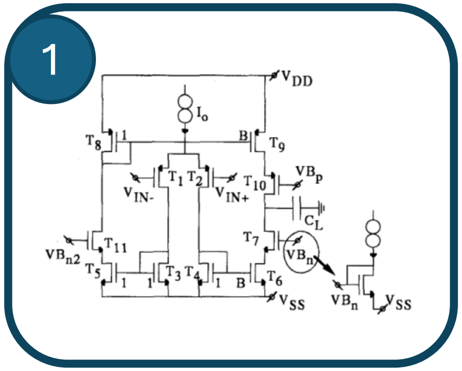
- For a given structure

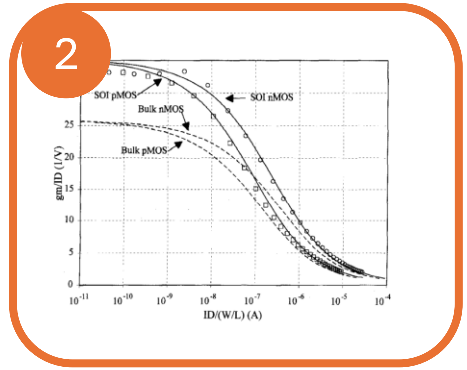
- Methods are based on
  - ⇒ Extraction of MOS parameters (LUT)
    - $I_D/(W/L)$ vs g_m/I_D
    - g_m/I_D vs V_{gs0}



Overview of Design Methods for RFIC
g_m/Id approach based on LUT

General Principle





- For a given structure

- Methods are based on
  - $\Rightarrow$ Extraction of MOS parameters (LUT)
    - $I_D/(W/L)$ vs g_m/I_D
    - g_m/I_D vs V_{gs0}
  - $\Rightarrow$ Set of equations

$$SR = \frac{B \cdot I_{D1}}{C_L}$$

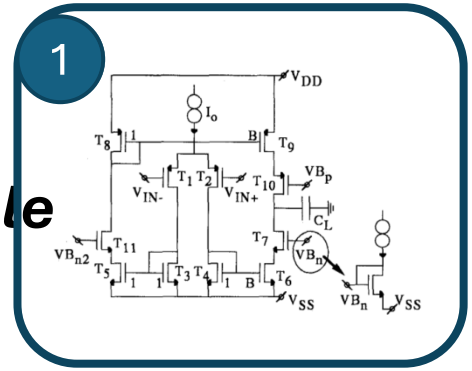
$$f_T = \frac{B \cdot g_{m1}}{2\Pi \cdot C_L} \qquad (5)$$

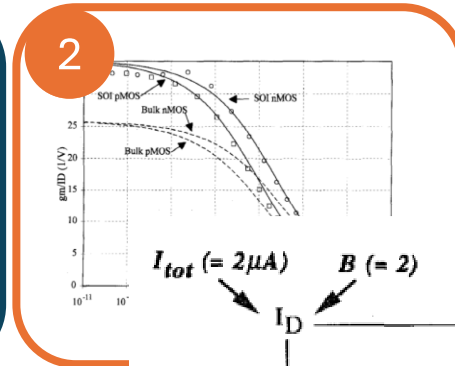
$$A_0 = \left(\frac{g_m}{I_D}\right)_1 \cdot \left(\frac{g_m}{I_D}\right)_2 \cdot \frac{1}{\frac{1}{V_{A6} \cdot V_{A7}} + \frac{1}{V_{A9} \cdot V_{A10}}} \qquad (4)$$

Overview of Design Methods for RFIC

g_m/Id approach based on LUT

General Principle





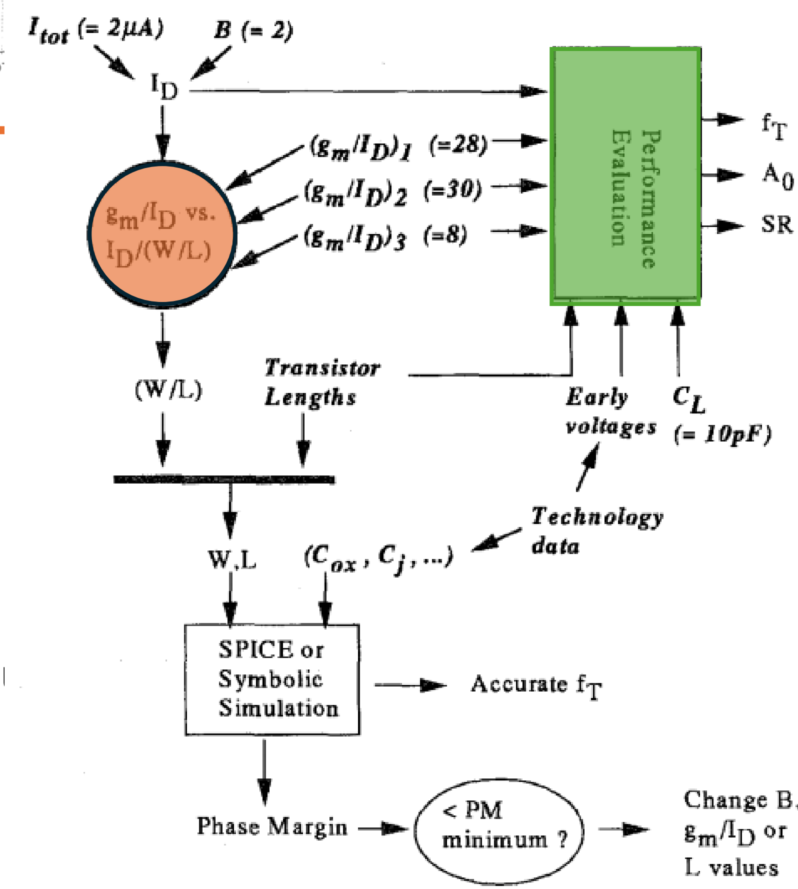
3

$$SR = \frac{B \cdot I_{D1}}{C_L}$$

$$f_T = \frac{B \cdot g_{m1}}{2\Pi \cdot C_L} \quad (5)$$

$$A_0 = \left(\frac{g_m}{I_D}\right)_1 \cdot \left(\frac{g_m}{I_D}\right)_2 \cdot \frac{1}{\frac{1}{V_{A6} \cdot V_{A7}} + \frac{1}{V_{A9} \cdot V_{A10}}} \quad (4)$$

- For a given structure
- Methods are based on
  - ⇒ Extraction of MOS parameters (LUT)
    - $I_D/(W/L)$ vs g_m/I_D
    - g_m/I_D vs V_{gs0}
  - ⇒ Set of equations
- Methods helps the designers in sizing the struct
- Quite used in low frequency domain



Overview of Design Methods for RFIC

g_m/Id approach based on LUT

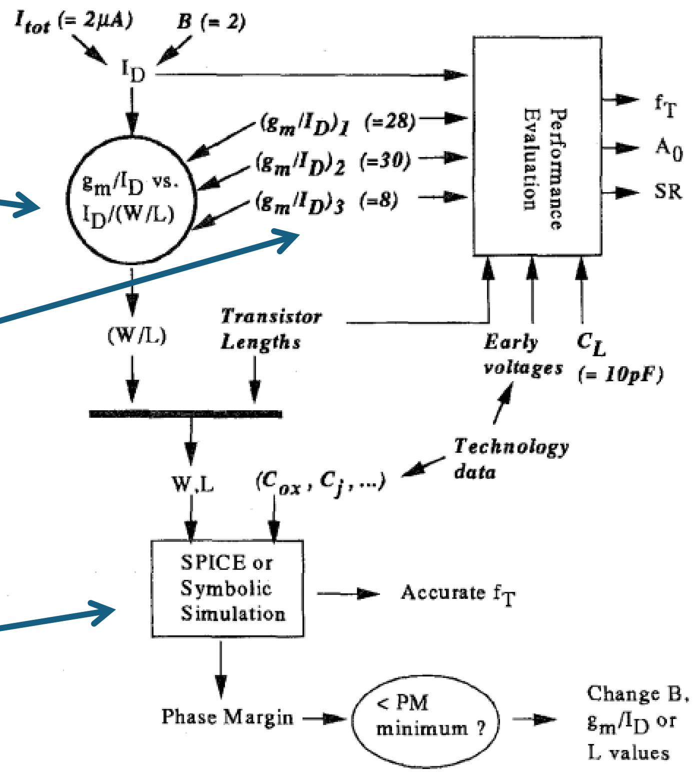
LIMITATIONS ?

- Time Consuming

- Lakes of precision (parametric set of characteristics)

- Long optimization sequence

Need for a model based approach

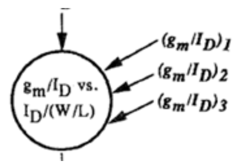


Overview of Design Methods for RFIC

g_m/Id approach based All Region Models (ACM/EKV)

All Region 3PM model

- EKV – [Enz, Krummenacher, Vittoz]
- ACM – [Schneider, Galup]



$$\frac{I_D}{\left(W/_L\right)} = i_f I_{S0}$$

- With a 3PM model we have :

$$\frac{g_m}{I_D} = \frac{2}{n\phi_t\left(1+\sqrt{1+i_f}\right)} \qquad g_m = \frac{2I_S}{\phi_t}\left(\sqrt{1+i_f}-1\right) \qquad V_P - V_{S(D)} = \phi_t\left[\sqrt{1+i_{f(r)}} - 2 + \ln\left(\sqrt{1+i_{f(r)}}-1\right)\right]$$

$$V_P \cong \frac{V_G - V_{T0}}{n}$$

- PROS: The sizing is straightforward
- CONS: Inaccurate with SCE

Non-linearities can't be captured
gds effect can't be captured

Can we design RFICs '

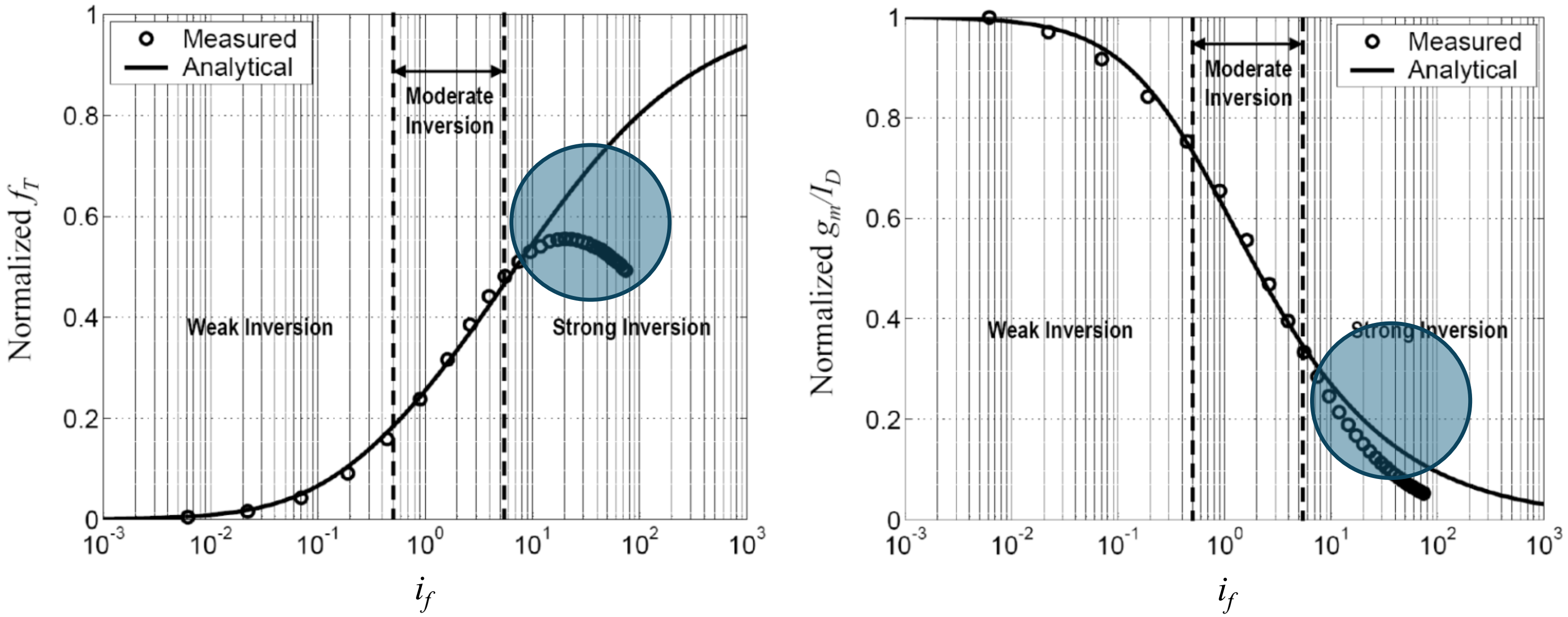
Overview of Design Methods for RFIC

g_m/Id in RFIC design

Design Regions

Year 2000 (RF-180nm)

- f_t grows with i_f



Overview of Design Methods for RFIC

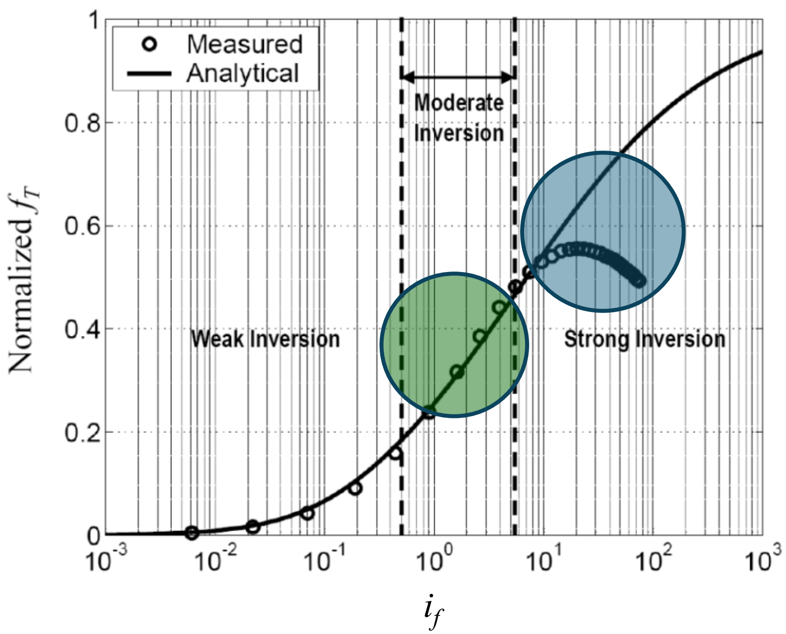
g_m/Id in RFIC design

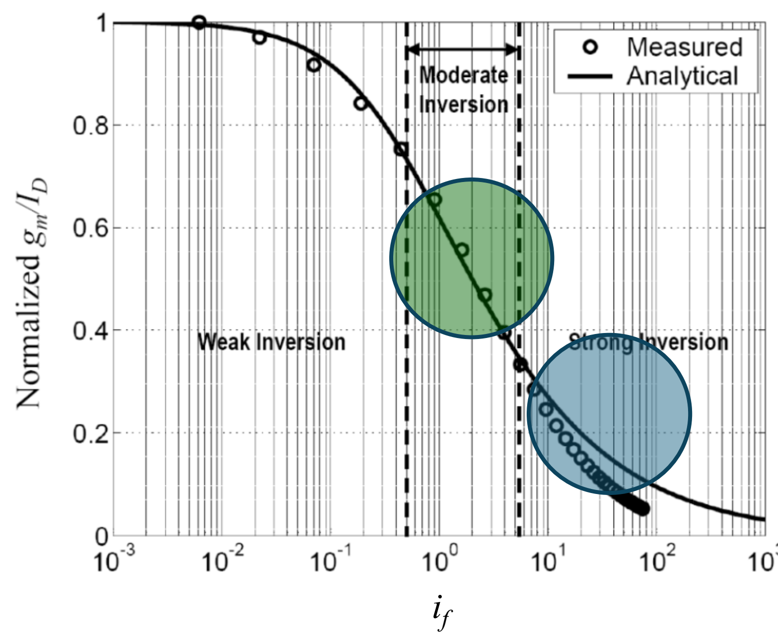
Design Regions

Year 2000 (RF-180nm)

Year 2016 (RF-22nm) up to now

- f_t grows with i_f **but** g_m/I_D reduces with i_f





Overview of Design Methods for RFIC

g_m/Id in RFIC design

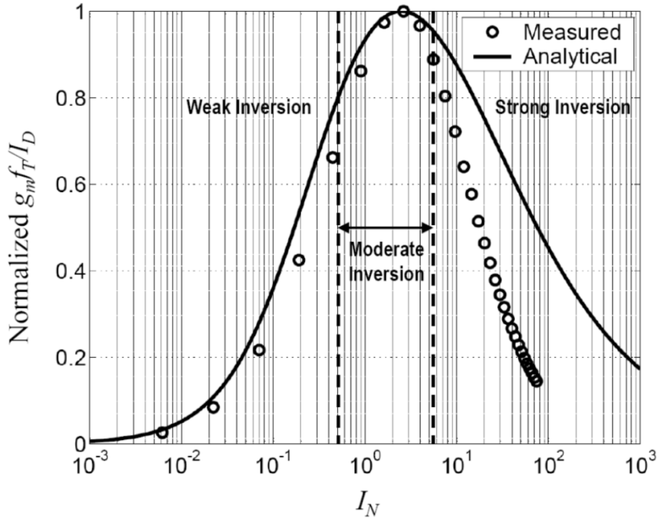
$g_m f_T / I_D$: A First Approach

A. Shameli et P. Heydari, « Ultra-Low Power RFIC Design Using Moderately Inverted MOSFETs: An Analytical/Experimental Study », *RFCI*, 2004.

- For RF design

- A FOM that maximize the gain bandwidth product

$$\frac{g_m f_T}{I_D}$$



- Gives the i_f that produces the best GBW product

- Not optimal :
  - the gain or the bandwidth might be oversized.
  - Do not depends on the topology

Overview of Design Methods for RFIC

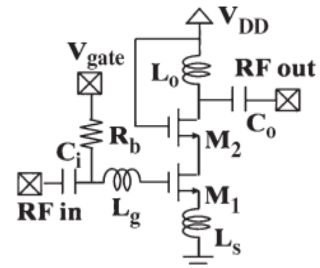
g_m/Id in RFIC design

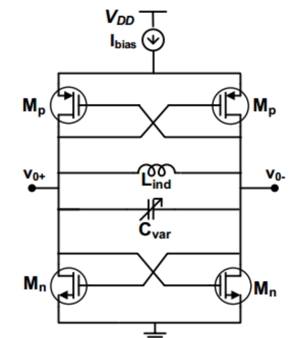
LN
A

LO

Function Based FoM

- For a given Function
- Define a FoM for the function
- Find the i_f that maximizes the FoM



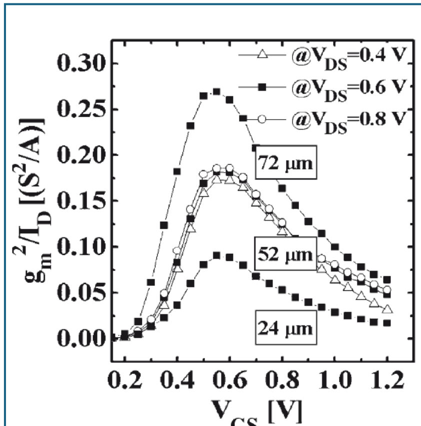


$$\mathrm{FoM}_{\mathrm{LNA}} = \frac{G}{(F-1)\cdot P} \propto \frac{g_m^2}{\left(\frac{I_D}{g_m^2}\right)\cdot I_D} \propto \left(\frac{g_m^2}{I_D}\right)^2$$

I. Song et B.-G. Park, « A Simple Figure of Merit of RF MOSFET for Low-Noise Amplifier Design », *Electron Device Lett. IEEE*, vol. 29(12), 2008.

$$PN(\Delta f) = 10log\left(\frac{k_B T\pi^2}{64Q^2}\frac{g_m}{I_D}\frac{1}{I_D}\frac{f_0}{(\Delta f)^2}\lambda\right)$$

R. Fioreli ; J. Núñez ; F. Silveira; “All-Rnversion region gm/ID methodology for RF circuits in FinFET technologies”
2018 NEWCAS



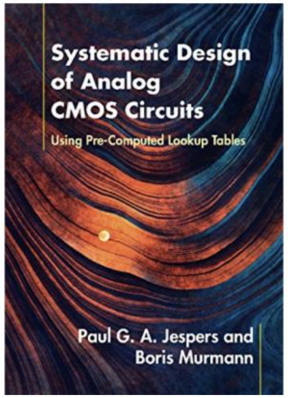
Overview of Design Methods for RFIC

g_m/Id in RFIC design

Circuit Based Method

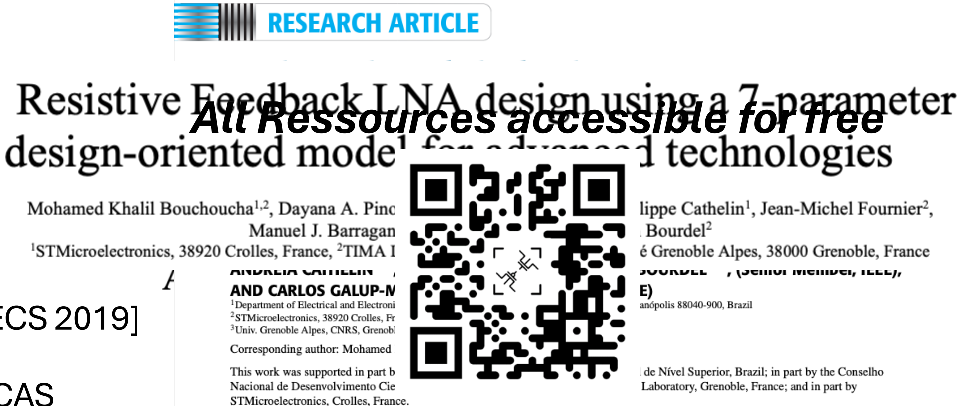
Circuit Sizing Based on LUT

- For a given Circuit
- Similar to the one introduced by Silveira, Flandre, Jespers in 1996
- Capacitance and noise effects can be captured in LUT for bandwidth and noise analysis
- Well known and well referenced
- But …
    - Still complicated
    - The gap between physics and design remains
    - No analytical relationships to size « by hand »



Circuit Sizing Based on ACM

- Equations can be derived for a given circuit
- Quasi analytical approach
    - R-F LNA designed with 3PM-ACM [Bourdel - ICECS 2019]
- Gds and gm3 (NL) are taken into account
    - R-F LNA designed with 7PM-ACM [Bouchoucha – ISCAS 2023]
    - 2G LNA designed with 5PM-ACM2[Alves Neto – ACCESS 2024]



All Ressources accessible for free

https://github.com/ACMmodel/MOSFET_model

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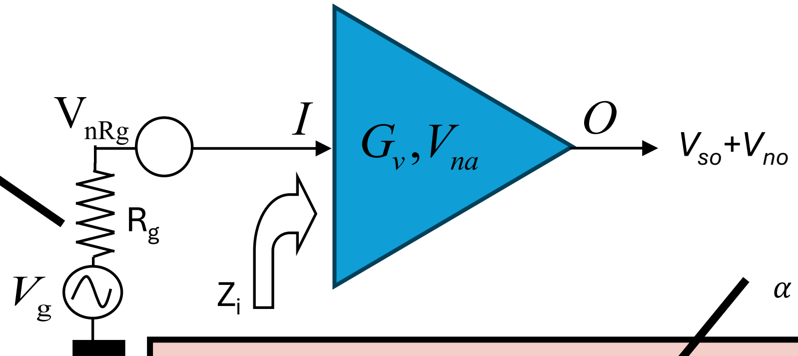
LNA Design considerations
Noise Factor

- NF is the signal to noise ratio (SNR) degradation (Eq. 1)

$$F = \frac{(S/N)_i}{(S/N)_o} \quad (1)$$

$$\overline{v_{nRg}^2} = 4KTR_g$$

$$V_{RMS\_nRg} = \sqrt{4KTR_g \Delta f}$$



$$\alpha = \left\| \frac{Z_i}{Z_i + R_g} \right\|$$

$$F = \frac{V_{si}^2 / V_{ni}^2}{V_{so}^2 / V_{no}^2} = \frac{V_g^2 / V_{nRg}^2}{V_{so}^2 / V_{no}^2} = \frac{V_{no}^2}{\alpha^2 . G_v^2 . V_{nRg}^2} = \frac{\overline{v_{no}^2}}{\alpha^2 . G_v^2 . \overline{v_{nRg}^2}}$$

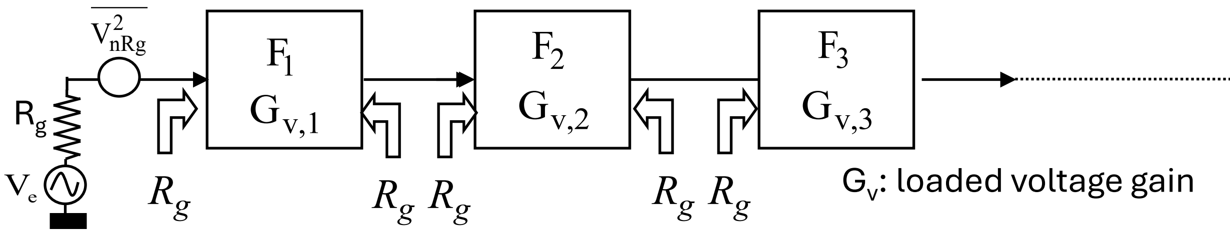
$$F = \frac{total\ output\ noise}{total\ output\ noise\ of\ the\ ideal\ (no\ aditive\ noise)\ device} \quad (2)$$

- NF also express the quantity of noise added by the stage regarding the noise delivered by the source (R_g) on Δf. (Eq. 2)

LNA Design considerations

Friss Formula

➢*RF Basis*



$$F = F_1 + \frac{(F_2 - 1)}{G_{v,1}^2} + \frac{(F_3 - 1)}{G_{v,1}^2 . G_{v,2}^2} + ...$$

This formula is valid only for real impedances and in case of power matching: (Z_s=Z_e=R_g)

In RFIC, impedances are complex and never equal. This formula cannot be us
However, the following statements remain valid in RFIC.

The gain of the first stages reduces the NF of the following ones.

=> The receiver chain must start by amplifiers

=> The NF of the first stage must be as low as possible

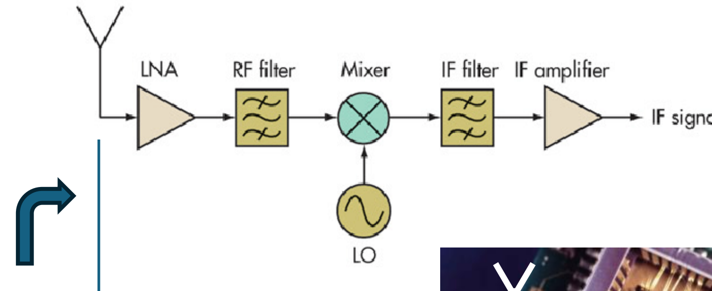
LNA

Note that lossy stages (G_v<1) increase the NF, especially when they are in front of the receiver chain ***(antenna filter, image rejection filter, antenna switch).***

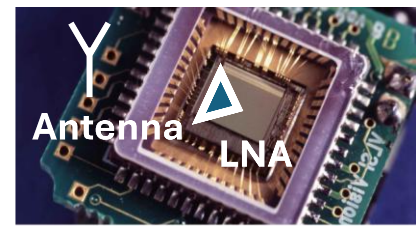
LNA Design considerations
Input patching

System point of vue

- LNA is the first device due to Friss formula
- Antenna is mainly 50 Ω.

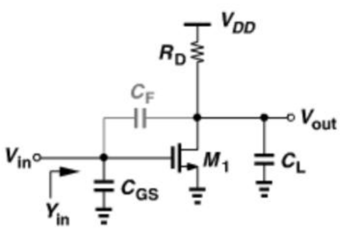


$$Z_{lna}=Z_g*$$



In CMOS

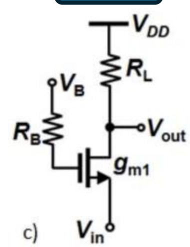
- Generally, the input impedance is capacitive Re (Y11) is very low
- For exemple : CS amplifier



$$\Re(Y_{in}) = R_D \| 1/g_m$$

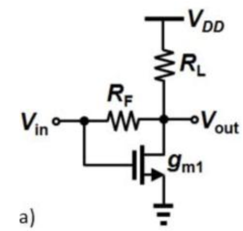
$$\Im(Y_{in}) = \frac{1}{C_{GS} C_F \omega}$$

CG



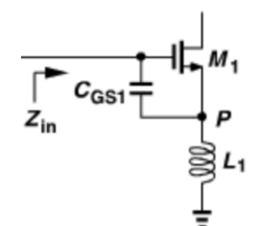
$$\Re(Z_{in}) = \frac{1}{g_{m1}}$$

R-Feedback



$$\Re(Z_{in}) = \frac{R_F}{1+|A_V|}$$

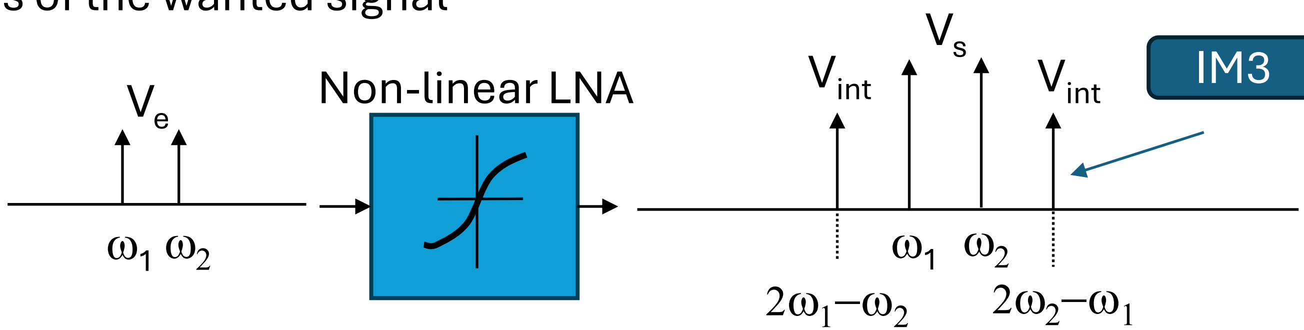
Inductive Degeneration

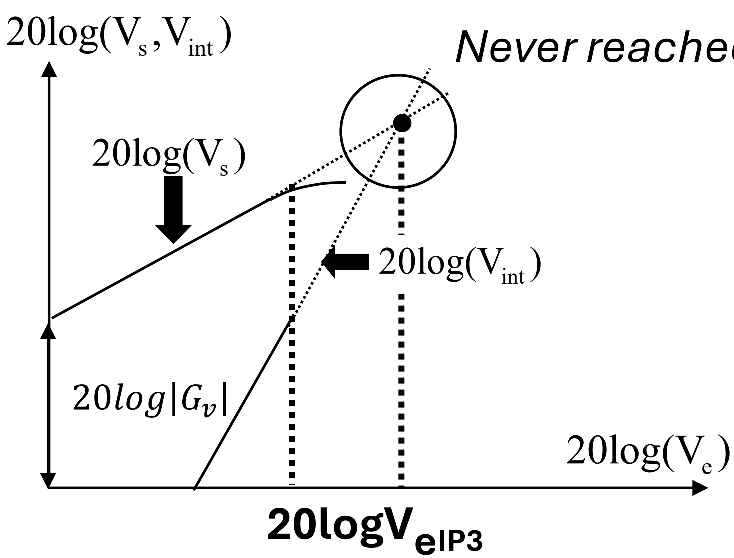


$$\Re(Z_{in}) = \frac{g_m L_1}{C_{GS}}$$

LNA Design considerations
Non-Linearities

ω_1 and ω_2 are 2 harmonics of the wanted signal





Never reached in measurement !

The IIP3 (V_{eIP3}) is the input signal level for which the output IM3 is equaling the fundamental harmonic (Vs) extrapolated from small signal (AC).

The IIP3 (V_{eIP3}) is related to the maximum power you can apply to your system

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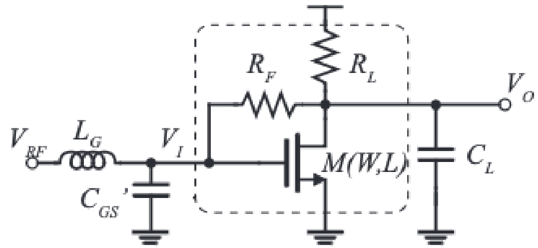
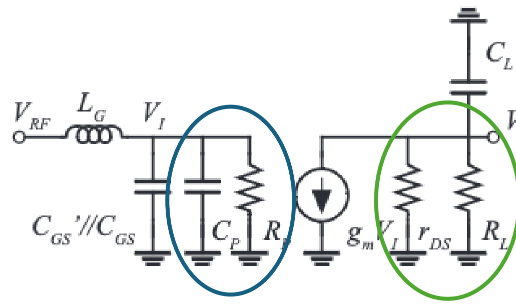
Resistive Feedback LNA
Topology

R-Feedback general considerations

- Simple
- Compact (No-inductors)
- Wideband
- RF allows to synthesize a real part in Zin
- LG and CGS' will help in cancelling the imaginary part
- while controlling Qin





Input impedance

$$Z_{IN} = L_G s + \left(\frac{1}{(C_{GS} + C'_{GS})s} // Z_P\right)$$

$$\boxed{\Re(Zp) = R_P = \frac{R_O + R_F}{1 + G_m R_O},}$$

$$\boxed{C_P = \frac{R_O^2 C_L (G_m R_F - 1)}{(R_O + R_F)^2}}$$

$$\boxed{R_O = \frac{R_L r_{DS}}{R_L + r_{DS}}}$$

$$\Re(Z_{IN}) = R_S = \frac{R_P}{(1 + Q_P^2)} = 50\ \Omega \qquad Q_P = R_P C_T \omega_0 \qquad C_T = C_{GS} + C'_{GS} + C_P$$

$$\Im(Z_{IN}) = 0 = L_G s + \frac{Q_P^2}{C_T s (1 + Q_P)^2}$$

Note :

$$\begin{cases} \Re(Zp) = \dfrac{1 + \left(\frac{f}{f_c}\right)^2}{\frac{1+G_m R_O}{R_O+R_F} + \frac{1}{R_F}\left(\frac{f}{f_c}\right)^2}, \\ \Im(Zp) = -\left(1 + \dfrac{R_F}{R_O}\right)^2 \dfrac{1 + \left(\frac{f}{f_c}\right)^2}{2\pi f C_L (G_m R_F - 1)} \end{cases}$$

Reduces For

$$\frac{f_c}{f} = N > 3$$

Resistive Feedback LNA

Topology

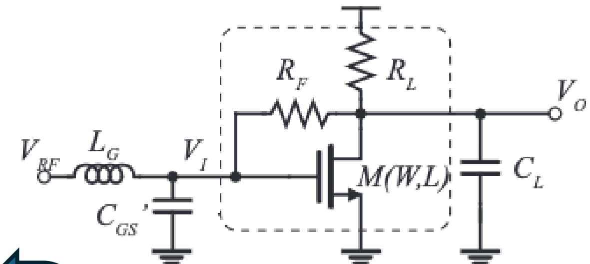
Voltage Gain

$$|G_o| = \left|\frac{V_O}{V_{RF}}\right| = \frac{|G_T|}{\sqrt{\left(1+\left(\frac{f_0}{f_c}\right)^2\right)}}$$

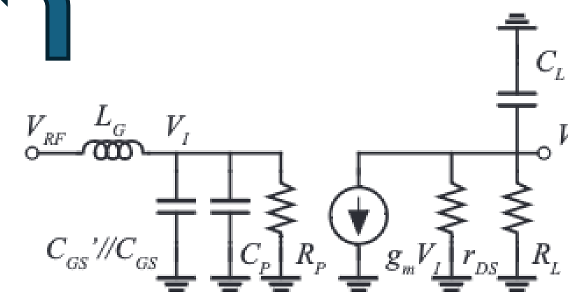
$$|G_T| = |G_v| Q_{IN} = \frac{(G_m R_F - 1) R_O}{(R_O + R_F)} \sqrt{1 + Q_P^2}$$

$$\frac{f_c}{f_0} = N > 3$$

$$Q_{IN} = V_I / V_{RF} \qquad Q_{IN} = \sqrt{1+Q_P^2} = \sqrt{\frac{R_O + R_F}{R_S(1+G_m R_O)}}$$



R_S
(the source resistance seen at the 50 Ω input)



BW

$$f_c = \frac{R_O + R_F}{2\pi R_O R_F C_L} = N f_0$$

Noise Figure

$$F = 1 + \frac{4\left(\frac{R_F}{Q_{IN}^2} + R_S\right)^2}{Q_{IN}^2 G_m R_S \left[\frac{R_F}{Q_{IN}^2} + R_S + \frac{G_m R_S R_F R_L}{R_F + R_L}\right]^2} \left[\gamma + \frac{1}{G_m R_L} + \frac{\left(1 + \frac{Q_{IN}^2 G_m R_S R_F}{R_F + Q_{IN}^2 R_S}\right)^2}{G_m R_F}\right]$$

$$\left(F_{min} = 1 + \frac{(1 + G_m\ ) {R_S}^2 R_F}{R_S\,(1 - G_m\ R_F)^2} + \frac{\gamma\, g_m\,(R_S + R_F)^2}{R_S\,(1 - G_m\ R_F)^2} + \frac{(R_S + R_F)^2}{R_S\, R_L (1 - G_m\ R_F)^2}\right)$$

IIP_3

$$V_{IIP3} = \frac{2}{Q_{IN}} \sqrt{\frac{2G_m}{G_{m3}}}$$

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What we need in ACM-2

Small signal parameters

Small signal (AC) parameters

- G_T, NF, IIP3 vs (G_m, G_{m3}, G_{DS})

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{I_S}{\phi_t} g_G = \frac{I_S}{n\phi_t} \frac{2(q_s - q_d) - i_d\,\zeta\left(\frac{q_s}{1+q_s} - \frac{q_d}{1+q_d}\right)}{1 + \zeta\,(q_s - q_d)}$$

$$g_{ds} = \frac{I_S}{\phi_t} g_D = \frac{I_S}{n\phi_t} \frac{2(q_s\sigma - q_d(\sigma - n)) - i_d\zeta\left(\sigma\frac{q_s}{1+q_s} - (\sigma - n)\frac{q_d}{1+q_d}\right)}{1 + \zeta(q_s - q_d)}$$

$$g_{m3} = \frac{I_S}{(n\phi_t)^3}\left\{\frac{\frac{2q_s}{(1+q_s)^3} - \frac{2q_d}{(1+q_d)^3} - \zeta n^2 g_{G2}\left(\frac{q_s}{1+q_s} - \frac{q_d}{1+q_d}\right) - \zeta\left[2n g_G\left(\frac{q_s}{(1+q_s)^3} - \frac{q_d}{(1+q_d)^3}\right) + i_d\left(\frac{q_d(1-2q_d)}{(1+q_d)^5} - \frac{q_d(1-2q_d)}{(1+q_d)^5}\right)\right]}{1 + \zeta\,(q_s - q_d)}\right\}$$

- Valid in all region (qs and qd shall be explored)

- We consider only saturation

$$q_{dsat} = q_s + 1 + \frac{1}{\zeta} - \sqrt{\left(1 + \frac{1}{\zeta}\right)^2 + \frac{2q_s}{\zeta}}$$

$$g_{msat} = \frac{2I_S}{n\phi_t}\frac{q_s}{1 + \zeta(q_s + 1)} \qquad g_{dsat} = \frac{\sigma}{n}\frac{2I_S}{\phi_t}\frac{q_s}{1 + \zeta(q_s + 1)} \qquad g_{msat3} = \frac{16 I_S}{(n\phi_t)^3}\frac{q_s}{(q_s + 1)^3}\frac{2 - 2\zeta q_s - 3\zeta q_s^2}{(q_s + 1)^4}$$

- It reduces the exploration to only qs.

What we need in ACM-2

Small signal parameters

Large signal (DC) parameters

- To compute the final voltages

$$V_T = V_{T0} - \sigma(V_{SB} + V_{DB})$$

$$V_P = \frac{V_{GB} - V_T}{n}$$

$$\frac{V_P - V_{S(D)B}}{\phi_t} = q_{s(d)} - 1 + \ln q_{s(d)}$$

- Sometime we'll use i_f in the code

$$i_d = i_f - i_r$$

$$q_{S(D)} = \sqrt{1 + i_{f(r)}} - 1$$

$$i_d = \frac{(q_s + q_d + 2)}{1 + \zeta|q_s - q_d|}(q_s - q_d)$$

$$I_D = I_S . i_d$$

$$I_S = \frac{\mu C'_{ox} n (U_T)^2}{2} \frac{W}{L}$$

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Inversion Level Based Method for R-Feedback LNA with ACM-2

General Approach :

Requirements
- GT, NF, IIP3, IDC Possible Tradeoff
- fo, CL, BW No Tradeoff

Design parameters
- ACM parameters for a fixed L
- $V_{T0}, I_S, n, \sigma, \zeta$

Design Variables (parameters)
- W, qs are first order design variables (qs = inversion level sets the energy efficiency and the voltages)
- RL, RF are second order design variables

Approach :
- Explore the different tradeoff (the design space) on GT, NF, IIP3 and IDC by playing with W, qs.
- In saturation region (only qs is needed)

$$g_{msat} = \frac{2I_S}{n\phi_t}\frac{q_s}{1+\zeta(q_s+1)} \qquad g_{msat3} = \frac{16I_S}{(n\phi_t)^3}\frac{q_s}{(q_s+1)^3}\frac{2-2\zeta q_s-3\zeta q_s^2}{(\zeta q_s+2)^4} \qquad g_{dsat} = \sigma\frac{2I_S}{n\phi_t}\frac{q_s}{1+\zeta(q_s+1)}$$

- Circuit equations depend on **G**m and ACM gives **g**m (normalized)…

Where we introduce W in the design space

$$|G_T| = \frac{(G_m R_F - 1)R_O}{(R_O+R_F)}\sqrt{\frac{R_O+R_F}{R_S(1+G_m R_O)}} \qquad G_{[m;DS]x} = \mu C'_{ox}\frac{(U_T)^{2-x}}{2}\frac{W}{L}g_{[m;DS]x} \qquad I_S = \mu C'_{ox} n\frac{(U_T)^2}{2}\frac{W}{L} \qquad I_{SL} = \frac{I_S}{W} = \mu C'_{ox} n\frac{(U_T)^2}{2L}$$

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Reducing the variables :

Starting from : $|G_T| = \frac{(G_m R_F - 1)R_O}{(R_O + R_F)}\sqrt{\frac{R_O + R_F}{R_S(1 + G_m R_O)}}$ $\quad G_T(G_m; R_0; R_F; R_S) = G_T(W; q_S; I_D; V_{DSAT}; V_{T0}; I_S; n; \sigma; \zeta; f_c; C_L)$

variables parameters

$$G_{[m;DS]x} = \mu C'_{ox}\frac{(U_T)^{2-x}}{2}\frac{W}{L}g_{[m;DS]x} \longrightarrow g_{msat} = \frac{2I_S}{n\phi_t}\frac{q_s}{1+\zeta(q_s+1)} \Rightarrow \boxed{G_m(q_S; W)}$$

$$\longrightarrow g_{dsat} = \frac{\sigma}{n}\frac{2I_S}{\phi_t}\frac{q_s}{1+\zeta(q_s+1)} \Rightarrow \boxed{G_{DS}(q_S; W)}$$

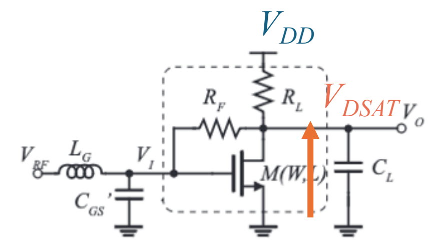
$$R_O = \frac{R_L r_{DS}}{R_L + r_{DS}} \longrightarrow G_{DS}(q_S; W)$$

$$R_L(I_D) = \frac{V_{DD} - V_{DSAT}}{I_D} \longrightarrow V_{DSAT} = \phi_t(\sqrt{1 + i_f} + 3)$$

$$i_f = (1 + q_s)^2$$

$$I_D = I_{SL} * W * i_f$$

$$\Rightarrow \boxed{R_0(q_S; W)}$$



$$R_F = \frac{R_0}{2\pi R_0 C_L f_c - 1} \Rightarrow \boxed{R_F(q_S; W)\Big|_{f_c}}$$

$$\left(f_c = \frac{R_O + R_F}{2\pi R_O R_F C_L}\right)$$

$$\Rightarrow \boxed{G_T(G_m; R_0; R_F; R_S) = G_T(W; q_S)}$$

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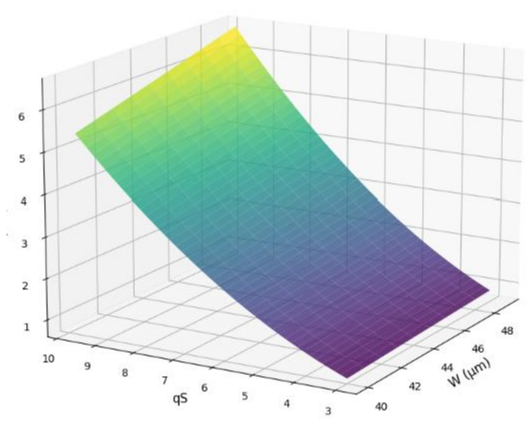
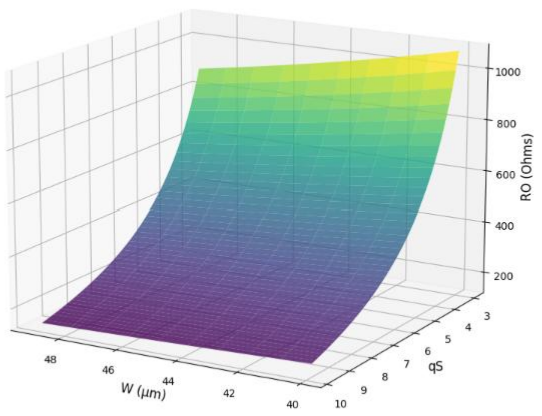
Finally : $I_D(q_s;W)$; $R_F(q_s;W)$; $R_0(q_s;W)$; $G_T(q_s;W)$

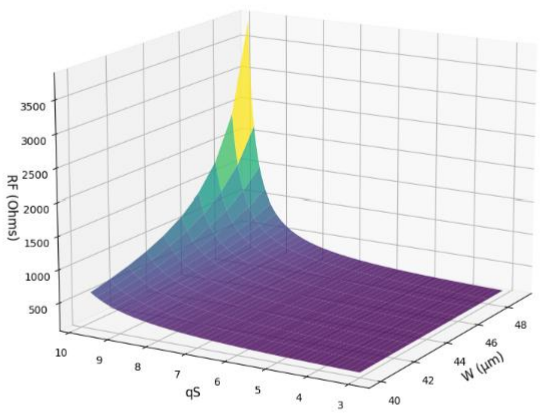
$I_D(q_s;W)$



$R_0(q_s;W)$



$R_F(q_s;W)$



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Computing GT, F and IIP3:

Finally : $|G_T| = \frac{(G_m R_F - 1)R_O}{(R_O + R_F)}\sqrt{\frac{R_O + R_F}{R_S(1 + G_m R_O)}}$

$\boxed{G_T(q_s; W)|_{f_c; C_L}}$

$$V_{IIP3} = \frac{2}{Q_{IN}}\sqrt{\frac{2G_m}{G_{m3}}}$$

$\boxed{IIP_3(q_s; W)|_{f_c; C_L; R_S}}$

$$F = 1 + \frac{4\left(\frac{R_F}{Q_{IN}^2} + R_S\right)^2}{Q_{IN}^2 G_m R_S \left[\frac{R_F}{Q_{IN}^2} + R_S + \frac{G_m R_S R_F R_L)}{R_F + R_L}\right]^2}\left[\gamma + \frac{1}{G_m R_L} + \frac{\left(1 + \frac{Q_{IN}^2 G_m R_S R_F}{R_F + Q_{IN}^2 R_S}\right)^2}{G_m R_F}\right]$$

$\boxed{F(q_s; W)|_{f_c; C_L; R_S}}$

with $G_T(q_s; W)|_{f_c; C_L}$

$\boxed{F(G_T; W)}$

Remember :

$$Q_{IN} = V_I/V_{RF} = \sqrt{1 + Q_P^2} = \sqrt{\frac{R_O + R_F}{R_S(1 + G_m R_O)}}$$

Inversion Level Based Method for R-Feedback LNA with ACM-2

Exploring the design space:

Setting GT (or NF, or IIP3) helps to build 2D plots.

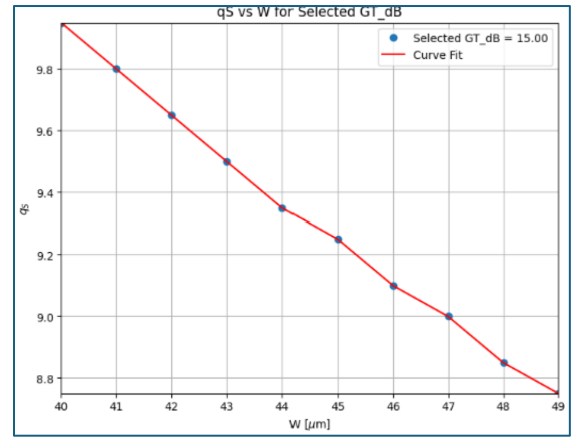
For a particular G_T **=> *We get the relationship q_S<=>W***

=> *We plot*

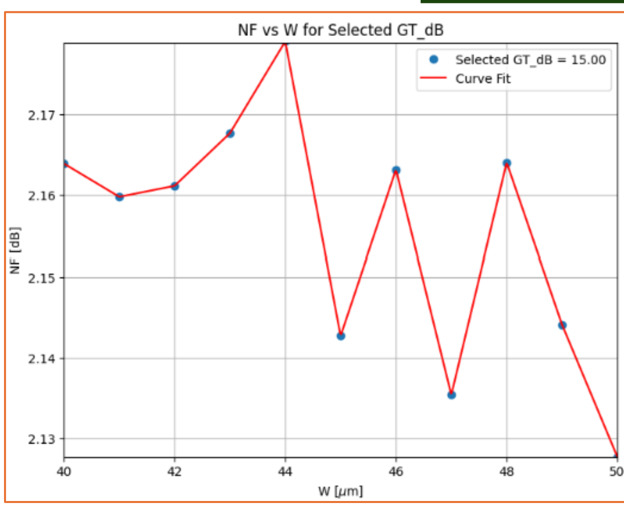
=> *We plot $IIP3(W)$*

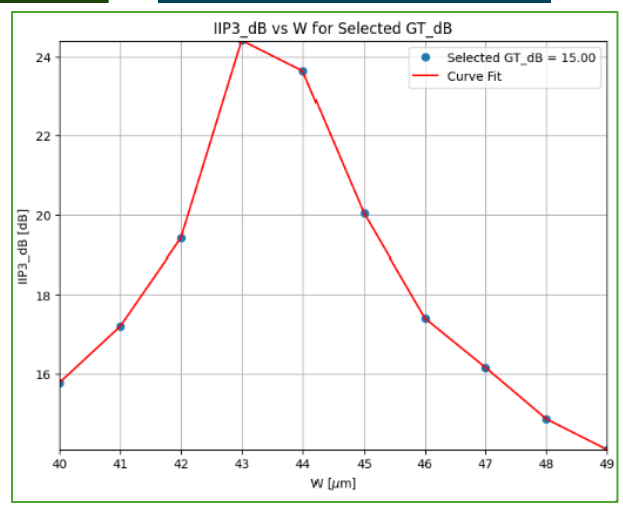
And We already have I_D

q_S



$W(\mu m)$





Inversion Level Based Method for R-Feedback LNA with ACM-2

Setting the final value:

- We choose W, that gives q_S for a given G_T.
- $(W;q_S)$ gives R_0, R_L, I_D, G_m, V_{DSAT} and V_G

Input Matching

- *With* R_0, R_F, G_m => R_P $\quad \Re(Zp) = R_P = \dfrac{R_O + R_F}{1 + G_m R_O},$
- *With* R_S *and* R_P *calculate* Q_P $\quad \Re(Z_{IN}) = R_S = \dfrac{R_P}{(1 + Q_P^2)} = 50\ \Omega$
- *With* Q_P *calculate* C_T *and* C_{GS}' $\quad Q_P = R_P C_T \omega_0 \quad C_T = C_{GS} + C'_{GS} + C_P \quad C_P = \dfrac{R_O^2 C_L (G_m R_F - 1)}{(R_O + R_F)^2}$
- *With* C_T *calculate* L_G $\quad \Im(Z_{IN}) = 0 = L_G s + \dfrac{Q_P^2}{C_T s (1 + Q_P)^2}$

Validation

Now, let's simulate with a real PDK