SIMPLE NOISE FORMULAS FOR MOS ANALOG DESIGN.

Alfredo Arnaud(1), *Carlos Galup-Montoro*(2)

(1) GME –IIE, Facultad de Ingeniería, Universidad de la República , Montevideo – Uruguay.
(2) LCI, Departamento de Engenharia Eletrica,Universidade Federal de Santa Catarina.

ABSTRACT

The designer needs simple and accurate models to estimate noise in MOS transistors as a function of their size, bias point and technology. In this work, we present a simple, continuous, physics-based model for flicker noise. We review also thermal noise and we examine the behavior of the corner frequency (f_c) in terms of the bias point. The expressions that are presented are simple and valid in all the operating regions, from weak to strong inversion, constituting a useful set of equations for low noise analog design. Finally we examine the design of two low noise circuit elements, fabricated in a 0.8µm technology.

1. INTRODUCTION

Thermal noise does not vary with the frequency and it is originated by thermal movement of carriers. Flicker noise or simply 1/f noise is such that its power spectral density (PSD) varies with frequency in the form $S(f) = K/f$ [1-4]. It is quite well accepted that the sources of low frequency noise are mainly carrier number and mobility fluctuations due to random trapping – detrapping of carriers in energy states near the surface of the semiconductor [2,3]. However, the exact mechanism and the statistics of the resulting noise current, as well as how it is related to technology parameters such as doping concentration or surface quality, are not yet clear.

To calculate total current noise in a MOS transistor, the noise current caused by trapping-detrapping of carriers in each channel element must be integrated. To perform this integration without further approximations we will employ the MOSFET model from reference [5]. The fundamental approximation of this model is the linear dependence of the inversion charge density $Q_I^{'}$ on the surface potential ϕ_S :

$$dQ_I^{'} = \left(C_b^{'} + C_{ox}^{'}\right)d\phi_S = nC_{ox}^{'}d\phi_S \,, \tag{1}$$

where *n* is the slope factor slightly dependent on the gate voltage, $C_b^{'}, C_{ox}^{'}$ are the inversion layer and oxide capacitance per unit area. The drain current I_D in a long-channel transistor is calculated with (1) and the charge sheet approximation [6]:

$$I_D = \frac{\mu W}{nC_{ox}^{'}}\left(-Q_I^{'} + \phi_t nC_{ox}^{'}\right)\frac{dQ_I^{'}}{dx} \,. \tag{2}$$

W, L are transistor dimensions, μ is the effective mobility.

2. FLICKER NOISE MODEL

To integrate the elementary noise contributions along the channel we split the transistor in Fig.1 into 3 series elements: the upper transistor with source transconductance $g_{msu} = -\mu \frac{W}{L-d} Q_{IX}^{'}$ [5,6], the lower transistor with drain transconductance $g_{mdl} = -\mu \frac{W}{d} Q_{IX}^{'}$, and a noisy element dA modeled as a noisy resistor ($Q_{IX}^{'}$ is $Q_I^{'}$ evaluated at the point X in the channel). If we represent by i_{dA} the noise current produced by the element dA , then one can calculate the resulting effect of i_{dA} on the drain current noise, using small signal analysis: $\Delta I_d = (\Delta x/L).i_{dA}$. Thus, if $S_{dA}(x,f)$ is the P.S.D. of $i_{dA}\,.\,\Delta x$, then the total noise current of the transistor is:

$$S_{I_d}(f) = \frac{1}{L^2}\int_0^L S_{dA}(x,f).dx \tag{3}$$

Equation (3) is quite general and could be employed with any model for the noise of single channel elements such as the thermal noise model, or the carrier number fluctuation model. To calculate the total drain noise produced by the carrier number fluctuation we use the same physical hypothesis as Reimbold [1]; so it is possible to write the PSD of the fluctuations ΔN of the number N of carriers per unit area, in the channel area dA:

$$S_{\Delta N}(f) = \frac{N_{ot}.\left(Q_I^{'}/\phi_t\right)^2}{dA.\left(Q_I^{'} - nC_{ox}^{'}\phi_t\right)^2} \tag{4}$$

N_{ot} is the effective number of traps [4], a technology parameter to be adjusted. By means of small signal analysis, it is possible to relate these fluctuations to the current: $i_{dA} = I_D.\Delta N/N$. The PSD of i_{dA} is then introduced into Eq.(3) to calculate the total flicker noise,

$$S_{I_d} = \frac{q^2 N_{ot} I_D^2}{W.L^2.f}\int_0^L \frac{dx}{\left(nC_{OX}^{'}\phi_t - Q_I^{'}\right)^2} = \frac{q^2 N_{ot}\mu I_D}{nC_{OX}^{'}L^2 f}\int_{Q_{IS}^{'}}^{Q_{ID}^{'}} \frac{dQ_I^{'}}{nC_{OX}^{'}\phi_t - Q_I^{'}} \tag{5}$$

the integration over the channel length in (5) has changed into integration over the channel charge density with the aid of (2). It follows:

$$\frac{S_{I_d}}{I_D^2} = \frac{q^2 N_{ot}\mu}{L^2 nC_{OX}^{'} I_D}.\ln\left[\frac{nC_{OX}^{'}\phi_t - Q_{IS}^{'}}{nC_{OX}^{'}\phi_t - Q_{ID}^{'}}\right].\frac{1}{f} \tag{6}$$

An expression similar to (6) is used in BSIM3 to model strong inversion noise due to charge trapping [2], but we must emphasize that (6) is valid for any inversion level, including moderate inversion.

0-7803-7762-1/03/$17.00 ©2003 IEEE

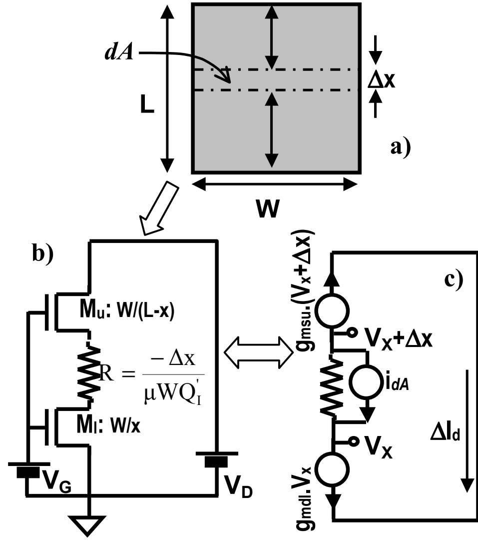

Figure 1. a) Element $dA = W.dx$ in a MOS transistor channel b) the transistor is separated into 3 series components c) Small signal analysis to calculate the effect of the noisy element dA in the drain current.

In weak inversion, $Q'_{IS}, Q'_{ID} << nC'_{OX}\phi_t$. With a first order series expansion, one can rewrite (6) as ($N^* = nC'_{OX}\phi_t / q$ [4]):

$$\frac{S_{I_d}}{I_D^2} = \frac{N_{ot}}{WLN^{*2}} \cdot \frac{1}{f} \tag{7}$$

In strong inversion in saturation, S_{I_d} increases linearly with I_D as predicted by (6) if we neglect the variation of the logarithmic term.

$$S_{I_d} \approx \frac{3 I_D q^2 N_{ot} \mu}{L^2 n C'_{ox}} \cdot \frac{1}{f} \tag{8}$$

Some 1/f noise measurements have been performed in MOS transistors covering all the regions of operation with the aid of a low noise amplifier and spectrum analyzer. In all cases the PSD closely follows a 1/f dependence. This is consistent with the assumption of a uniform spatial distribution of the traps inside the oxide [3]. Noise spectrums were acquired from 0.3 to 30Hz, where the PSD is high enough to measure flicker noise particularly in weak inversion (avoiding also the effect of the AC line). For the calculation of the theoretical model, the charge densities $Q'_{IS(D)}$ were estimated with a circuit simulator using the ACM model [5]. The parameter N_{ot} of the model in (6) is adjusted to best fit the measurements, with the result $\overline{N}_{otN} = 2x10^7 cm^{-2}$, $\overline{N}_{otP} = 3x10^7 cm^{-2}$, for the N and PMOS respectively. Fig.2 contains simulation and measurements of normalized flicker noise PSD (S_{I_d} / I_D^2) for a saturated NMOS of a 0.8μ CMOS process, with an aspect ratio W/L=200μ/5μ in order to be able to comfortably characterize weak inversion operation. Note here the plateau in weak inversion. Fig.3 was obtained for a W/L=20/10 NMOS transistor, fabricated in the same 0.8μ process (but different run), from the linear region up to saturation with V_G=3.3V.

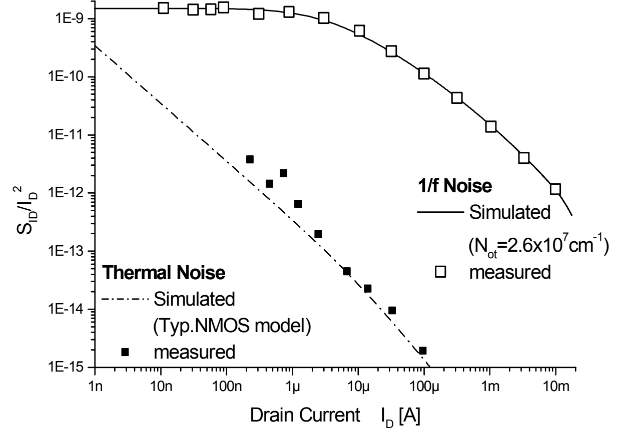

Figure 2. Normalized flicker (thermal) PSD $S_{I_d(iw)} / I_D^2$ at f=1Hz for a saturated NMOS (W/L=200μ/5μ).

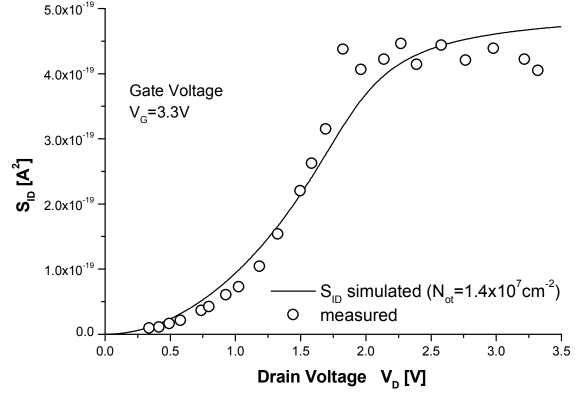

Figure 3. Flicker noise PSD at f=1Hz, for a W/L=20/10 NMOS transistor, from linear region up to saturation.

3. THERMAL NOISE MODEL

Let us consider the classical model for MOS thermal noise [6]:

$$S_{iw} = \frac{-4k_B T \mu Q_I}{L^2} \tag{9}$$

where Q_I is the total inversion charge. With the same procedure used in Eq.(5), it is possible to calculate the thermal noise in terms of Q'_{IS}, Q'_{ID} [7]:

$$S_{iw} = \frac{4k_B T \mu^2 W^2}{nC'_{ox}L^2} \cdot \left[\frac{1}{3}\left(Q'^3_{ID} - Q'^3_{IS}\right) + \frac{nC'_{ox}\phi_t}{2}\left(Q'^2_{IS} - Q'^2_{ID}\right) \right] \tag{10}$$

<u>In weak inversion</u>, supposing that $Q'_{IS} \approx \left(\frac{ng_m L}{\mu W}\right)^2 >> Q'_{ID}$, $nC'_{ox}\phi_t Q'^2_{IS} >> Q'^3_{IS}$, is possible to rewrite Eq.(14) as:

$$S_{iw} = 2nk_B T g_m \quad (11)$$

<u>In strong inversion</u>, supposing that $nC'_{ox}\phi_t Q'^2_{IS} << Q'^3_{IS}$, $Q'_{IS} >> Q'_{ID}$, $I_D = \frac{ng_m^2 L}{2W\mu C'_{ox}}$, is possible to rewrite Eq.(14) as:

$$S_{iw} = \frac{8}{3} nk_B T g_m \quad (12)$$

In the plot of Fig.2 the estimated and measured values of the normalized PSD of white noise are shown. These measurements were obtained with the same experimental setup, but at a frequency of several kHz to avoid the flicker noise effect.

4. CORNER FREQUENCY f_c

The corner frequency at which the flicker noise and thermal noise have the same value, has particular importance in analog design. It can be calculated directly in terms of Q'_{IS}, Q'_{ID} from Eqs.(6,10) but with the aid of Eqs.(7,8,11,12) this expression acquires a simpler form:

$$f_c = \frac{\gamma g_m}{WLC'_{ox}} \cdot \frac{N_{ot}}{N^*} \approx \frac{\pi}{2} f_T \cdot \frac{N_{ot}}{N^*} \quad (13)$$

with $\gamma = \frac{1}{2}$ at W.I and $\gamma = \frac{9}{16} \approx \frac{1}{2}$ at strong inversion. Note that the corner frequency in Eq.(13) is related also to the transition frequency f_T of the transistor [5], which results in a useful approximation for the designer. In Fig.4 we present the simulated and measured values for the corner frequency in a saturated NMOS transistor at various bias current values.

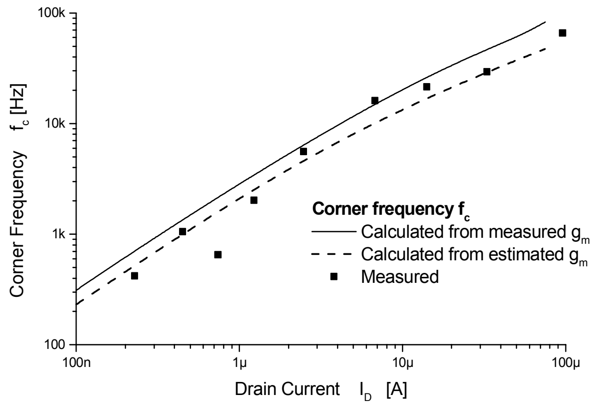

Figure 4. Estimated and measured value of the corner frequency f_c, for a W/L=200/5 NMOS transistor.

The dots are the measured values, the continuous line is f_c calculated using Eq.(13) with the measured value for g_m while the dashed line estimates [5]:

$$g_m = \frac{2.I_S.i_f}{n\phi_t.\left(\sqrt{1+i_f}+1\right)} \quad (14)$$

with $I_S = \frac{1}{2}\mu C_{OX} n\phi_t^2 (W/L)$, and i_f is the normalized current that reflects the inversion level of the transistor[5]. Both simulation and measurements predict that the corner frequency decays as the transistor goes into deep weak inversion. At extremely low currents, even at very low frequency thermal noise will dominate; this is in accordance with the noise measurements obtained in [8]. On the other hand, at strong inversion flicker noise is important even at elevated frequencies.

5. DESIGN EQUATIONS AND EXAMPLES

From the designer perspective, Eqs.(6-8, 10-13) are a very useful tool. For a single transistor the current noise is $S_i = 2nk_B T.g_m(1 + f_c/f)$; and the total noise seen at the gate can be estimated for a defined bandwidth between two frequencies $f_1 < f < f_2$:

$$\bar{v}_n^2 = \frac{2nk_B T}{g_m} \cdot \int_{f_1}^{f_2} \left(1 + \frac{f_c}{f}\right) df = \alpha.\frac{1}{g_m} + \beta.\frac{1}{WL} \quad (15)$$

with $\alpha = 2nk_B T(f_2 - f_1)$, $\beta = \frac{nk_B T}{C'_{ox}} \cdot \frac{N_{ot}}{N^*} Ln\left(\frac{f_2}{f_1}\right)$. In a more complex topology the noise equations vary but, in general, it will be possible to identify a term related to the transconductance of the transistors (associated to the thermal noise), and a term inversely proportional to the area of the transistors (associated to flicker noise). Take the example of the transconductor of Fig.5a. In this case the total current noise is:

$$S_{i_Tot}(f) = 4nk_B T.\left[\left(B^2 g_{m1} + (B^2 + B)g_{m2} + g_{m3}\right) + \ldots \right. \quad (16)$$

$$\left. + \frac{1}{2N^* C'_{ox}.f}\left(\frac{B^2 N_{otP} g_{m1}^2}{(WL)_1} + \frac{(B^2 + B)N_{otN} g_{m2}^2}{(WL)_2} + \frac{N_{otP} g_{m3}^2}{(WL)_3}\right)\right]$$

and the total input noise voltage is:

$$\bar{v}_n^2 = 4nk_B T.\left[\frac{(f_2 - f_1)}{g_{m1}}\left(1 + \left(1 + \frac{1}{B}\right)\frac{g_{m2}}{g_{m1}} + \frac{1}{B}\frac{g_{m3}}{g_{m1}}\right) + \ldots \right. \quad (17)$$

$$\left. \frac{L(f_2/f_1)}{2N^* C'_{ox}}\left(\frac{N_{otP}}{(WL)_1} + \frac{\left(1 + \frac{1}{B}\right)N_{otN}}{(WL)_2} \cdot \frac{g_{m2}^2}{g_{m1}^2} + \frac{N_{otP}}{(WL)_3} \cdot \frac{g_{m3}^2}{B^2 g_{m1}^2}\right)\right]$$

Note from Eq.(17) that each term may become the most significant or negligible depending on the copy factor B, the invertion level, or the area of the transistors. It is not necessarily true that the flicker noise is reduced for a PMOS input pair, and the mirrors have a significative noise contribution. A design rule is to roughly estimate the weight of each term and reduce the most significant ones according to a defined area and current budget. In the plot of Fig.5b it is shown the estimated and measured noise current of the OTA of Fig.5a designed according to (17) to operate in a range, from 3 to 20kHz with a total noise less than 20µV. The excess noise between predicted and

measured values can be assigned to inaccuracy in transistor parameters, and to the excess noise due to short channel transistors with $L \approx 1\mu$ in the circuit.

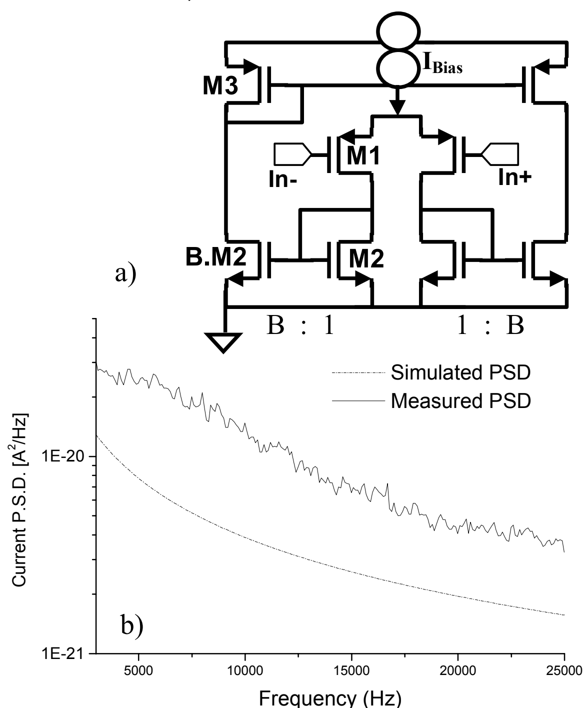

Figure 5. a) Schematic (B=3, I_{Bias}=60μA) b) estimated (16) and measured noise PSD for a symmetrical OTA.

The second example is a preamplifier for a piezoresistive accelerometer [9]. In this case $f_1 = 0.5Hz, f_1 = 7Hz$, and the total noise $\bar{v}_n \leq 0.25\mu V$, so (17) yields to prohibitive transistor areas to reduce flicker noise. The selected solution to avoid 1/f noise is to implement a chopper amplifier with the topology used in [10] where the amplifying element is a resonant g_m-C filter with the topology of Fig.6. The noise introduced by g_{m1} is dominant and a design criteria is: a) the input pair is in weak inversion to minimize thermal noise with the available current budget b) the area of this transistor is selected to fix the corner frequency f_c (13) slightly greater than the operating frequency of the chopper ($f_{Ch} = 8kHz$), according to [10] c) the rest of the elements of g_{m1} are sized with the same criteria. The measured noise for the resonant filter at the input resulted in $81 \frac{nV}{\sqrt{Hz}}$ at the operating frequency while $100 \frac{nV}{\sqrt{Hz}}$ were estimated in the design process.

6. CONCLUSIONS

Based on common physics hypotheses but with the aid of an advanced compact transistor model, we integrate the contribution to the transistor noise current of all the noisy elements in the MOS channel resulting in a simple, single piece, flicker noise model, continuous in all the operation regions from weak to strong inversion. Thermal noise calculation has also been discussed as well as the estimation of the corner frequency f_c using the new model for flicker noise. It has been demonstrated that it is directly related to the transistor transition frequency. Some measurements and simulations are presented.

Flicker, thermal and corner frequency equations were reduced to a simple set of equations that allow the designer to estimate the total noise of a circuit as well as to explore the trade-offs in low-noise design. Two simple examples were presented that illustrate the use of this simple set of equations.

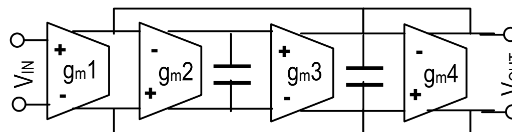

Figure 6. a) Schematic of a g_m-C resonant amplifier.

7. ACKNOWLEDGEMENT

The authors would like to thank Prof. Márcio C. Schneider and Ing.Pablo Aguirre for helpful suggestions and support.

8. REFERENCES

[1] G. Reimbold, "Modified 1/f trapping noise theory and experiments in MOS transistors biased from weak to strong inversion-influence of interface states," IEEE Trans. Electron Devices, vol. ED-31, pp. 1190–1198, Sept. 1984.

[2] K. K. Hung, P. K. Ko, C.Hu, Y.C.Cheng, "A physics-based MOSFET noise model for circuit simulators", IEEE Trans. Electron Devices, vol. 37, no.5, pp.1323–1333, May. 1990.

[3] Chang, J., Abidi, A. A. and Viswanathan, C. R., "Flicker noise in CMOS transistors from subthreshold to strong inversion at various temperatures", IEEE Trans. Electron Dev., vol. 41(11), 1965-1971, 1994.

[4] Y. Nemirovsky, I. Brouk, and C. G. Jakobson, "1/f noise in CMOS transistors for analog applications", IEEE Trans. Electron Devices, vol. 48, no.5, pp.921-927, May. 2001.

[5] A. I. A. Cunha, M. C. Schneider, C. Galup-Montoro, "An MOS transistor model for analog circuit design", IEEE JSSC, vol.33, no.10, pp.1510-1519, Oct.1998.

[6] Tsividis, Y. P., *Operation and Modeling of the MOS Transistor*. McGraw Hill, 1999.

[7] A.Emira, E.Sánchez-Sinencio, M.C.Scneider, "Design tradeoffs of CMOS current mirrors using one-equation for all-region model" Circuits and Systems, 2002. ISCAS 2002. IEEE Int. Symposium on , Volume: 5 , 2002 Page(s): 45 -48

[8] B.Linares-Barranco, T.Serrano-Gotarredona, "Reliable Handling of Femto-Ampere Currents in Standard CMOS", Procs.28th European Solid-State Circ.Conf., ESSCIRC 2002.

[9] P.Aguirre, A.Arnaud, "Diseño de un filtro pasabandas para amplificador chopper para bajo ruido y micro-consumo", Proc.VIII Iberchip Conf. ISBN970-93260-0-7 .

[10] C.C.Enz, G.C.Temes, "Circuit Techniques for reducing the effects of Op-Amp Imperfections: Autozeroing , Correlated Double Sampling, and Chopper Stabilization", Proceedings of the IEEE, Vol.84, Nº11, Nov.1996.