ISFETs: theory, modeling and chip for characterization

Rodrigo Wrege, Márcio Cherem Schneider, Janaina Gonçalves Guimarães and Carlos Galup-Montoro

***Abstract*—The ISFET (Ion Sensitive Field Effect Transistor) is a structure based on the MOSFET (Metal Oxide Semiconductor Field Effect Transistor) which is capable of measuring ionic concentration of a solution. The ISFET has been used for such areas as DNA sequencing, viruses and bacteria detection. The basic idea behind the ISFETs emerged in 1970, but a deeper understanding of some of its non-idealities and the development of architectures to reduce their effects are still needed. For that reason, this work revisits the basic principles of ISFET operation. The ISFET modeling using the binding site theory, Gouy-Chapman-Stern model and the Advanced Compact Model of the transistor is introduced and implemented in Matlab®. Furthermore, the details of a chip designed on the Virtuoso® platform, aimed at characterizing the ISFETs on the SilTerra D18V technology, are presented. Simulation results estimate an average sensitivity of 45.3 mV/pH for the designed devices over a pH range from 1 to 10. The chip sent for fabrication was kindly supported by Chipus Microeletrônica S.A. and SilTerra Malaysia Sdn Bhd.**

***Index Terms*—ISFETs, modelling, pH sensor.**

I. Introduction

The importance of detecting viruses, bacteria, early stages of cancer, analyzing biochemical fluids, and performing DNA sequencing is undeniable. To accomplish this, proper techniques and sensors needed to be developed. Chemical sensors implemented in CMOS (Complementary Metal Oxide Semiconductor) technology have the advantages of reduced dimensions, low power consumption, and low fabrication cost. A sensor that has all these advantages and has been applicable in such areas as those mentioned above is the ISFET (Ion-Sensitive Field-Effect Transistor).

ISFETs are based on MOSFETs (Metal Oxide Semiconductor Field Effect Transistors), in which the floating gate terminal is covered with a sensitive membrane in contact with a solution polarized by a reference electrode. As a result, the ISFET threshold voltage changes in accordance with ion concentration (pH) of the solution.

The basic idea behind the ISFET was introduced in 1970 [1], but a way to implement it in a standard CMOS technology was only devised in 1999 [2]. The technique consists in connect the transistor gate to the top metal which is in contact with the passivation layer, usually Si_3N_4, as shown in Fig. 1.

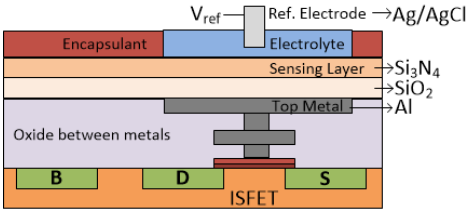

Fig. 1. ISFET structure in a standard CMOS technology.

This paper presents the theory and modelling of the ISFET in Section II . Section III describes the chip designed for characterization of the ISFETs. Simulations and results are discussed in Section IV. Conclusions and future work are presented in Section V.

II. Theory and Modeling of ISFETs

A. Main non-idealities

ISFETs have some non-idealities. One of them is the offset in the threshold voltage due to trapped charges at the floating gate and at the passivation layer, which contribute to an increase of the mismatch between devices. The threshold voltage of ISFETs also presents a temporal drift of order of 1.5 to 8.5 mV/h [3]. Temperature effects can also be detrimental to the determination of the pH. According to [4] a 7 K temperature variation around room temperature is comparable with a 1 pH variation. ISFETs suffer from both the chemical and the MOSFET noise. Different architectures and techniques have been used to overcome the effects of those non-idealities [4].

B. Reference electrode

The reference electrode polarizes the solution in contact with the ISFET; thus, the electrode impacts the ISFET's performance [5]. The potential of the usually applied Ag/AgCl electrode, relative to the standard hydrogen electrode (SHE), is 0.19 V [5]. The SHE absolute potential is (4.44 ± 0.02) V at 25°C [6].

However, the great dimensions of the standard Ag/AgCl electrode are an obstacle to its application for small volumes, of the order of tens of µL. Alternatives to the Ag/AgCl electrode include miniaturization, which has a complex

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construction [5], or the use of quasi-reference electrodes, composed by a metal (pad or a wire) in direct contact with the test solution. In this case, the potential is dependent of the solution composition, but this inconvenience can be circumvented by differential measurements [7].

C. ISFET modeling

The ISFET's sensitivity to the solution's ion concentration is modeled using the site-binding theory and the Gouy-Chapman-Stern (GCS) double layer model. These theories are combined with the transistor model to describe the current and voltages in the ISFET's terminals.

The relationship between the charge density in the electrolyte/insulator interface (σ_o) and in the diffuse layer described in the CGS model (σ_d) can be defined [8] as

$$\sigma_{\mathrm{d}} = -\sigma_{\mathrm{o}} = -C'_{\mathrm{eq}}\,\phi_{eo} \tag{1}$$

where C'_{eq} is the total capacitance per unit area in the electrolyte/insulator interface and $\varnothing_{eo}$ the interface potential.

1) Site-Binding and GCS theories

The charge density σ_o can be obtained through the site-binding theory, which describes the equilibrium between SiOH sites and H^+ ions in solution. According to this theory, σ_o is given [9] by

$$\sigma_{\mathrm{o}} = \left(\frac{H_s^2 - K_- K_+}{H_s^2 + K_+ H_s + K_- K_+}\right) qNsil + \left(\frac{H_s}{H_s + K_n}\right) qNnit \tag{2}$$

where q is the electron charge, $Nsil$ the number of silanol (SiH_3OH) sites per area, $Nnit$ the primary amines sites per area, K_+, K_- and K_n are the dissociation constants of the passivation layer and H_s is the proton concentration in the insulator surface, which is related to the ion concentration in the solution (H_b) through the Boltzmann equation:

$$H_s = H_b \exp\left(-\phi_{eo}/\phi_t\right) \tag{3}$$

where $\varnothing_t$ is the thermal voltage. The values of the parameters for Si_3N_4 layer are listed in Table I [9].

The charge density σ_d and the capacitance C'_{eq} can be obtained using the GCS theory. This model considers the charges in two layers: the Helmholtz layer, with charges near the insulator surface and the boundary in the Outer Helmholtz Plane (OHP); and the Gouy-Chapman layer with diffuse charges following the Boltzmann distribution [10]. The charge density σ_d is obtained by [10]:

$$\sigma_{\mathrm{d}} = -\sqrt{8\mathrm{kTn}^0 \varepsilon_r \varepsilon_0}\,\sinh\left(z\phi_2/(2\phi_t)\right) \tag{4}$$

where ε_0 is the permittivity of free space, ε_r the relative dielectric constant of the medium, k is the Boltzmann constant, T the absolute temperature and $\varnothing_2$ the potential in the OHP.

The capacitance C'_{eq} in this model is given by [10]:

$$\frac{1}{C'_{eq}} = \frac{x_2}{\varepsilon_r \varepsilon_0} + \frac{1}{\sqrt{2\varepsilon_r \varepsilon_0 z^2 q^2 n^0/(kT)}\cosh\left(zq\phi_2/(2kT)\right)} = \frac{1}{C'_H} + \frac{1}{C'_G} \tag{5}$$

with n^0 the bulk solution concentration ($=NaC$, with Na the Avogrado's constant and C the concentration in mol/m³), x_2 is the OHP distance from electrode and z is the magnitude of the ionic charge. It is possible to see that C'_{eq} is a series association between a linear capacitance (C'_H) and a non-linear capacitance (C'_G). C'_H and C'_G are the Helmholtz and the Gouy-Chapman capacitances per unit area, respectively.

The potentials $\varnothing_{eo}$ and $\varnothing_2$ can be obtained with the following equation system:

$$\begin{cases} \phi_{eo} = \dfrac{\sigma_{\mathrm{o}}}{C'_{\mathrm{eq}}} \\ \phi_2 = \phi_{eo} + \dfrac{\sigma_{\mathrm{d}}}{\varepsilon_r \varepsilon_0 / x_2} \end{cases} \tag{6}$$

Once $\varnothing_{eo}$ has been determined, the transistor model is used to obtain the ISFET's voltages and currents.

2) ACM model

According to the Advanced Compact Model (ACM), valid in all transistor regions of operation [11], the voltages in the terminals are related to the direct and reverse inversion levels (i_f and i_r respectively) by:

$$V_{\mathrm{P}} - V_{\mathrm{S(D)}} = \phi_t\left(\sqrt{1+i_{f(r)}} - 2 + \ln\left(\sqrt{1+i_{f(r)}} - 1\right)\right) \tag{7}$$

where V_S *and* V_D are the source and drain voltage, and V_P is the pinch off voltage given by:

$$V_{\mathrm{P}} \cong \frac{V_{\mathrm{GB}} - Vt_{\mathrm{isf}}}{n} \tag{8}$$

where V_{GB} is the gate voltage and Vt_{isf} the ISFET threshold voltage. The drain current I_D is related to the inversion levels by:

$$I_{\mathrm{D}} = I_{\mathrm{S}}(i_{\mathrm{f}} - i_{\mathrm{r}}) \tag{9}$$

with I_S being the normalization current, associated with the sheet normalization current I_{SH} by:

$$I_{\mathrm{S}} = \mu_n C'_{ox}\, n \frac{\phi_t^2}{2}\frac{W}{L} = I_{\mathrm{SH}}\frac{W}{L} \tag{10}$$

where u_n is the charge mobility, C'_{ox} oxide capacitance per unit area, W the transistor width and L the transistor length.

Due the capacitive divider composed of the passivation layer and the gate capacitance, the V_{GB} voltage is attenuated with respect to the potential applied in the reference electrode (V_{ref}) [4] according to

$$V_{GB} = V_{ref}\frac{C_{pass}}{C_{pass} + (C_{ox}C_b)/(C_{ox} + C_b)} \tag{11}$$

where C_b is the depletion capacitance, defined in [11], and C_{pass} is the passivation capacitance corresponding to the series association of the capacitance of the Si_3N_4 layer (C_{SiN}) and the Undoped Silicate Glass (C_{USG}), for the case of the technology used in this project.

The ISFET's threshold voltage (Vt_{isf}) is given [12] by

$$Vt_{isf} = Vt_{mos} + \left(E_{ref} + \chi_{sol} + \phi_{lj} - \frac{\phi_m}{q} - \phi_{eo}\right) \tag{12}$$

with Vt_{mos} is the transistor threshold voltage, E_{ref} the absolute

electrode potential, X_{sol} the potential due to dipoles in the insulator interface, $Ø_{lj}$ the liquid junction potential between electrode and solution, and $Ø_m$ the silicon work function.

The ISFET sensitivity to pH depends on the membrane material used. The sensitivity can be described as $2.3Ø_t\alpha$ with α between 0 and 1, resulting in a maximum theoretical sensitivity of 59 mV/pH at 25 °C [13]. Practical results are below this as shown in Table II.

III. Chip Design

The chip, which was designed in Virtuoso®, consists of a P- and N-type arrays of ISFETs and PMOS and NMOS transistors. The benefits of using high aspect ratios between the top metal area (A_{pass}) and gate area (A_{mos}) have been already discussed in [14]. For this project, thick oxide transistors with $W/L=9\mu m/1.8\mu m$ and the highest A_{pass}/A_{mos} allowed by the DRC were employed. The top metal area is 80 µm x 80 µm resulting in A_{pass}=395A_{mos}. A hole in the top metal layer with minimum dimensions (3µm x 3 µm), was opened above the transistor gate in order to remove trapped charges from the oxide using ultraviolet radiation [15].

The chip, which is currently under fabrication, has a total area of 2.28 mm x 2.28 mm with a sensing area of 871 µm x 420 µm. The accessible ISFETs are highlighted in Fig. 2.

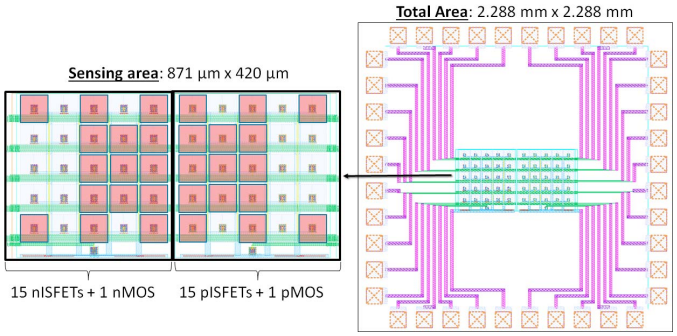

Fig. 2. Chip Layout.

IV. Simulation Results

A Matlab® based algorithm was developed for the model and the project parameters. A nISFET, an Ag/AgCl reference electrode, a 1:1 electrolyte, 0.1 mol/L concentration and a Si_3N_4/USG passivation layer were adopted. The parameters of the solution, electrode, and transistor are shown in Table I [5], [6], [9], [10].

TABLE I
PARAMETERS USED IN SIMULATION

Param.	Value	Unity	Param.	Value	Unity
C	0.1	mol/L	ε_r	78.49	-
K_+	15.8	mol/L	C_{USG}	264	fF
K_-	$63.1*10^{-9}$	mol/L	C_{SiN}	849	fF
K_n	$1*10^{-10}$	mol/L	W	9	µm
$Nsil$	$3*10^{18}$	m^{-2}	L	1.8	µm
$Nnit$	$2*10^{18}$	m^{-2}	Vt_{mos}	0.747	V
E_{ref}	4.63	V	Is	306	nA
X_{sol}	3	mV	n	1.61	-
$Ø_m/q$	4.7	V	t_{ox}	12.5	nm
$Ø_{lj}$	1	mV	T	25	°C
x_2	0.5	nm			

Fig. 3 shows the behavior of $Ø_{eo}$ and Vt_{isf} in terms of the solution pH, as described in (12).

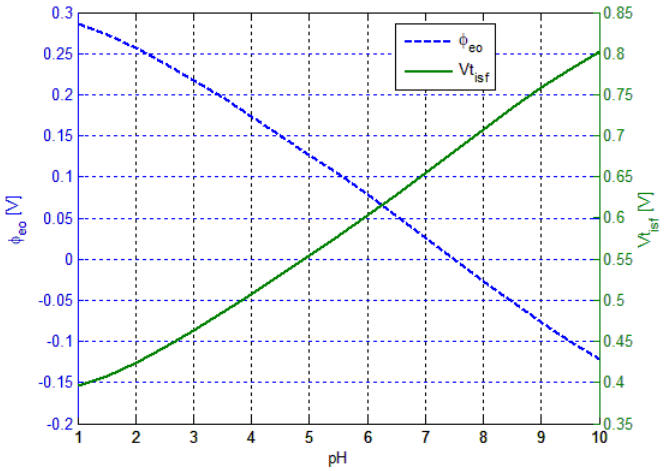

Fig. 3. $Ø_{eo}$ and Vt_{isf} variation with solution pH.

Fig. 4 represents the ISFET I_D x V_{ref} response to different pH values, for V_{DS} = 1 V. The I_D x V_{DS} curves for different pH with V_{ref} = 1V are shown in Fig. 5.

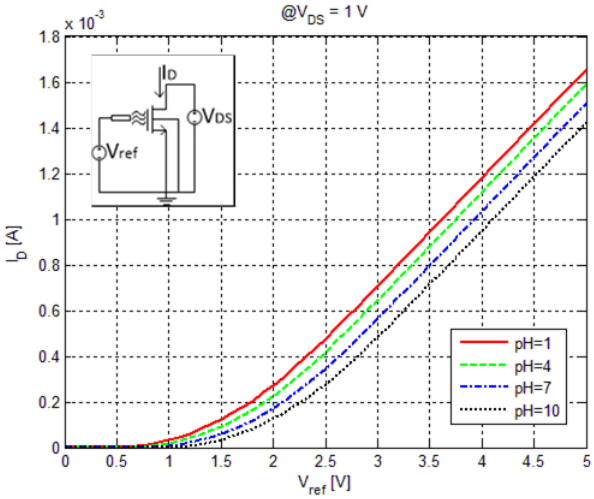

Fig. 4. ISFET I_D x V_{ref} response according to solution pH.

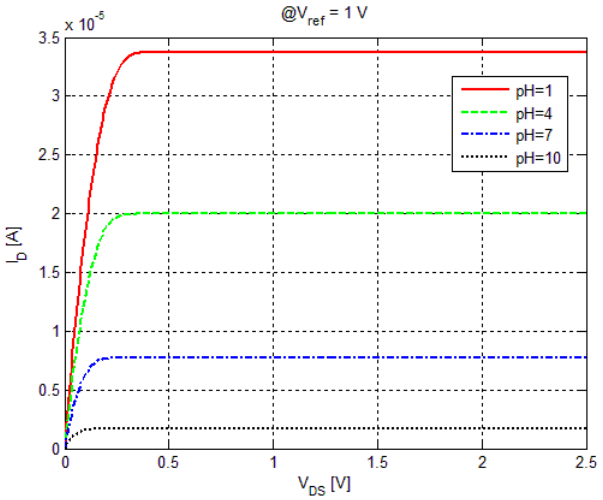

Fig. 5. ISFET I_D x V_{DS} behavior with pH and V_{ref}= 1V.

The results of Fig. 4 and Fig. 5 show the potentials and currents behavior in the ISFET's terminals, as described in (7). The GCS capacitances per unit area are in Fig. 6.

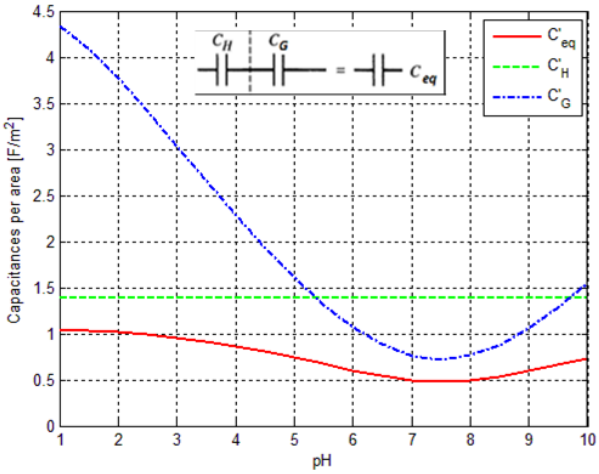

Fig. 6. Gouy-Chapman-Stern capacitances per unit area.

From Fig. 3 it is possible to obtain the Vt_{isf} sensitivity to pH (dVt_{isf}/dpH). In Fig. 7 this result is compared with the theoretical sensitivity given in [13].

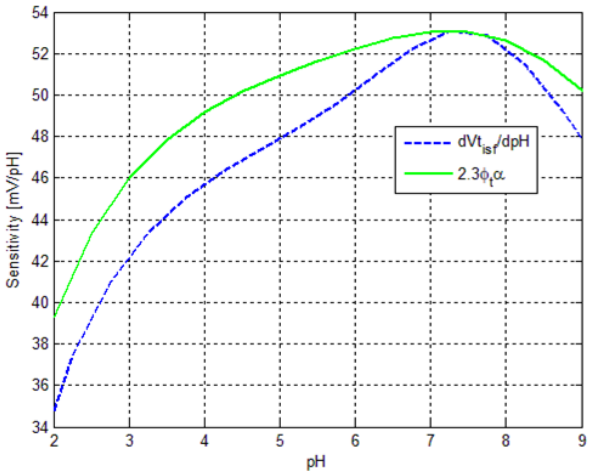

Fig. 7. *Vt* sensitivity to pH.

The simulated values result in an average sensitivity of 45.3 mV/pH (α = 0.77) in the pH range 1-10. Besides that, the theoretical and simulated curves are similar. This result is comparable with the practical ones shown in Table II for standard CMOS technology.

TABLE II
ISFETs SENSITIVITY IN STANDARD CMOS TECHNOLOGY

Reference	Sensitivity (mV/pH)	Technology
[16]	20	AMS 0.35 µm
[17]	39.6	AMS 0.35 µm
[18]	40	AMS 0.35 µm
[3]	42.1	AMS 0.35 µm
[7]	43	AMS 0.6 µm
[15]	46	AMS 0.35 µm
[2]	47	Atmel-ES2 1 µm

V. CONCLUSION

This paper presented the ISFET theory, model and a chip design for characterization. The devices were simulated using a macro model implemented on Matlab®, giving a simulated sensitivity in accordance with practical results from different publications. The characterization will enable the future inclusion of these devices in a complete system for biochemical analysis using the SilTerra D18V technology.

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