Development of a Compact Model for Tunnel FETs Designed for Circuit Simulation

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Abstract—This paper demonstrates for the first time a compact model for Tunnel FETs (TFETs), developed for IC simulations. The model is based on Kane's Model for band-to-band-tunneling. The proposed model is applied to the transfer and the g_m/I_D characteristics of various TFET structures, both experimental and TCAD-simulated. We find a good agreement between the devices and our model. The agreement is improved for those TFETs which have an enhanced electrostatic gate control.

Keywords—tunnel FETs; ultra-low power applications; circuit simulations

I. INTRODUCTION

The band-to-band-tunneling FET (BTB-TFET or TFET) is a recent concept for a logical switching device. Nirschl *et al.* presented TFET simulations in 2004 [1], pointing out its insensibility to short channel effects compared to MOSFETs and showing that a TFET inverter is able to switch faster than a MOSFET inverter. In the same year, Appenzeller *et al.* were the first to experimentally demonstrate that a TFET can exhibit a sub-threshold swing smaller than 60 mV/dec by studying a carbon nanotube (CNT) TFET [2]. An experimental TFET inverter has been presented by Knoll *et al.* [3]. The working principle of a TFET is based on quantum-mechanical tunneling. The current is given by carriers which tunnel from source to the channel. The tunneling rate is determined by the size of the tunneling barrier at the source-channel junction. As in the MOSFET, this energy barrier is controlled by a gate voltage. However, there are different challenges that have to be dealt with when designing a TFET. The tunneling current has to be maximized by optimizing the tunnel junction properties. As in the MOSFET, the gate control must be increased, as it directly impacts the tunnel probability. Also important is suppression of the ambipolar behavior, since in contrast to the MOSFET, the TFET is a bipolar device that is switched on for negative and positive gate voltages.

Since the design challenges for the TFET are complex and the technology is new, there is no standard structure for the device yet. To assess the qualities of a device it is important to design test circuits; and one of the first steps in this direction is to achieve a compact model of the device. Our goal in this paper is to develop a simple empirical model for the TFET that covers both the sub- and the superthreshold regimes for circuit simulation.

II. MODEL DEVELOPMENT

The transconductance-to-current ratio,

$$\frac{g_m}{I_D} = \frac{1}{I_D} \cdot \frac{dI_D}{dV_G} = \frac{d\ln I_D}{dV_G}, \tag{1}$$

is a very important parameter in circuit design. It is "*a measure of the efficiency of the transistor to translate current (power) into transconductance (speed)*" [6]. The g_m/I_D value is reciprocal to the subthreshold swing S (inverse of the subthreshold slope), $\frac{g_m}{I_D} = \ln 10 \cdot \frac{d\log I_D}{d\,V_G} = \ln 10 \cdot \frac{1}{S}$. Hence, in the subthreshold region, where the ideal MOSFET has a linear relation between $\log I_D$ and V_G with the minimum subthreshold swing of $S = 60$ mV/dec, g_m/I_D has its maximum value of 38 V^{-1}. In opposition to MOSFETs, for which many compact models are available [6], there are no compact analytical models for the TFET so far. Vandenberghe *et al.* presented an elaborated analytical model that includes all relevant physical aspects [7]. However, this model has been developed specifically for the technology of the studied device and cannot be considered as compact. De Michielis *et al.* proposed a model which is good for numerical device simulation, but it is not appropriate for IC simulation [8].

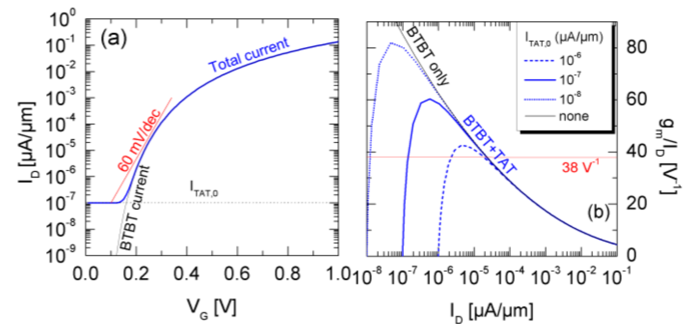

Figure 1 (a): Calculated transfer characteristic after the idealized Kane's Model. The BTBT current (solid black curve) becomes zero at $V_G \rightarrow 0$. If one adds TAT current (dotted black line), the overall current (solid blue curve) is equal to the TAT current at zero voltage. (b): g_m/I_D *vs.* I_D calculated from the transfer characteristics of Fig. 1(a). If only the BTBT current is considered, the value of g_m/I_D becomes infinite for zero.

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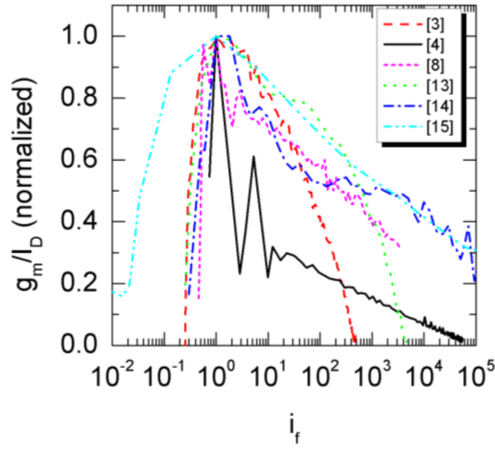

Figure 2: The g_m/I_D *vs.* i_f characteristics of various TFETs with different architectures. g_m/I_D and I_D have been normalized for comparison of the curves to each other.

Wan *et al.* showed a simplified model that is mainly valid for the on-state at higher V_G, and not for the off-state and the subthreshold region [9]. The aforementioned models are based on Kane's model for tunneling [10], which also is the initial point to our approach of developing a compact model:

$$G(x,y)=A_{Kane}F^2(x,y)\ exp\left(-\frac{B_{Kane}}{F(x,y)}\right), \tag{2}$$

where $G(x,y)$ is the tunneling rate (charge carriers generated per time and space at the location (x,y)), $F(x,y)$ is the local electric field, and A_{Kane} and B_{Kane} are material parameters. The tunneling current is calculated as the integral over the tunneling junction.

$$I_{BTBT}=q\iint G(x,y)dxdy. \tag{3}$$

We replace the electric field $F(x,y)$ by an effective constant electric field $F_{eff}=F_{eff}(V_G)$ which is independent of the space coordinate (x,y). The relation between F_{eff} and $F(x,y)$ is determined by the device structure. The electric field is directly related to the surface potential $F_{eff}\sim\Phi_0$. The relation between Φ_0 and V_G is for constant V_D:

$$\delta\Phi_0=q\frac{C_{ox}}{C_{ox}+C_{inv}+C_D}\delta V_G, \tag{4}$$

with $C_{ox,inv,D}$ being the capacitances of the oxide, the inversion layer and the drain, respectively [11]. To break the sub-60 mV/dec-limit and to achieve high on-currents, TFETs require an excellent electrostatic gate control so that $C_{ox}>>C_{inv}$, C_D. In this case, it follows from Eq. (4) that V_G and Φ_0 are directly proportional, so it follows that $V_G\sim F_{eff}$. We rewrite Eq. (3) as

$$I_{BTBT}=A_0V_G^2\ exp\left(-\frac{B_0}{V_G}\right), \tag{5}$$

where A_0 and B_0 are modified Kane's parameters, which depend on both the material parameters and the device geometry. The resulting I_D-V_G relation is shown as the black curve in Fig. 1(a). To test the suitability of Eq. (5) for circuit simulation we calculate g_m/I_D via Eq. (1):

$$\frac{g_m}{I_D}=\frac{d}{dV_G}ln\left(A_0V_G^2\ exp\left(-\frac{B_0}{V_G}\right)\right)=\frac{2}{V_G}+\frac{B_0}{V_G^2} \tag{6}$$

For voltages $V_G\rightarrow 0$ follows that $g_m/I_D\rightarrow\infty$ and the subthreshold swing $S\rightarrow 0$. An infinite g_m/I_D value would mean an infinite efficiency of the transistor for zero current, which does not have a physical meaning. So far, we have assumed that I_D is solely characterized by the band-to-band-tunneling current. In fact, for small V_G that can no longer be held true, and the off-state is dominated by different physical mechanism, such as trap-assisted tunneling (TAT), and ambipolar "leakage". For further development of the model, we focus on TAT as limitation factor only. For trap-assisted tunneling the generation rate is given by

$$G_{TAT}=\left(1+\Gamma(F)\right)\cdot G_{SRH}, \tag{7}$$

where $\Gamma(F)$ is the rate of carriers generated by a trap, and G_{SRH} is Shockley-Read-Hall generation rate [12]. In case of mid-gap traps the SRH rate only depends on carrier concentrations and lifetimes. In non-ideal devices, vacancies and dislocations also contribute to I_{TAT}, which can lead to a severe performance decrease. Eq. (7) can be integrated over the tunnel junction in the same fashion as the BTBT generation rate in Eq. (2), so that both generation rates and the total drain current is the sum of BTBT and TAT currents:

$$I_D=I_{BTBT}+I_{TAT}. \tag{8}$$

G_{SRH} is a field-independent constant. At this point, we make two assumptions: *Firstly*, the electric field for small V_G is very small ($F<<10^5$ V/cm), and so we can assume that $\Gamma(F)\approx 0$ [13]. Hence it follows that $G_{TAT}=G_{SRH}$, which is a field-independent constant. With the generation rate G_{TAT}

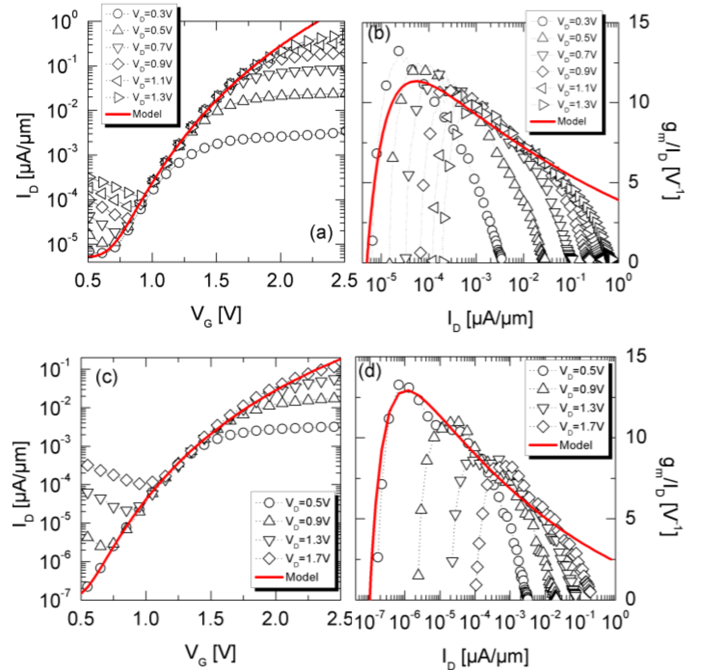

Figure 3. I_D *vs.* V_G (a,c) and g_m/I_D *vs.* I_D (b,d) curve for a homostructure SiGe TFET [4] and a heterostructure Si/SiGe TFET [14], respectively. The red curve represents the model according to Eq. (9) and Eq. (10), respectively. The fit agrees with the data for a certain V_G region, which varies for V_D.

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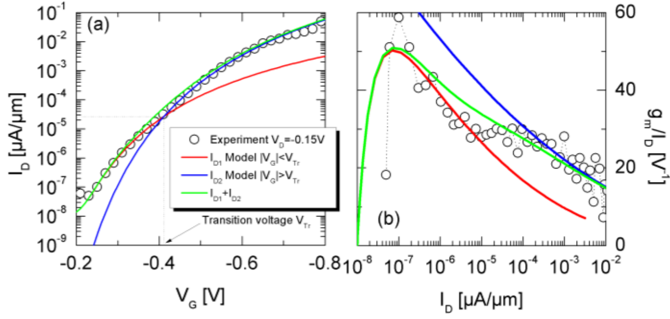

Figure 4. I_D *vs.* V_G (a) and g_m/I_D *vs.* I_D (b) curve for a Si TFET by Morita *et al.* [15]. The transfer curve can be fitted with two sets of parameters, for two V_G regimes: the first set is for the regime $V_G < V_{tr}$, the second for $V_G > V_{tr}$.

being a constant, the current I_{TAT} is also a constant. *Secondly*, for larger V_G, when $\Gamma(F) > 0$, the TAT generation rate cannot be considered constant on the one hand, but on the other hand the drain current is dominated by band-to-band tunneling $I_{BTBT} >> I_{TAT}$ [13]. For the use in our model, we set that $I_{TAT} = I_0$ constant for all V_G. We write down the I_D-V_G relation including both band-to-band and trap assisted tunneling:

$$I_D = A_0 V_G^2 \exp\left(-\frac{B_0}{V_G}\right) + I_0. \quad (9)$$

The resulting curve is displayed in blue in Fig. 1(a), for the arbitrarily chosen parameters $A_0 = 1$ AV^{-2}m^{-1}, $B_0 = 2$ V and $I_0 = 10^{-7}$ µA/µm. We extract from Eq. (9) the g_m/I_D characteristics as a function of V_G, according to Eq. (1)

$$\frac{g_m}{I_D} = \frac{A_0(2V_G + B_0)\exp\left(-\frac{B_0}{V_G}\right)}{A_0 V_G^2 \exp\left(-\frac{B_0}{V_G}\right) + I_0}. \quad (10)$$

The resulting curve is displayed in Fig 1(b). We observe two significant differences compared to the g_m/I_D characteristics in Eq. (6) without considering TAT: the first one is that $V_G \rightarrow 0$ the equation yields $g_m/I_D \rightarrow 0$. The second one is that the g_m/I_D curve has a finite peak maximum. These properties make the TFET g_m/I_D characteristics genuinely distinguishable from the g_m/I_D characteristics of a conventional MOSFET. Since, in principle, there is no lower limit for the subthreshold swing in a TFET, the only limiting factor in our model is the off-current characterized by I_0.

III. Model Application

Fig. 2 shows the g_m/I_D characteristics for TFETs from various technologies. For comparison, g_m/I_D has been normalized by the maximum value, and I_D was normalized accordingly, $i_f = I_D/I_{max}$. The curves exhibit the characteristic features which are addressed by our model. One exception though can be observed by the g_m/I_D curve of the TFET by Knoll *et al.*, who manged to suppress TAT by obtaining the transfer characteristics by a pulsed measurement [5], and the resulting g_m/I_D curve has no

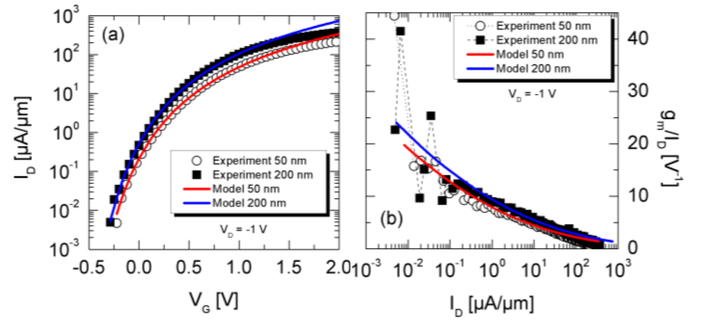

Figure 5. I_D *vs.* V_G (a) and g_m/I_D *vs.* I_D (b) curve for a Si NW TFET by Knoll *et al.* [5], for two different gate lengths $L_g = 50$ and 200 nm, respectively. The g_m/I_D curve has no defined peak due to the suppression of TAT by pulsed measurement.

clearly defined peak (see Fig. 2 and 5(b)). In order to test the agreement of our model with the experiments, we fit TFET data from various groups to our model. The fitting parameters are the modified Kane's parameters A_0, B_0 and the off-current I_0. Furthermore, we introduced the offset voltage V_0, which is an empirical parameter, and substituted in Eq. (9) and (10) V_G by V_G-V_0. Fig. 3 shows the experimental data of a homo-structure $Si_{0.5}Ge_{0.5}$ (Fig. 3(a) and (b), [4]) and a heterostructure $Si/Si_{0.5}Ge_{0.5}$ (fig 3(c) and (d), [14]) TFET for different V_D. These data were fitted with our model. We observe an agreement of model and experiment for a small V_G interval. The extent and position of the interval depends on V_D. Deviations from the model can be attributed to the lack of superior electrostatic gate control, which was a necessary requirement for the development of the model, even though these devices feature a high-*k*/metal gate. For non-ideal gate-control the linear relation between V_G, Φ_0 and F_{eff} is confined to a rather small V_G range. For large V_G, the experimental I_D is notably smaller than the calculated I_D from the fit. We attribute this to an increased source/drain-resistance, which leads to decreased on-currents. Fig. 4 shows the transfer and g_m/I_D characteristics of a Si TFET presented by Morita *et al.* [15]. To obtain an optimal fit, we must distinguish two V_G regimes, $V_G < V_{tr}$ and $V_G > V_{tr}$, where V_{tr} is an empirically determined "transition voltage". For each region we find different fit parameters. Fig. 4(a) shows I_D-V_G-fits for each region separately, which excellently agree with the experimental data. It also shows both fitted currents summed up. The current sum also agrees with the data well, except for the transition region.

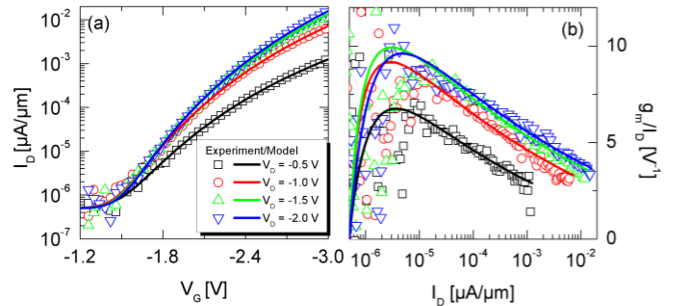

Figure 6. I_D *vs.* V_G (a) and g_m/I_D *vs.* I_D (b) curve of a planar Si TFET by Wan et al [9]. Note that the fits are dependent on V_D.

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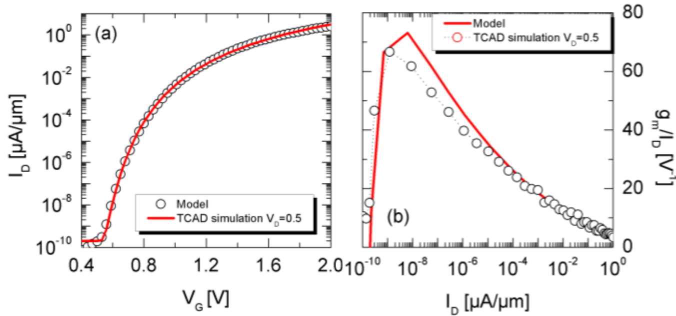

Figure 7. I_D *vs.* V_G (a) and g_m/I_D *vs.* I_D (b) curve for a TCAD-simulated SiGe TFET [22], which has the same architecture as the experimental device in ref. [5].

Fig 4(b) shows the g_m/I_D data with the respective fits for each region, and the g_m/I_D values for the current sum. The latter gives a good agreement with the experiment. Furthermore it should be noticed that the g_m/I_D characteristics achieves values that are significantly larger than the MOSFET limit of 38 V^{-1}. Fig. 5 displays the transfer (a) and the g_m/I_D (b) characteristics of a Si nanowire TFET by Knoll *et al.* [5] for two different gate lengths of 50 and 200 nm. The respective fit for each data set shows a good agreement in the transfer characteristics (fig 5(b)), except for very high V_G. There is also a good agreement between data and model fit for the Si TFET by Wan *et al.* [9], shown in Fig. 6. Note that for this device the fits are different for each V_D, in contrast to the SiGe TFETs shown in Fig. 3. The good agreement of experiment and data fit in Fig. (5) and (6) can be explained by both TFETs having an improved electrostatic gate control. An almost ideal electrostatic control is achieved in TCAD simulations (SYNOPSYS) of a planar $Si_{0.5}Ge_{0.5}$ TFET [16], as can be seen in Fig. 7 (a) and (b). g_m/I_D significantly exceeds 38 V^{-1}. Table 1 summarizes the extracted fitting parameters for the studied devices, including the maximum g_m/I_D values and their respective values of V_G, and I_D. The large variance of the fitting parameters for the different devices indicates their strong dependence on the device architecture.

IV. Conclusion

We developed an empirical model for TFETs which is based on Kane's model for band-to-band tunneling for the on-state. The off-current is dominated by trap-assistant tunneling.

Device	A_0	B_0	V_0	I_0	g_m/I_D, max	$V_G(g_m/I_D$, max)	$V_D(g_m/I_D$, max)	$I_D(g_m/I_D$,max)
	[$Am^{-1}V^{-2}$]	[V]	[V]	[μA/μm]	[V^{-1}]	[V]	[V]	[μA/μm]
[4]	2,62E-01	31,35	-0,8	5E-06	13,23	0,86	0,30	2,33E-05
					11,34	*0,87*		*5,65E-05*
[14]	9,59E-04	28,52	-0,8	1E-07	13,26	0,75	0,50	6,78E-07
					12,93	*0,70*		*1,30E-06*
[15]	3,24E-05	5,77	0,3	2E-10	66,66	0,56	0,50	1,22E-09
					73,16	*0,59*		*6,40E-09*
[5]	3,03E+02	5,45	-0,8	0	44,42	-0,22	-1,00	4,73E-03
					19,80	*-0,22*		*8,10E-03*
[5]	6,20E+02	5,30	-0,8	0	41,49	-0,27	-1,00	6,67E-03
					24,05	*-0,28*		*5,29E-03*
[16]	1,87E-08	2,91	0,0	1E-08	58,78	-0,25	-0,15	1,00E-07
					50,91	*-0,24*		*6,98E-08*
[9]	1,45E-05	27,06	0,0	5E-07	10,95	-1,65	-2,00	3,40E-06
					9,62	*-1,68*		*4,64E-06*

Table 1. Extracted parameters for different TFET with different architectures Also shown is the maximum value for g_m/I_D with its respective values for I_D, V_G and V_D, experimentally (regular) and from the fit (italic).

Our model fits with good agreement various experimental TFES, while an improved electrostatic control provides agreement over a larger V_G region.

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