Design and testing of a CMOS Self-Biased Current Source

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***Abstract*—This paper presents the design and testing of a self-biased current source. The design described in this paper is based on the concept of inversion coefficient, which allows a direct calculation of the dispersion in the output current in terms of the internal bias errors and transistor mismatch. The circuit was fabricated in a standard CMOS 180 nm technology.**

***Index Terms*—Self-biased current source, Self-cascode MOSFET, operational amplifier, inversion coefficient.**

I. Introduction

Current sources are essential biasing circuits [1]. To reduce power consumption in CMOS technologies, various current sources based on sub-threshold operation of the MOSFET have been proposed. Some of them include integrated resistors [2], or transistors operating in linear region [3], [4] to replace the passive components. This paper present a very simple and intuitive design of a modular self-biased current source using the Self-Cascode MOSFET (SCM) [5], [6] including the analysis of the errors associated to moderate inversion operation of transistors and mismatch effects.

The paper is organized as follows. In Section II, the Self-Cascode MOSFET (SCM) is briefly described and approximated design equations are derived. In Section III, the design procedure of the SCM based current reference in terms of the circuit specifications is presented. Section IV shows simulation and experimental results. Finally the conclusions are presented in Section V.

II. Self-Cascode Mosfet

The SCM, commonly used as a Proportional-to-Absolute Temperature (PTAT) low voltage generator, is the core of several self-biased current sources [5]–[8]. In the SCM of Fig. 1, M_1 operates in the triode region and M_2 operates in saturation ($i_{f2} \gg i_{r2}$).

The current flowing through each transistor is

$$I_{D1} = I_{SQ} S_1 (i_{f1} - i_{r1}) = I_D \tag{1}$$

$$I_{D2} \approx I_{SQ} S_2 i_{f2} = I_D \tag{2}$$

where i_f and i_r are the forward and reverse normalized currents or inversion levels [9]–[11], I_{SQ} is the specific current dependent on the technological parameters and S_1 and S_2 are the geometric ratios of the transistors. Since $V_{D1} = V_{S2}$ and $V_{G1} = V_{G2}$, then $i_{r1} = i_{f2}$. Thus, from (1) and (2) it follows that

$$i_{f1} = \left(1 + \frac{S_2}{S_1}\right) i_{f2} = \alpha_1 i_{f2} \tag{3}$$

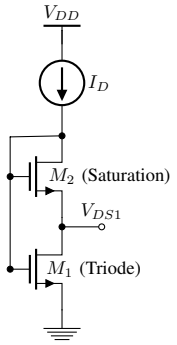


Fig. 1: Self-Cascode MOSFET.

Applying the Unified Current Control Model (UICM) to both transistors [10], [11] results in

$$V_{DS1} = \phi_t \left[F\left(i_{f1}\right) - F\left(i_{f1}/\alpha_1\right) \right] \tag{4}$$

where

$$F\left(i\right) = \sqrt{1+i} - 2 + \ln\left(\sqrt{1+i} - 1\right) \tag{5}$$

In strong inversion (SI), $i_{f1} \gg 1$, Eqs. (4) and (5) can be simplified as

$$\frac{V_{DS1}}{\phi_t} \sim \sqrt{i_{f1}} - \sqrt{i_{f1}/\alpha_1} \tag{6}$$

whereas in moderate inversion (WI, MI), $i_{f1} < 2$, and V_{DS1} can be approximated by

$$\frac{V_{DS1}}{\phi_t} \sim \ln \alpha_1 + \frac{\alpha_1 - 1}{4\alpha_1} i_{f1} \tag{7}$$

Finally, in weak inversion (WI), $i_{f1} \ll 1$, and

$$\frac{V_{DS1}}{\phi_t} = \ln \alpha_1 \tag{8}$$

III. SCM-Based Current Reference

The current source of Fig. 2 [7], [8] consists of two SCM biased by a PMOS current mirror and an operational amplifier that forces the internal nodes of the SCMs to be at the same potential.

If M_1 and M_2 operate in WI, it follows from (4), (5) and (8) that

$$\ln \alpha_1 = F\left(i_{f3}\right) - F\left(i_{f3}/\alpha_3\right), \quad \alpha_3 = 1 + S_4/S_3 \quad (9)$$

Thus, i_{f3} (the inversion level of M_3) is constant and dependent only on the geometrical ratios α_1 and α_3. The output reference current I_{OUT} is

$$I_{OUT} = I_{SQ} S_{e1} i_{f1} = I_{SQ} S_{e3} i_{f3} \quad (10)$$

where S_{e1} and S_{e3} are the geometric ratios of the transistors equivalent to SCM 1-2 and SCM 3-4 given [12] by

$$1/S_{e1(3)} = 1/S_{1(3)} + 1/S_{2(4)} \quad (11)$$

Thus, the output current is proportional to the specific current of the *n*-channel transistors. Consequently, the circuit is useful to bias transistors at constant inversion levels, independent of the temperature and technology.

As shown in Fig. 3, the operational amplifier in Fig. 2 can be replaced by an intermediate branch formed by M_5 and M_6, which imposes the equality of the potentials V_X and V_Y [11].

In effect, if M_6 is equal to M_2, its source voltage equals V_X. On the other hand, if M_3 equals M_5, its drain voltage equals V_Y. Thus, the series connection of M_5 and M_6 forces $V_X = V_Y$.

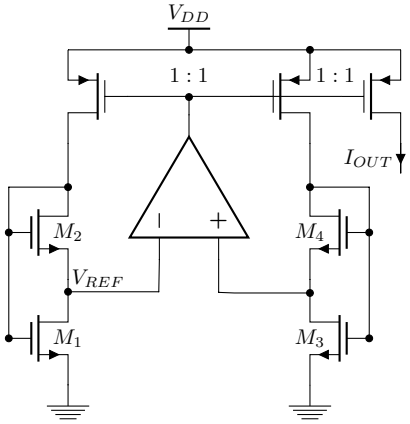


Fig. 2: Modular Self-Biased Current Source (start-up circuit not shown).

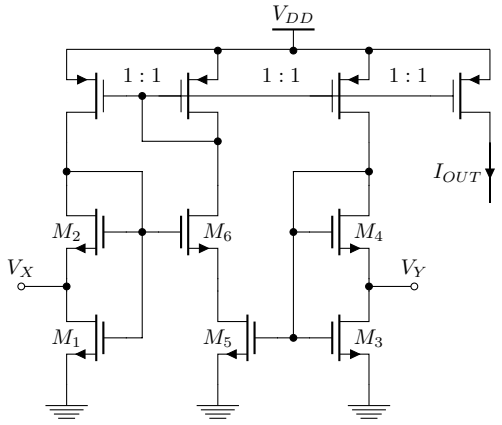


Fig. 3: Self-Biased Current Source (start-up circuit not shown) [5].

A. Error Analysis

To analyze the error in the reference voltage provided by the SCM operating in WI, we assume that (10) is valid, thus, we neglect the nonidealities in the *p*-channel current mirrors.

Consequently, the relative error in the output current is the same as the relative errors in the inversion coefficients i_{f1} and i_{f3}. From (7) we obtain the error in V_{REF} as a function of the inversion level i_{f1}.

$$\frac{\Delta V_{REF}}{\phi_t} = \frac{\alpha_1 - 1}{4\alpha_1}\Delta i_{f1} = \frac{\alpha_1 - 1}{4\alpha_1}\frac{\Delta I_D}{I_D} i_{f1} \quad (12)$$

Obviously, for deep weak inversion operation, this error is negligible.

The current source of Fig. 2 is susceptible to the offset voltage of the operational amplifier and that of Fig. 3 to the mismatches between the SCM transistors and the transistors of the intermediate branch.

As described in [8], an offset voltage V_{off} leads to an error in the inversion coefficient of M_3 given by

$$\frac{\Delta i_{f3}/i_{f3}}{V_{off}/\phi_t} = \frac{2}{\sqrt{1+i_{f3}} - \sqrt{1+i_{f3}/\alpha_3}}, \; 1 < \alpha_3 < \alpha_1 \quad (13)$$

which, using the approximations of Section II, can be written as

$$\frac{\Delta i_{f3}/i_{f3}}{V_{off}/\phi_t} = \frac{1}{\ln \alpha_1 - \ln \alpha_3}, \; \sqrt{\alpha_1} < \alpha_3 < \alpha_1 \text{@ WI, MI} \quad (14)$$

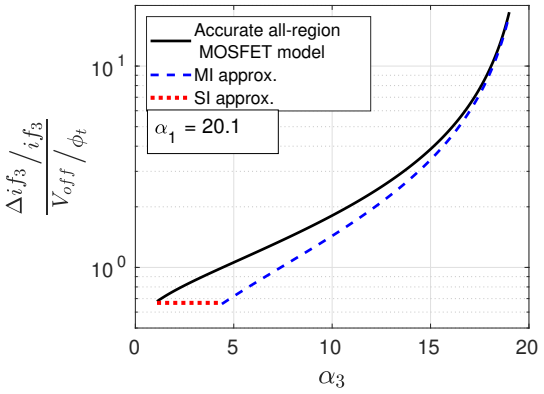
$$\frac{\Delta i_{f3}/i_{f3}}{V_{off}/\phi_t} = \frac{2}{\ln \alpha_1}, \; 1 < \alpha_3 \leqslant \sqrt{\alpha_1} \text{@ SI} \quad (15)$$

The curve of Fig. 4a shows the error in the inversion coefficient per normalized offset voltage as function of the geometric ratio α_3. Fig. 4b shows the inversion level and the overdrive voltages as functions of α_3. Clearly a value of α_3 near 1 minimizes the error of the inversion coefficient but implies operation in strong inversion with a high overdrive voltage incompatible with advanced technologies. Thus, as a rule of thumb one can make the choice of a value of α_3 which gives an error of the order of two or three times the minimum error in SI.

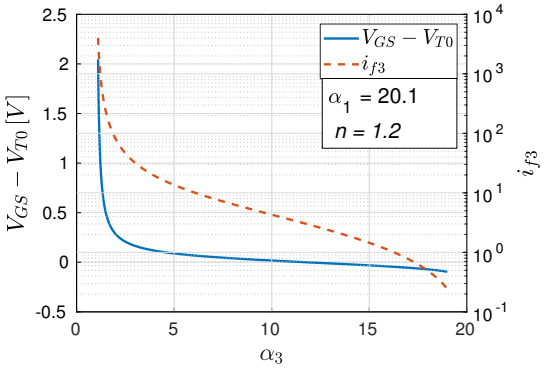
B. Circuit Design

The current source of Fig. 3 has been designed in a standard 180 nm CMOS technology to provide an output reference current I_{OUT} = 10 nA with $\Delta I_{OUT}/I_{OUT}$ = 10%. The PTAT reference voltage is affected by threshold voltage mismatch and, consequently, should be much higher than the voltage mismatch, but due to the logarithmic dependence of the PTAT voltage on α_1, a value of V_{REF} much larger than $3\phi_t$, is not practical [7]–[9]. We selected $V_{REF} = 3\phi_t$, and ΔV_{REF} = 0.5 mV. We can readily calculate α_1 writing i_{f1} in terms of α_1 with the help of (12) and solving $F\left(i_{f1}\right) - F\left(i_{f1}/\alpha_1\right) = 3$. We obtain, $\alpha_1 = 16.9$ and $i_{f1} = 0.808$. Once α_1 is determined, we calculate α_3 from (14). For an offset voltage of 1 mV $\alpha_3 = 11.2$. Finally from (9) we obtain $i_{f3} = 2.45$.

Fig. 5 shows the operating point (intersection point of the two curves of the two SCMs) of the projected current source.



(a) Relative sensitivity of the reference current versus α_3.



(b) Overdrive voltage and the inversion level versus α_3.

Fig. 4: Accuracy analysis of the current source.

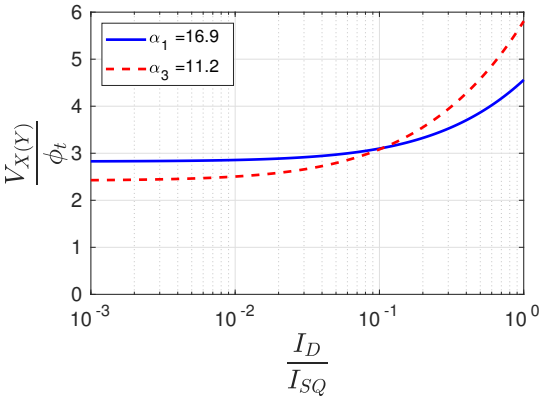


Fig. 5: Internal voltages of the SCMs as functions of the bias current.

For the calculation of the aspect ratio S of each transistor the normalized specific current I_{SQ} of the transistor was extracted. The value of I_{SQ} obtained through the g_m/I_D method was 175 nA [13]. The width W and length L of the transistors were determined through Pelgrom's model of the threshold mismatch [14], since the threshold voltage standard deviation dependent on the area of the devices, as shown in (16), we chose the same design criteria used in the current mirrors with large current gain or attenuation, to keep the same area for transistors with different geometric ratios [12]. The area A of the transistors was determined using (16) with the parameters shown in Table I. The width and length of the devices in terms of the geometric ratios and areas are simply given by (17). In Table I, the aspect ratios and the inversion coefficients of the transistors used in the SCMs are summarized. The transistors were implemented through series-parallel associations of unitary transistors [12].

$$\sigma(\Delta V_{T0}) = \frac{A_{VT}\zeta}{\sqrt{A}} \tag{16}$$

$$W = \sqrt{AS}, \quad L = \sqrt{\frac{A}{S}} \tag{17}$$

TABLE I: Parameters of the SBCS @ A_{VT} = 3.0 mV μm, $\sigma(\Delta V_{T0}) = 1$ mV, $\zeta = 4$.

Area [μm^2]	Transistor	S	α	i_f	i_r	W [μm]	L [μm]	I_{SQ} [nA]
147.280	M_1	0.0796	16.9	0.8079	0.04685	1× 3.425 (3.425)	9×4.780 (43.02)	165
147.280	$M_{2,6}$	1.263		0.04685	0	1×13.645 (13.645)	2×5.400 (10.80)	169
147.280	$M_{3,5}$	0.02769	11.2	2.452	0.2088	1×2.020 (2.020)	2×9×4.050 (72.930)	161
168.726	M_4	0.2834		0.2088	0	1×6.915 (6.915)	4×6.100 (24.4)	169

IV. Simulation and Experimental Results

Fig. 6 shows the approximate PTAT dependence of the current reference for different process corners.

To verify the initialization characteristics of the current source, a square wave of 5 Hz was applied. The results of simulation and experiment are shown in Figs. 7a and 7b, respectively. The stabilization time is high, since this current source does not have a start-up circuit.

An analysis of the impacts on the output reference current I_{OUT} under process variations and matching through Monte Carlo (MC) simulation was made. The results of the MC simulations and the measurements of 33 chip samples are shown in Figs. 8a and 8b, respectively. The simulation presented values of standard deviation and mean of I_{OUT} close to the experimental values, for the small number of available samples.

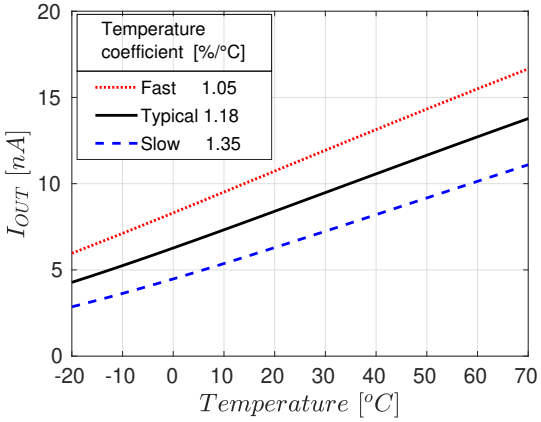
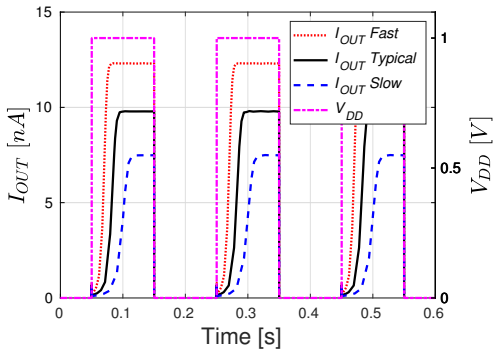
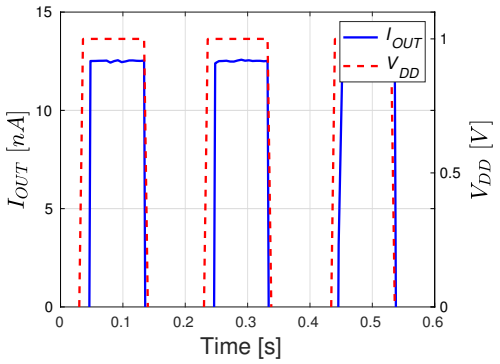


Fig. 6: Current reference at different process corners over temperature.

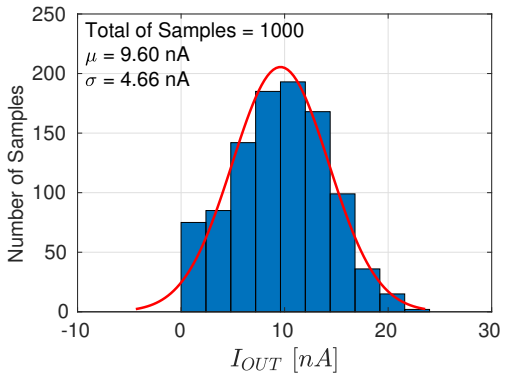


(a) Corner simulation of the output current.

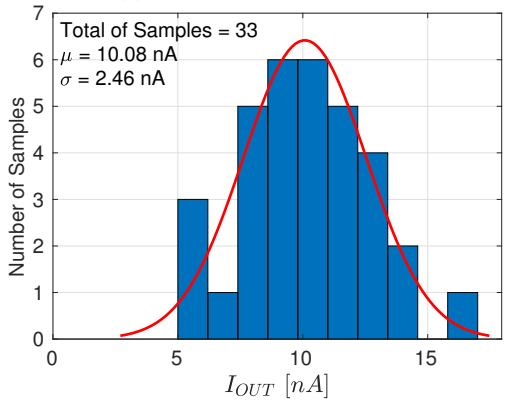


(b) Measured output current.

Fig. 7: Output current for a square wave V_{DD}.



(a) Monte Carlo simulation.



(b) Histogram of measured I_{OUT}.

Fig. 8: Output current dispersion.

V. Conclusions

A modular self-biased current source has been designed using a very simple and intuitive design procedure. The transistors have been seized in order to limit the output current dispersion. The advantage of using the inversion level as key variable is clearly show. Experimental results corroborate the design procedure.

Acknowledgment

The authors would like to thank the MOSIS Program, which provided resources for the fabrication of the test chips. This work was supported by the Brazilian agencies CAPES and CNPq, by means of scholarships.

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