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On the minimum supply voltage for CMOS analog circuits: rectifiers and oscillators

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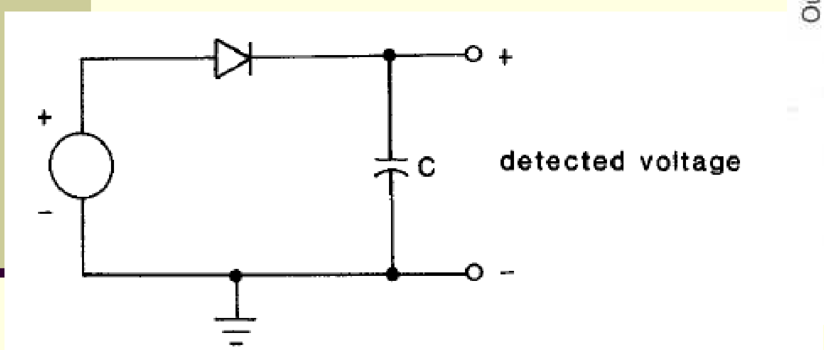
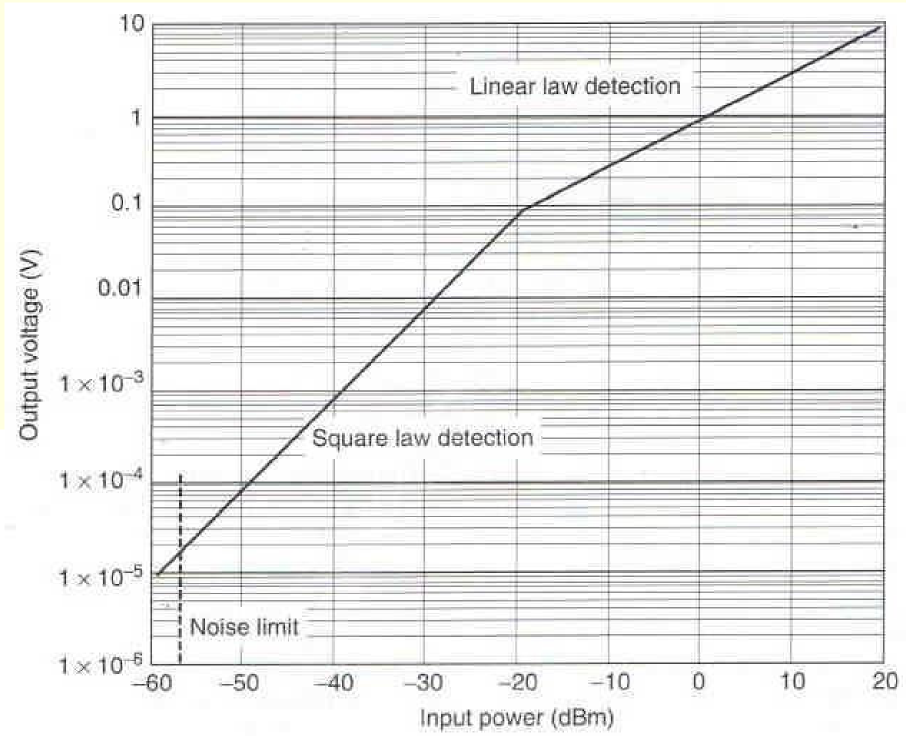
Rectifier outline

- ⇨Background: microwave power detection
- ⇨Power/peak detector
- ⇨Half-wave rectifier
- ⇨MOSFETs as diodes
- ⇨Weak inversion MOSFET model

Background: microwave power detection



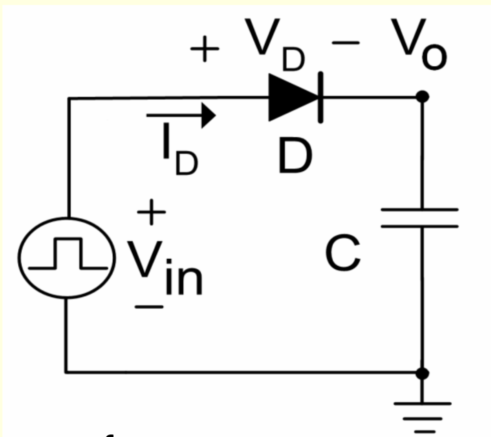
- Basic detector circuit



Wetenkamp, IEEE MTT-S Int. Microwave Symp. Dig., 1983

Power/Peak Detector 1

A simple case: square-wave input



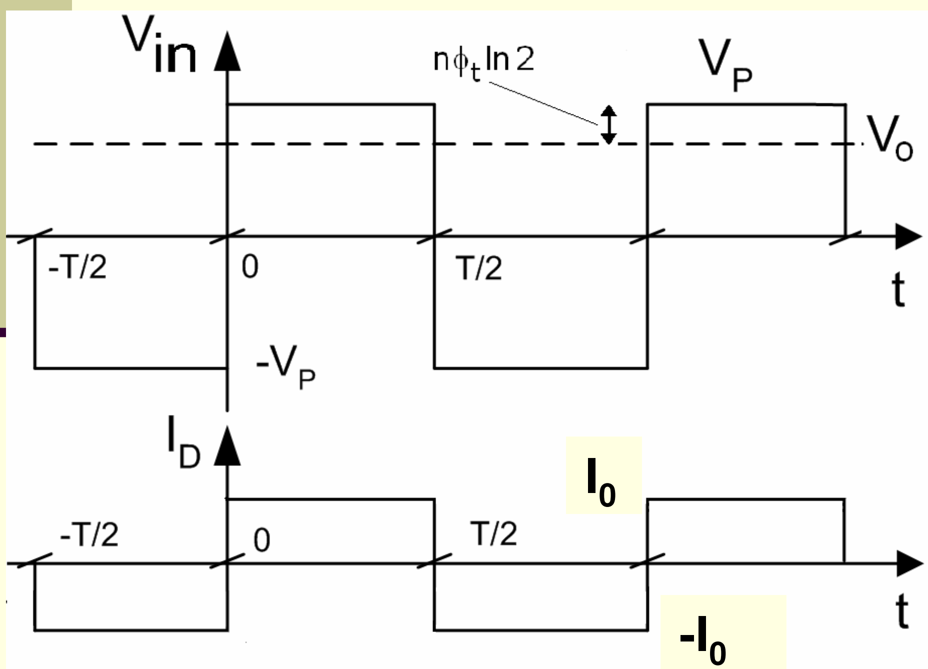
Steady-state analysis

Basic principle: charge conservation

$$\frac{1}{T}\int_{-T/2}^{T/2} I_D dt = 0 \qquad I_D = I_0[e^{\frac{V_D}{n\phi_t}} - 1]$$

$$\frac{I_0}{T}\left[\int_{-T/2}^{0}\left(e^{\left(\frac{-V_P - V_o}{n\phi_t}\right)} - 1\right)dt + \int_{0}^{T/2}\left(e^{\left(\frac{V_P - V_o}{n\phi_t}\right)} - 1\right)dt\right] = 0$$

Waveforms for $V_P >> n\phi_t$

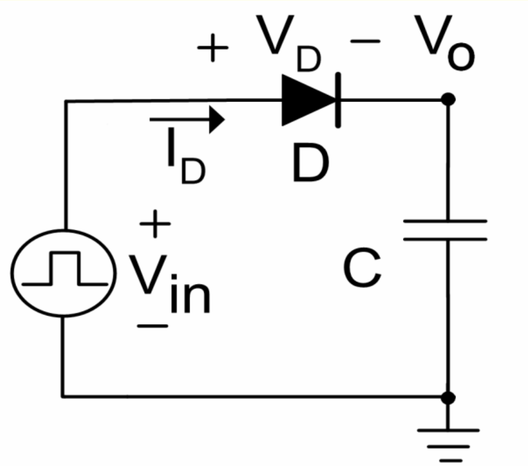


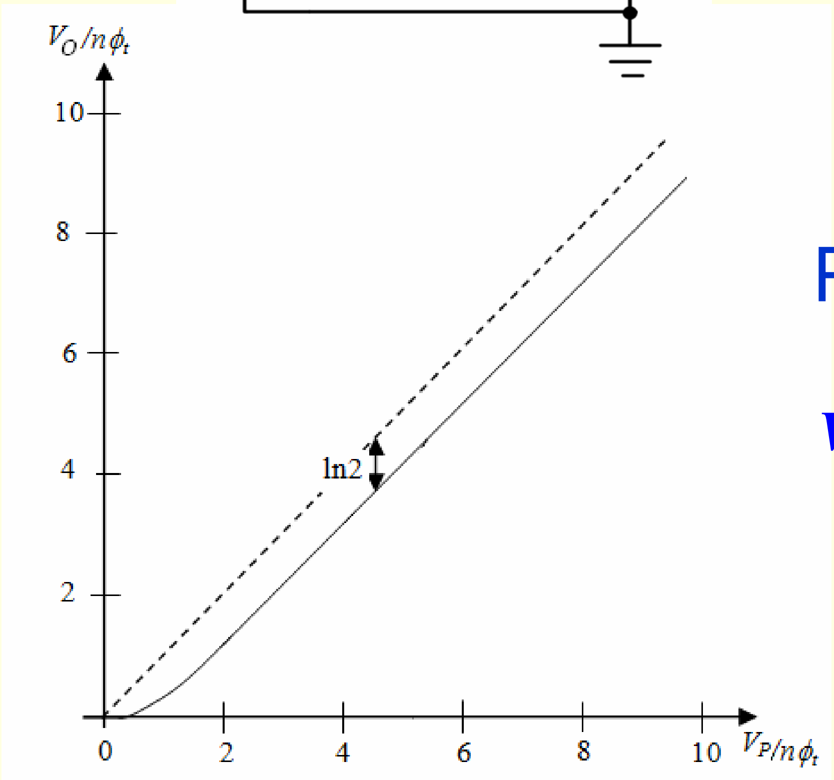
Assumption: very low ripple → $V_o \cong$ constant

$$\frac{V_o}{n\phi_t} = \ln\left[\cosh\left(V_P / n\phi_t\right)\right]$$

Power/Peak Detector 2

A simple case: square-wave input





$$\frac{V_o}{n\phi_t} = \ln\left[\cosh\left(V_P/n\phi_t\right)\right]$$

Power Detector

$$V_P \ll n\phi_t \quad \rightarrow \quad \frac{V_o}{n\phi_t} \cong \frac{1}{2}\left(\frac{V_P}{n\phi_t}\right)^2$$

Peak Detector

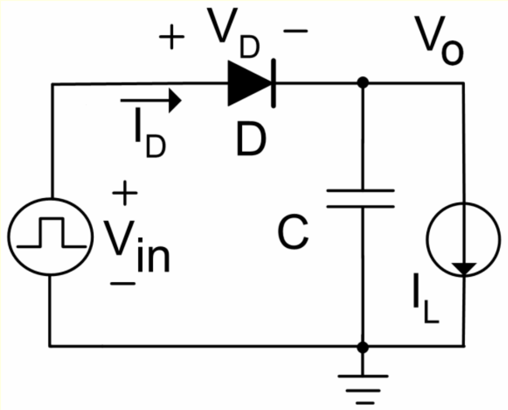
Diode "ON" voltage drop

$$V_P \gg n\phi_t \quad \rightarrow \quad V_O \cong V_P - n\phi_t \ln 2$$

Input

Results for sine input are similar.
Difference is a "form factor"

Half-wave rectifier circuit 1



Steady-state analysis (similar to peak detector)

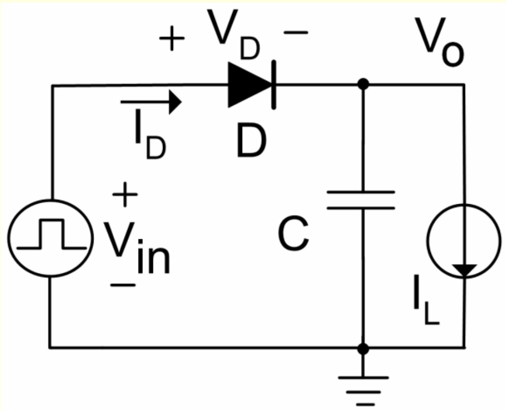
Basic principle: charge conservation

$$\frac{I_0}{T}\left[\int_{-T/2}^{0}\left(e^{\left(\frac{-V_P-V_o}{n\phi_t}\right)}-1\right)dt+\int_{0}^{T/2}\left(e^{\left(\frac{V_P-V_o}{n\phi_t}\right)}-1\right)dt\right]=I_L$$

Assumption: very low ripple → $V_o \cong$ constant

$$\frac{V_o}{n\phi_t}=\ln\left[\frac{\cosh\left(V_P/n\phi_t\right)}{1+I_L/I_0}\right]$$

Half-wave rectifier circuit 2

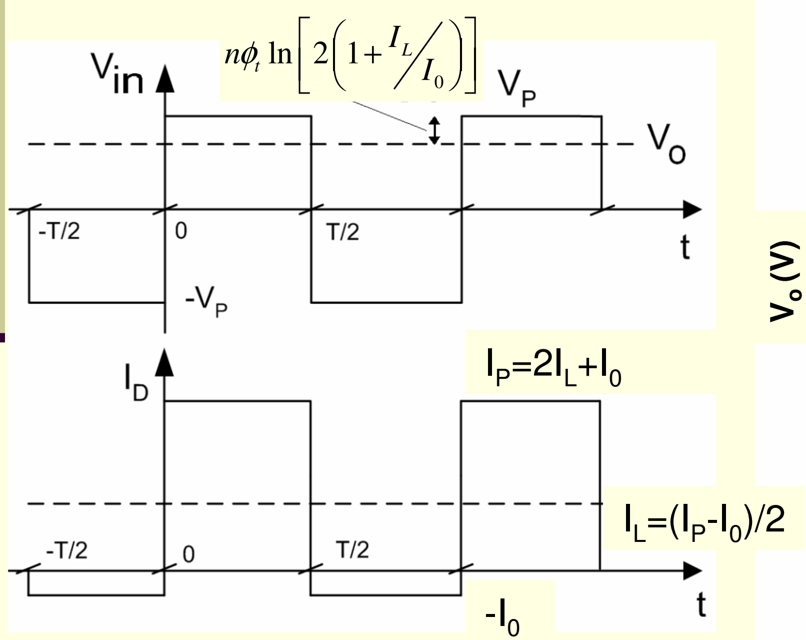


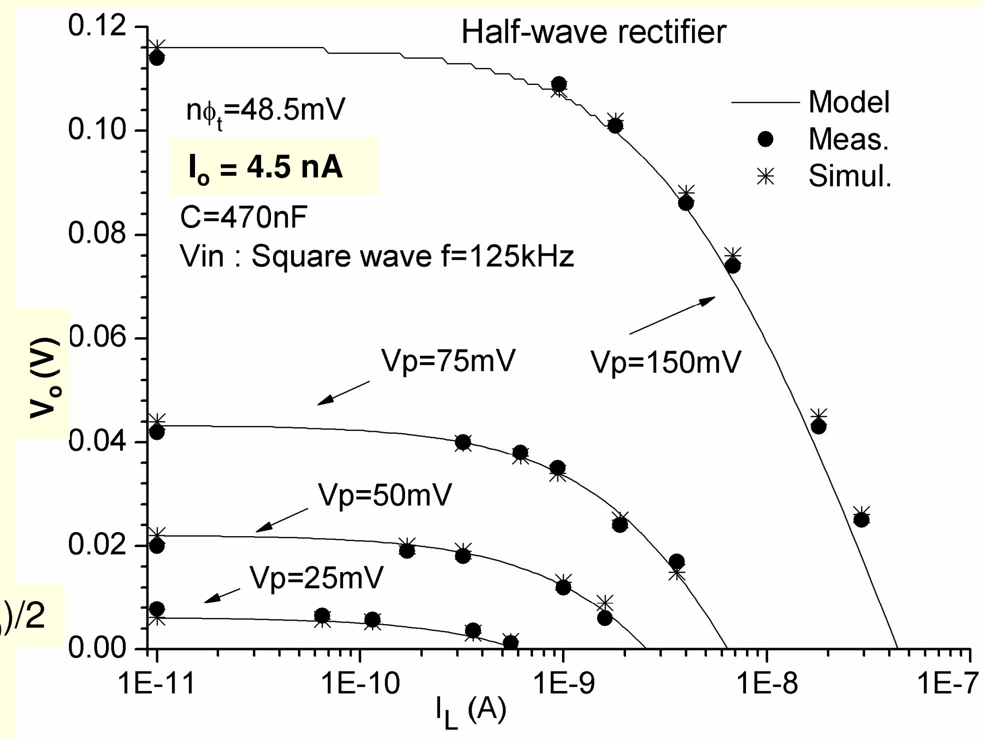
Input

Diode “ON” voltage drop

$$V_P > n\phi_t \quad \rightarrow \quad V_o \cong V_P - n\phi_t \ln\left(\frac{I_P + I_0}{I_0}\right)$$

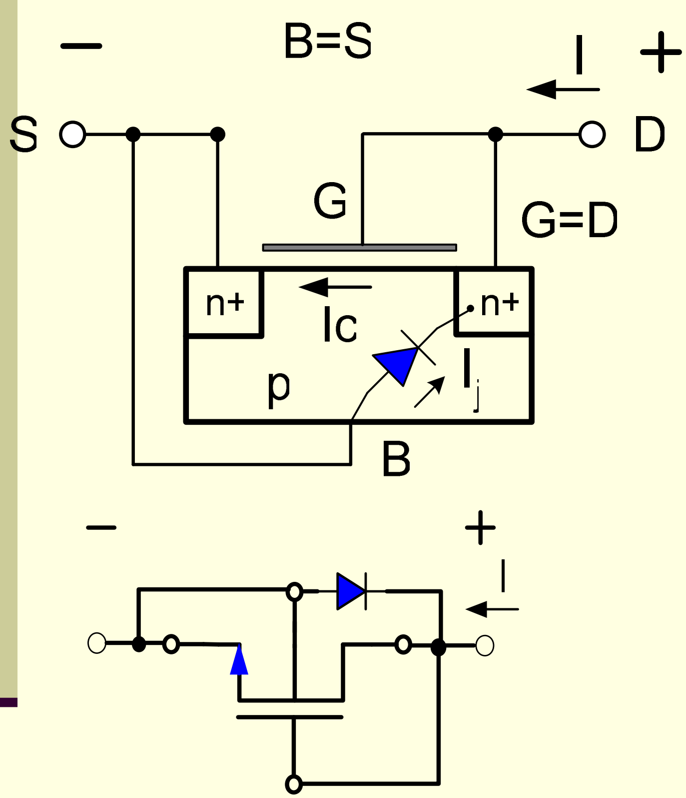
Waveforms for $V_P >> n\phi_t$





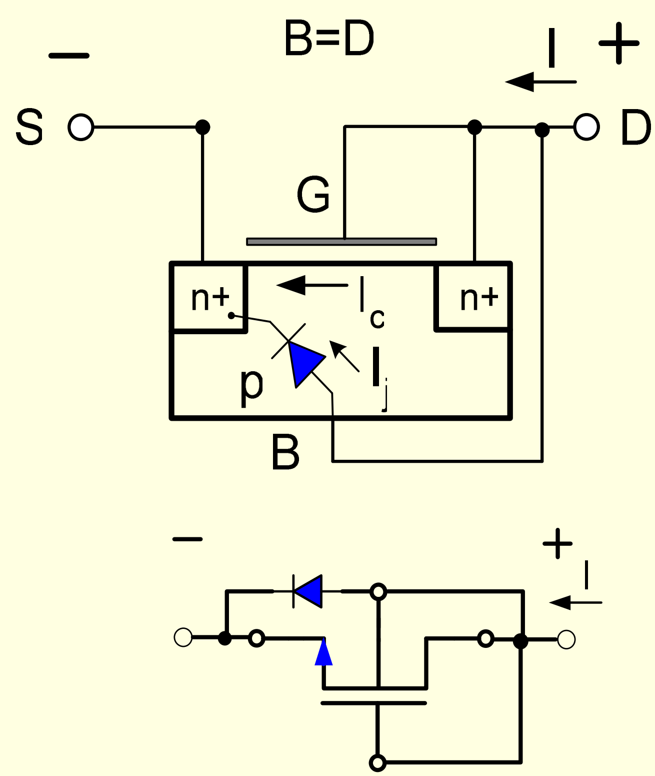
MOSFETs as diodes

Conventional



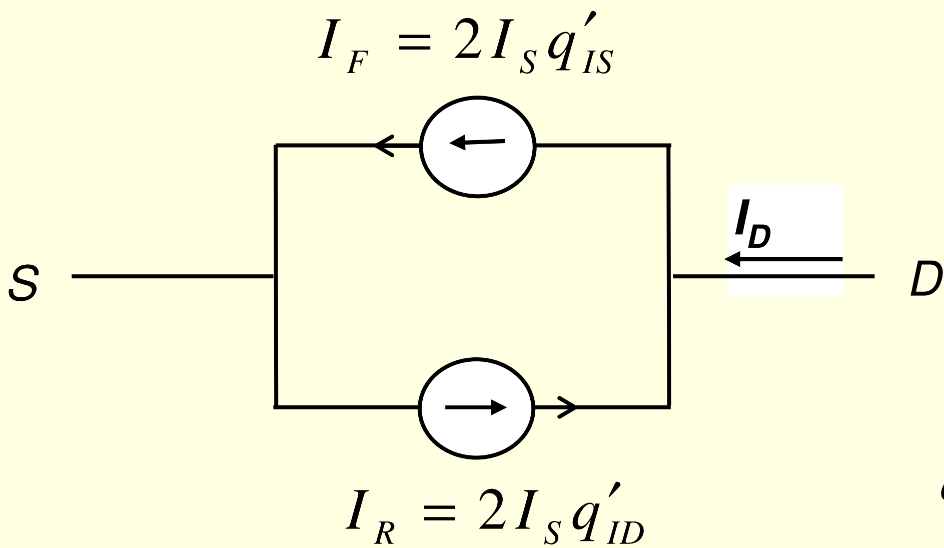
Channel and extrisinc diode are in anti-parallel

DTMOS



Channel and extrisinc diode are in parallel

Weak inversion MOSFET model



$$\phi_t = \frac{kT}{q} (= 26 \text{ mV @ } 300\text{K})$$

$$I_S = \mu C'_{ox} n \frac{\phi_t^2}{2} \frac{W}{L} = I_{SQ} \frac{W}{L}$$

$$q'_{IS(D)} = e^{\frac{V_P - V_{S(D)B}}{\phi_t}} \cong e^{\frac{V_{GB} - V_{T0} - n V_{S(D)B}}{n\phi_t}}$$

W, L width, length of the channel

μ mobility, C'_{ox} gate capacitance per unit area, *n* slope factor (n = 1.2-1.6)

V_P pinchoff voltage , V_{T0} threshold voltage

q'_{IS} *and* q'_{ID} are the normalized carrier densities (to the thermal charge $-nC'_{ox}\phi_t$) at source and drain.

I_S and I_{SQ} are the normalization (specific) and "sheet" normalization currents.

DTMOS diode in WI

- for the DTMOS connection $V_{GB} = V_{DB} = 0$, v = -V_{SB}

$$I_{DS} = I_F - I_R = 2I_S e^{-\frac{V_{T0}}{n\phi_t}} \left(e^{\frac{v}{\phi_t}} - 1 \right)$$

- the DTMOS diode behaves as a diode with ideality factor $n = 1$ for low voltage (weak inversion) operation.

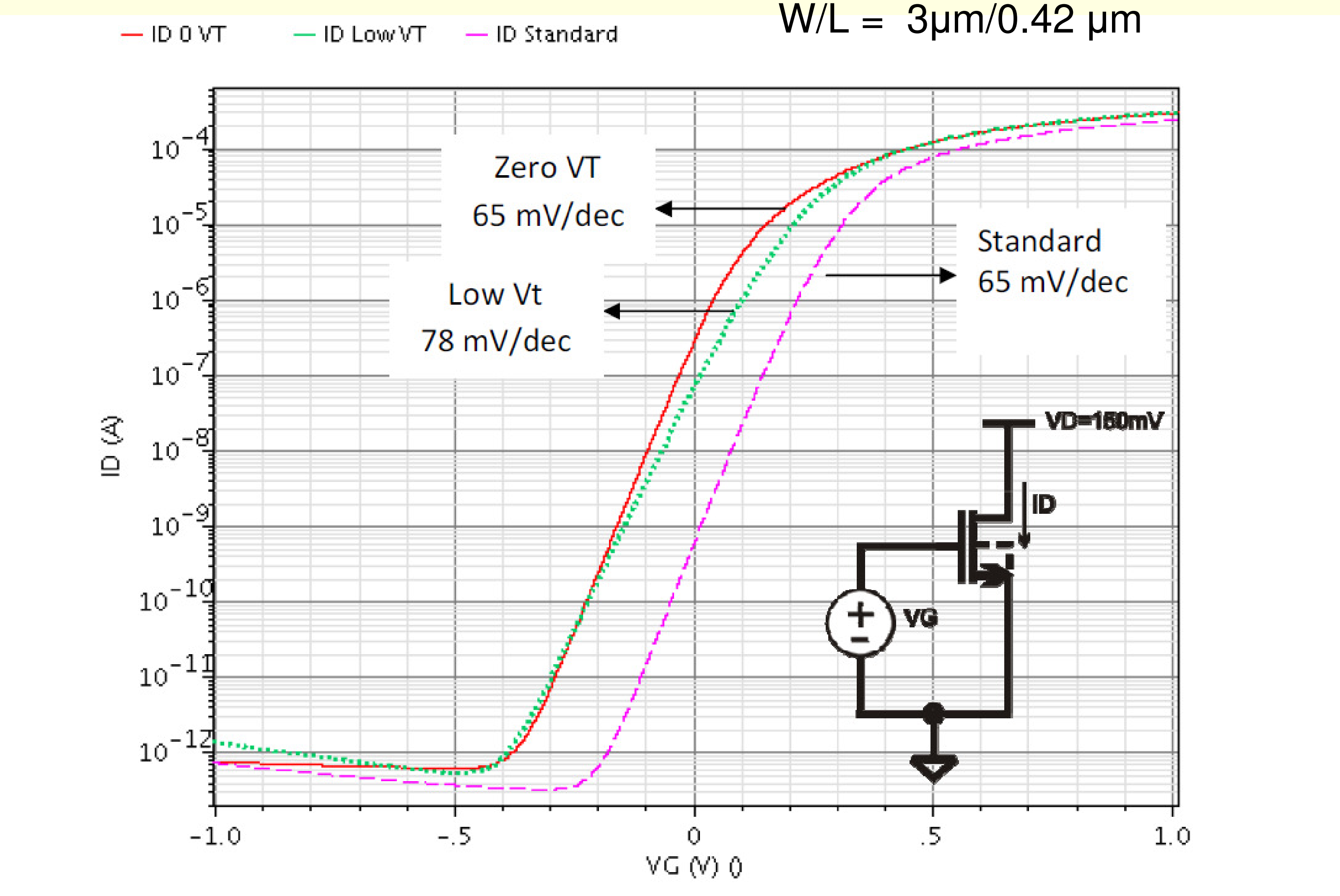
$$I_{DS} = I_D = I_0 \left(e^{\frac{v}{\phi_t}} - 1 \right)$$

- Current I_0 of the DTMOS diode can be determined as the saturated drain current of the (conventionally connected) transistor with $V_{GB} = V_{SB} = 0$.

$$I_{DSsat} = I_F = 2I_S e^{-\frac{V_{T0}}{n\phi_t}} = I_0$$

Standard, low-VT and zero-VT MOSFETs in a 130 nm technology

W/L = 3μm/0.42 μm



Rectifier summary

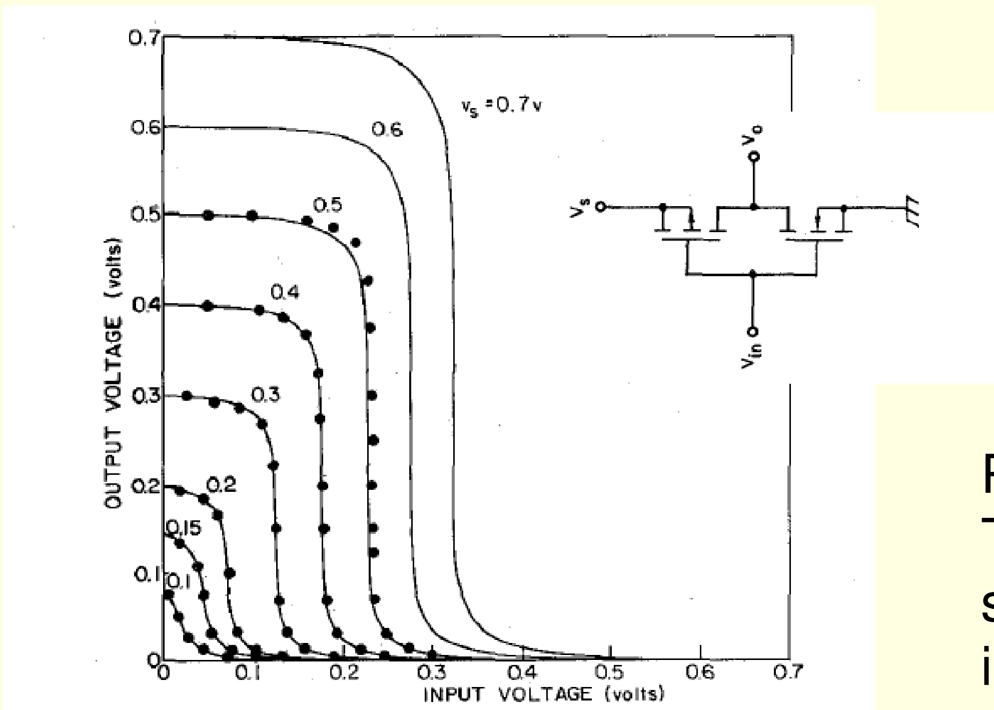
- Analytical model of the rectifier circuit in which the nonlinear device follows the diode Shockley (exponential) equation.
- The model is correct for input voltages down to below the thermal voltage.
- The main design parameter is the diode saturation current I_0.
- For a DTMOS (WI) diode $$I_0 \propto \frac{W}{L} e^{\frac{-V_{TO}}{n\phi_t}}$$

  we can take advantage of aspect ratio and of different V_T's

Oscillator outline

- ⇨Background: minimum supply voltage for FET circuits
- ⇨MOSFET charge based model
- ⇨Low voltage operation of the (C)MOS inverter
- ⇨Ring oscillator
- ⇨Colpitts oscillator

Background 1: minimum supply voltage for the CMOS inverter



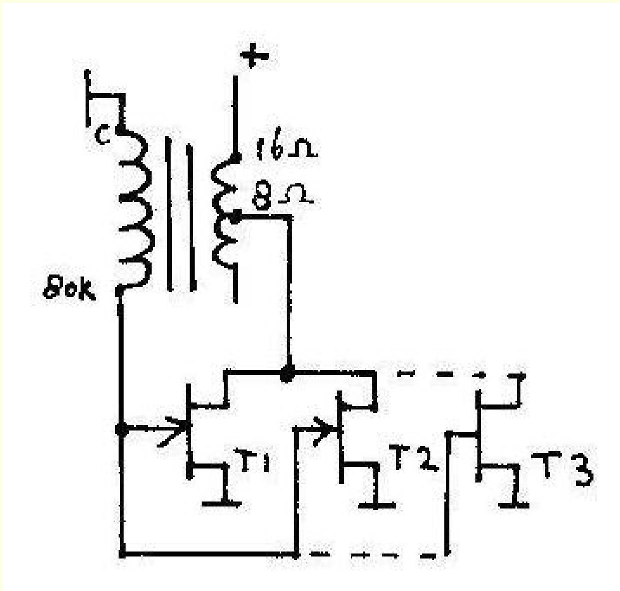
CMOS inverter transfer characteristics

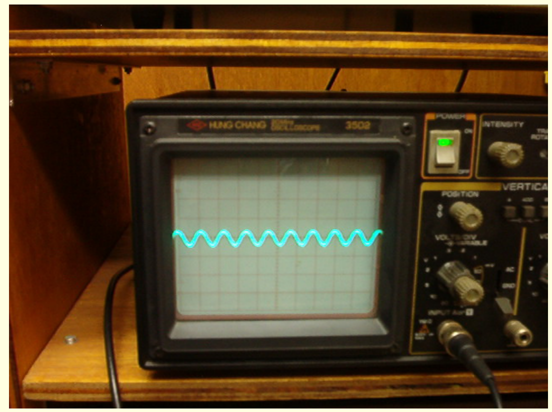
(Swanson and Meindl, IEEE JSSC 1972)

Prof. James Meindl: Theoretically, the minimum supply voltage for a CMOS inverter is
2 (ln2) (kT/q) = 36 mV
at room temperature
(IEEE JSSC, 2000)

Background 2: oscillators with super low supply voltage

Dick Kleijer, available at http://www.dicks-website.eu/fetosc/enindex.htm





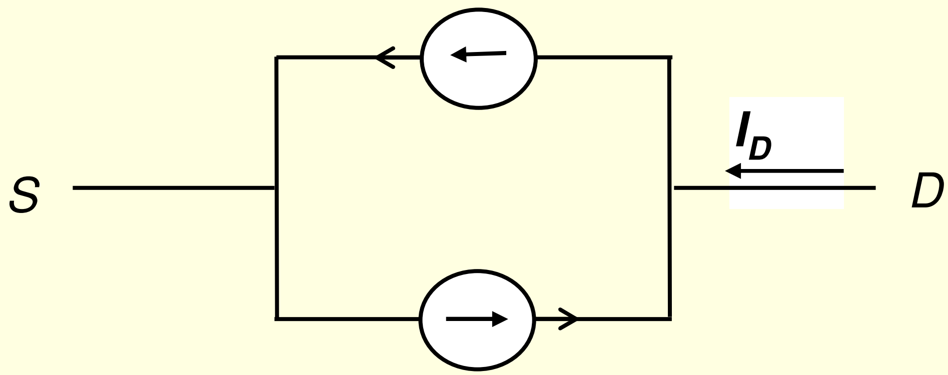
FET type	Supply voltage	Supply current
2x J 310	19 mV	1.04 mA
3x J 310	17 mV	1.40 mA

Oscillator with very high impedance winding (4 MΩ) transformer running on 5.5 mV supply voltage
Horizontal: 1 ms /div.
Vertical: 200 mV /div.

MOSFET charge-based model 1

$$I_S = \mu C'_{ox} n \frac{\phi_t^2}{2}\frac{W}{L} = I_{SQ}\frac{W}{L}$$

$$I_F = I_S\left(2q'_{IS} + q'^2_{IS}\right)$$



$$I_R = I_S\left(2q'_{ID} + q'^2_{ID}\right)$$

$$I_D = I_F - I_R$$

$$I_{F(R)} = I_S\left(2q'_{IS(D)} + q'^2_{I(S)D}\right)$$

W, L width, length of the channel

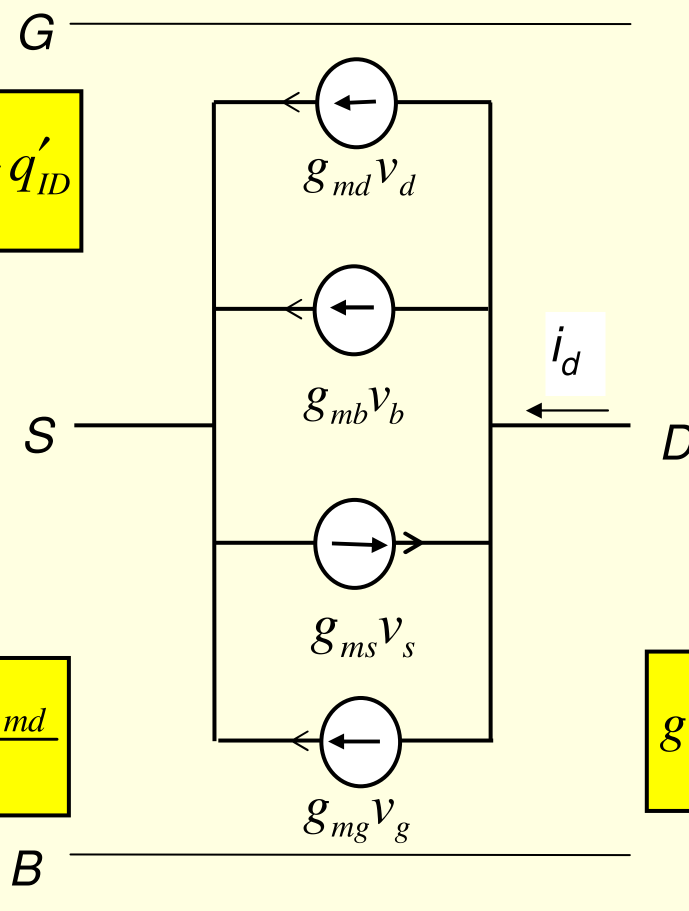
μ mobility, C'_{ox} gate capacitance per unit area, *n* slope factor (n = 1.2-1.6)

q'_{IS} *and* q'_{ID} are the normalized carrier densities (to the thermal charge $-nC'_{ox}\phi_t$) at source and drain.

I_S and I_{SQ} are the normalization (specific) and “sheet” normalization currents.

MOSFET charge-based model 2 : LF small signal model in the triode region

$$g_{md} = \frac{2I_S}{\phi_t} q'_{ID}$$



$$g_{mg} = \frac{g_{ms} - g_{md}}{n}$$

$$g_{ms} = \frac{2I_S}{\phi_t} q'_{IS}$$

$$g_{ms} = g_{mg} + g_{mb} + g_{md}$$

MOSFET charge-based model 3:the unified charge control model (UCCM)

V_P is the pinch-off voltage

$$\frac{V_P - V_S}{\phi_t} = q'_{IS} - 1 + \ln\left(q'_{IS}\right) \qquad \frac{V_P - V_D}{\phi_t} = q'_{ID} - 1 + \ln\left(q'_{ID}\right)$$

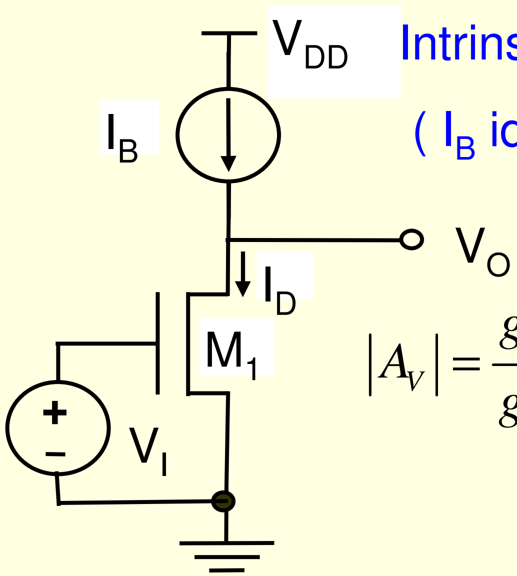
$$g_{ms} = \frac{2I_S}{\phi_t} q'_{IS} \qquad \frac{V_{DS}}{\phi_t} = q'_{IS} - q'_{ID} + \ln\left(\frac{q'_{IS}}{q'_{ID}}\right) \qquad g_{md} = \frac{2I_S}{\phi_t} q'_{ID}$$

$$V_{DS} = \frac{\phi_t^2}{2I_S}\left(g_{ms} - g_{md}\right) + \phi_t \ln\left(\frac{g_{ms}}{g_{md}}\right)$$

In WI

$$\frac{g_{ms}}{g_{md}} = \frac{q'_{IS}}{q'_{ID}} = e^{\frac{V_{DS}}{\phi_t}}$$

Low-voltage operation of the MOS inverter (WI / triode region)



Intrinsic gain stage

(I_B ideal current source)

weak inversion operation

$$|A_V| = \frac{g_{mg}}{g_{md}} = \frac{g_{ms} - g_{md}}{n g_{md}} = \frac{1}{n}\left(\frac{g_{ms}}{g_{md}} - 1\right)$$

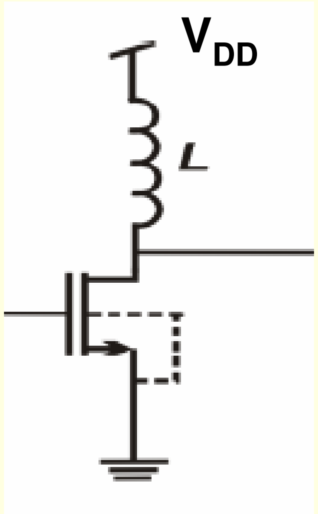
$$\frac{g_{ms}}{g_{md}} = \frac{q'_{IS}}{q'_{ID}} = e^{\frac{V_{DS}}{\phi_t}}$$

$$|A_V| = \frac{1}{n}\left(e^{\frac{V_{DS}}{\phi_t}} - 1\right)$$

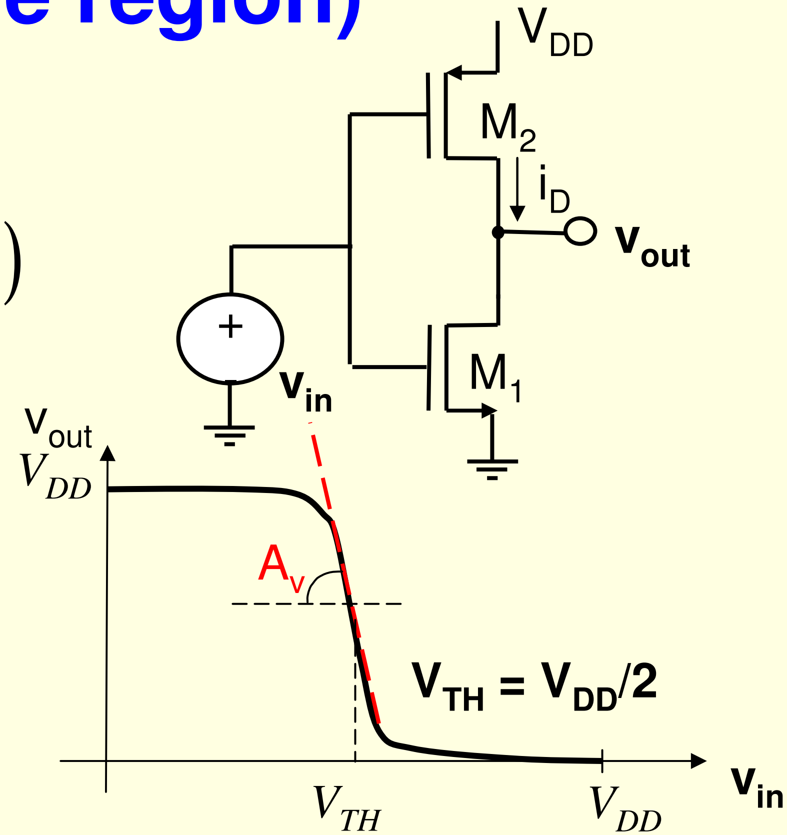
or

$$V_{DS} = \phi_t \ln\left(1 + n|A_V|\right)$$

Low–voltage operation of the (C)MOS inverter (WI / triode region)



$$V_{DS} = \phi_t \ln\left(1 + n\left|A_V\right|\right)$$



Minimum supply voltage for amplification $\left|A_V\right| = 1$

'ideal' MOSFET ***n*** **= 1**

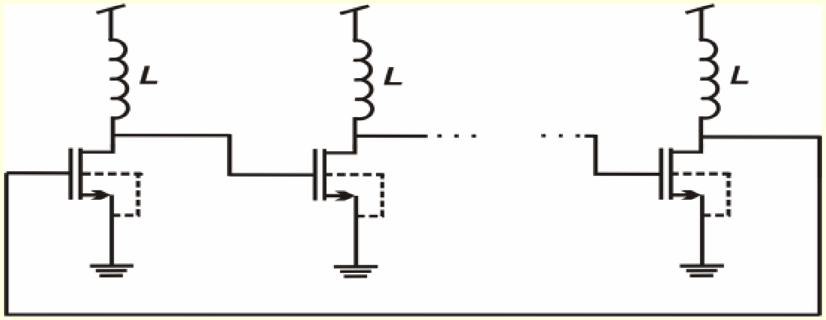
$$V_{DS} = V_{DD}$$

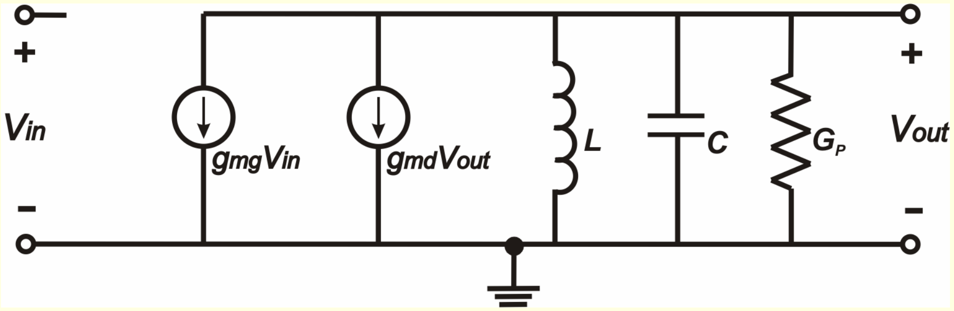
$$V_{DD\min} = (\ln 2)\phi_t$$

$$V_{DS} = V_{DD}/2$$

$$V_{DD\min} = 2(\ln 2)\phi_t$$

Ring oscillator 1





$$\frac{V_{out}}{V_{in}} = -\frac{g_{mg}}{g_{md}+G_p}\frac{1}{1+j\tan\theta}$$

Minimum gain for oscillation ⇨ $$\frac{g_{mg}}{g_{md}+G_p}\frac{1}{\sqrt{1+\tan^2\theta}} > 1$$

For the sake of simplicity, we consider θ = *π*. ⇨ $$\frac{g_{mg}}{g_{md}+G_p} > 1$$

Ring oscillator 2

Minimum gain for oscillation

$$\frac{g_{mg}}{g_{md}+G_p}=\frac{g_{ms}-g_{md}}{n\left(g_{md}+G_p\right)}>1$$

or

$$\frac{g_{ms}}{g_{md}}\geq 1+n\left(1+\frac{G_p}{g_{md}}\right)$$

From the UCCM

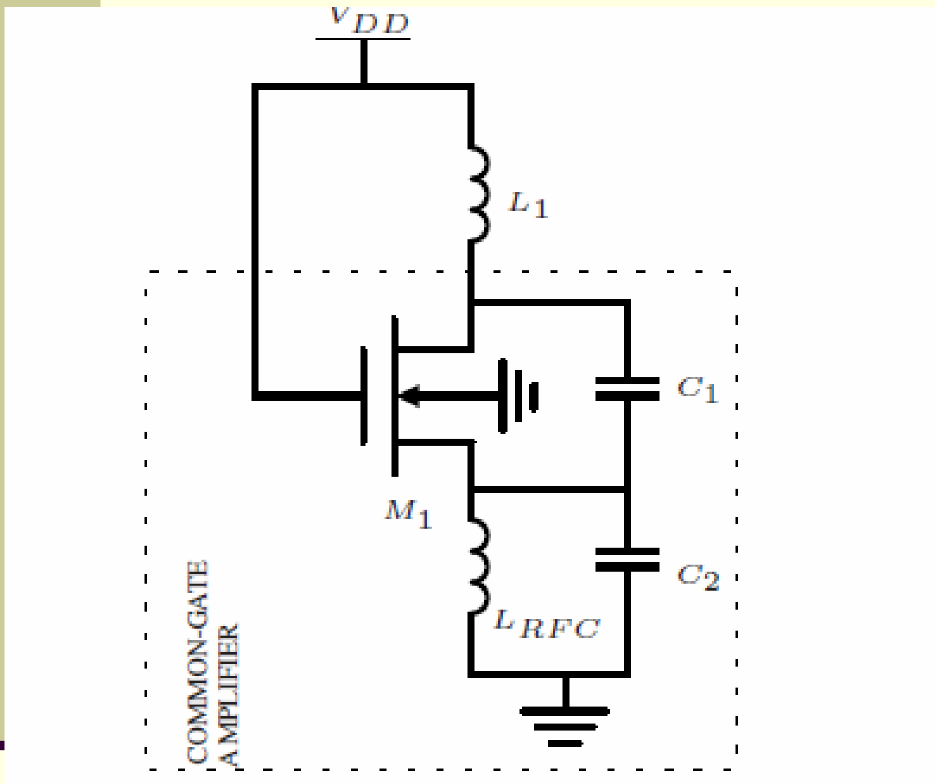
$$V_{DD\min}=\frac{\phi_t^2}{2I_S}n\left(g_{md}+G_p\right)+\phi_t\ln\left[1+n\left(1+\frac{G_p}{g_{md}}\right)\right]$$

SI **WI**

Considering high Q inductor ($G_P << g_{md}$) and WI operation and n = 1

$$V_{DD\min}=\left(\ln 2\right)\phi_t$$

Colpitts oscillator 1



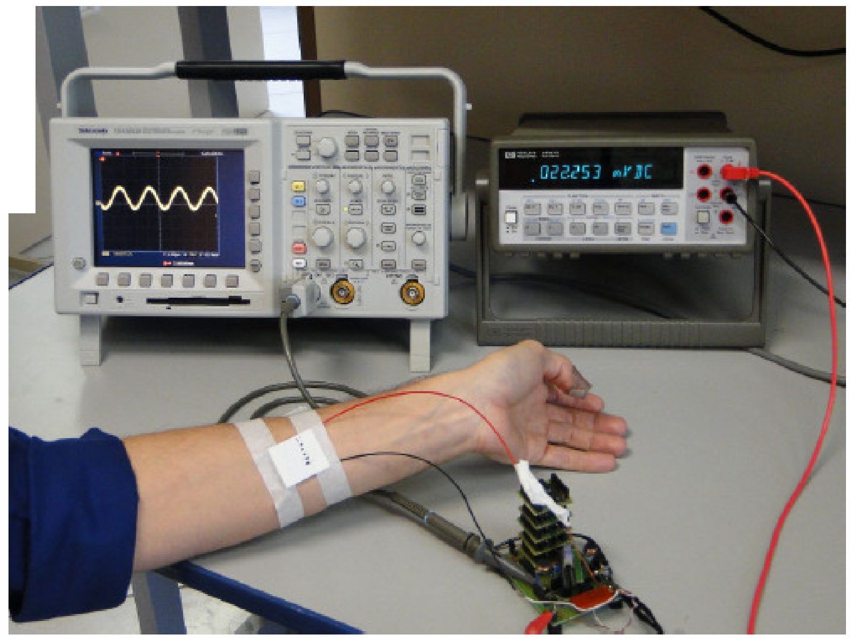
For high *Q* inductor (*$G_{inductor}$*<< *g_{md}*) and WI operation

$$V_{DD\min} \cong \phi_t \ln\left(1 + n\frac{C_2}{C_1}\right)$$

Colpitts oscillator 2

TRANSISTOR CHARACTERISTICS MEASURED FOR $V_{DD} = 20\,mV$ AT $T = 23\,^{o}C$.

Parameter	Value
I_S (Specific Current)	11.18 μA
V_{TH} (Threshold Voltage)	59 mV
g_{ms} (Source Transconductance)	520 μA/V
g_{md} (Drain Transconductance)	325 μA/V
n (Slope factor)	1.6



Photograph of the oscillator working from a thermoelectric generator at T=24 ^{o}C.

Oscillator summary

- There is no hard low voltage limit for analog MOS circuits (oscillators can operate with supply voltage under kT/q)
- The ideal active device for low voltage operation is a MOSFET with threshold voltage near zero
  (for WI operation at low supply voltage)
- The charge based MOSFET model is very convenient for the design of ultra-low-voltage circuits (operation in triode region/ WI)

References

- M. C. Schneider and C. Galup-Montoro, *CMOS Analog Design Using All-Region MOSFET Modeling*, Cambridge University Press, 2010.
- A. J. Cardoso, L. G. de Carli, C. Galup-Montoro, and M. C. Schneider, "Analysis of the rectifier circuit valid down to its low-voltage limit, " *IEEE Transactions on Circuits and Systems I*, 2011.
- F. R. de Sousa, M. B. Machado, C. Galup-Montoro, " A 20 mV Colpitts Oscillator powered by a thermoelectric generator, submitted to *ISCAS 2012*.