CHAPTER 3

PROGRAMMABLE SECOND GENERATION SWITCHED-CURRENT INTEGRATOR AND BIQUAD FOR LOW-VOLTAGE APPLICATIONS

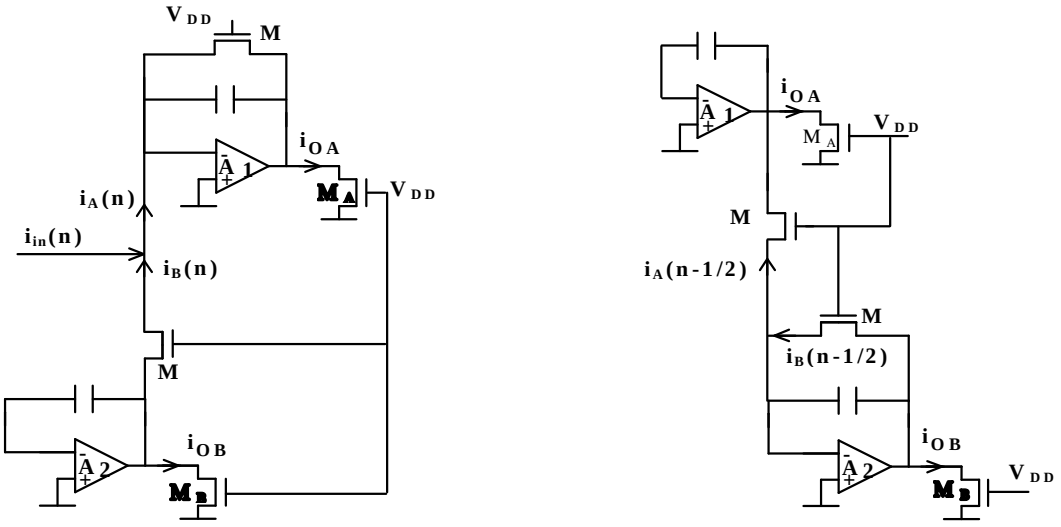
3.1 INTRODUCTION

In this chapter we propose a second generation SI integrator. The proposed integrator has been prototyped and programmed by using MOSFET-Only Current Dividers (MOCD) [33]. The consequence of the op-amp offset on the integrator performance has been studied. A programmable integrator-based biquad, which allows independent tuning of the center frequency and the quality factor has been implemented.

3.2 SECOND GENERATION INTEGRATOR

3.2.1 BASIC CELL

In this section, we propose a second generation SI integrator based on the SI mirror proposed in [21]. The proposed integrator is made up of two switched-current memory cells. Fig. 3.1 shows the proposed integrator at different clock phases. Two outputs are available, i_{OA} and $i_{OB.}$ As in the conventional second generation SI integrator (Fig. 2.4. (b)), the input current together with the feedback current are fed to the first S/H (M_1) at the first half cycle. At the next half clock cycle, the stored signal is held on the second S/H (M_2).



(a) At t=n. **(b)** At t = n-1/2.

Fig. 3.1. The low-voltage SI integrator on different phases.

The analysis of the integrator at the two clock phases is as follows:

$$i_{OA}(n) = -\alpha\, i_A(n) = -\alpha\{i_{in}(n) + i_B(n)\} \tag{3.1.a}$$

and

$$i_B(n) = i_B(n-1/2) \tag{3.1.b}$$

On the previous half cycle, the currents are

$$i_B(n-1/2) = i_A(n-1/2) \tag{3.1.c}$$

and

$$i_A(n-1/2) = i_A(n-1) \tag{3.1.d}$$

From (3.1), we can write

$$i_{OA}(n) = -\alpha\, i_{in}(n) + i_{OA}(n-1) \tag{3.2.a}$$

and

$$i_{OB}(n) = \gamma\, i_{in}(n-1) + i_{OB}(n-1) \tag{3.2.b}$$

where $\alpha = (W/L)_{MA}/(W/L)_M$ and $\gamma = (W/L)_{MB}/(W/L)_M$. W and L are the channel width and length, respectively.

The z-transform of (3.2.a) and (3.2.b) gives:

$$\frac{I_{OA}^{\phi_o}}{I_{in}^{\phi_o}} = -\alpha \frac{1}{1 - z^{-1}} \tag{3.3.a}$$

$$\frac{I_{OB}^{\phi_o}}{I_{in}^{\phi_o}} = \gamma \frac{z^{-1}}{1 - z^{-1}} \tag{3.3.b}$$

An SI integrator which allows for the possibility of several input currents together with its timing diagram are illustrated in Fig 3.2. This timing diagram is necessary to avoid the loss of information during clock transition in a practical implementation.

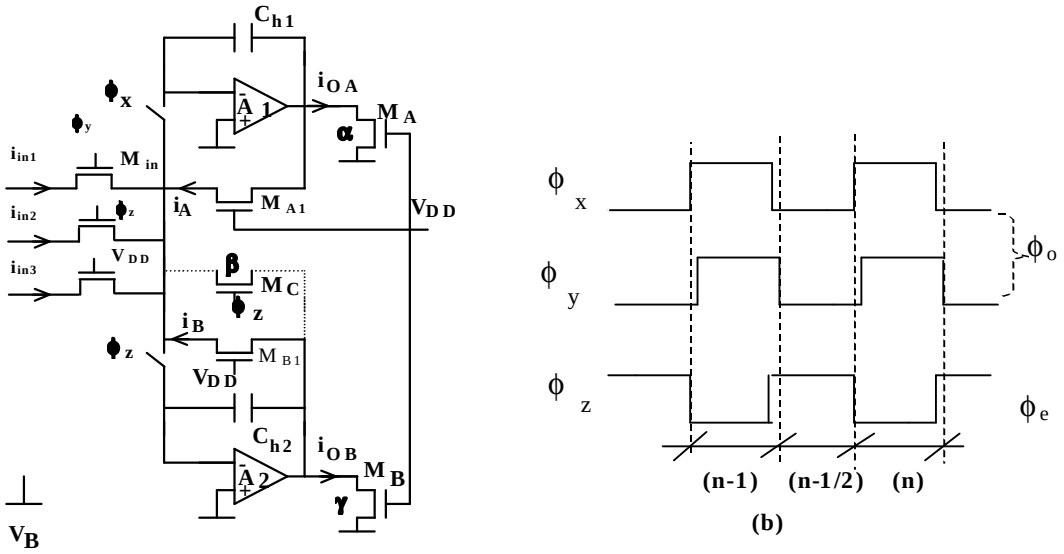


Fig. 3.2. The low-voltage second generation SI integrator.

(a) Circuit schematic.

(b) Clock phases.

Assuming that all MOS transistors have the same aspect ratios (W/L), the output/input relations are summarized in Table. 3.1. The continuous input (i_{in3}) is a sampled/held signal. If i_{in3} is sampled on the odd phase and held on the even phase, it is denoted as (odd+even). Conversely, if it is sampled on the even phase and held on the odd phase it is denoted as (even+odd). Table 3.1 illustrates that the proposed integrator allows performing forward, backward, and lossless discrete integrators which together, with inversion, give some flexibility for the biquad design.

Table 3-1. Transfer functions of the SI integrator in Fig. 3.2 (a).

	$I_{in1}^{\phi_o}$	$I_{in2}^{\phi_e}$	Continuous signal (I_{in3})	
			odd+even[1]	Even+odd[2]
$I_{OA}^{\phi_o}$	$-1 / (1-z^{-1})$	$z^{-1/2} / (1-z^{-1})$	-1	0
$I_{OA}^{\phi e}$	$-z^{-1/2} / (1-z^{-1})$	$z^{-1} / (1-z^{-1})$	$-z^{-1/2}$	0
$I_{OB}^{\phi_o}$	$z^{-1} / (1-z^{-1})$	$-z^{-1/2} / (1-z^{-1})$	0	$-z^{-1/2}$
$I_{OB}^{\phi_e}$	$z^{-1/2} / (1-z^{-1})$	$-1 / (1-z^{-1})$	0	-1

1. An odd+even signal is sampled at ϕ_o and held constant at ϕ_e.
2. An even+odd signal is sampled at ϕ_e and held constant at ϕ_o.

A lossy SI integrator can be realized using the dotted feedback path shown in Fig. 3.2. (a). The z-domain transfer functions are:

$$\frac{I_{OA}^{\phi_o}}{I_{in}^{\phi_o}} = -\alpha \frac{1}{1+\beta-z^{-1}} \tag{3.4.a}$$

$$\frac{I_{OB}^{\phi_o}}{I_{in}^{\phi_o}} = \gamma \frac{z^{-1}}{1+\beta-z^{-1}} \tag{3.4.b}$$

where $\beta=(W/L)_{MC} / (W/L)_{MB1}$ and $i_{in}=i_{in1}$.

The MOS transistor responsible for the loss must be clocked in the even phase; otherwise, the feedback factor would be $(1+\beta)I_{OB}z^{-1}$ which means that the integrator would become unstable.

The integrator with this topology has an axis that divides it into two identical sections, thus reducing the effects of charge injection [25]. Ideally, the charges injected by the two switches and clock feedthrough are equal. However, current errors due to charge injection are not canceled out due to circuit mismatch and nonlinearities. The proposed second generation SI integrator has the same sensitivities to transistor

mismatch [32] as the conventional second generation SI integrator in [20]. In the integrator proposed here, the switches operate at constant voltage [36, 37], which means that the charge injected into the holding capacitors (C_{h1} and C_{h2}) is signal-independent. Thus, the proposed integrator is capable of achieving higher accuracy than the conventional SI integrator. Moreover, if the voltage V_x obtained from the network in Fig. 2.5.(c) is applied into the non-inverting input of the op-amps, the conduction gap [8, 10] existing in conventional SI circuits is avoided. Therefore, the SI topologies proposed here are more suitable for low voltage applications than the conventional ones.

- **SIMULATION**

The SI integrator shown in Fig. 3.2.(a) has been simulated using the SMASH [38] simulator together with ACM MOSFET model [22]. The circuit was simulated for 8μA (20kHz) input signal, 1MHz sampling rate and C_{h1}= C_{h2}=0.5pF. The aspect ratios are 5.6μm/5.6μm for the MOS transistor and 3μm/0.7μm for the nMOS switches. The detailed design of the two-stage op-amp is presented in Appendix B. The simulation result is shown in Fig. 3.3. The offset between i_{AO} and i_{OB} is due to the offset voltage mismatch between the opamps. A linear voltage-to-current converter has been implemented using a linear resistor.

3.2.2 THE EFFECT OF THE OP-AMP OFFSET VOLTAGE

Fig. 3.4 illustrates the proposed SI integrator considering op-amp offsets. The operating voltages of the switches are V_B+V_{OFF1} or V_B+V_{OFF2}. This difference generates a current error proportional to the difference between the offsets. This problem is

exactly the same as in the conventional SI integrator if mismatch between the current sources (see Fig. 2.4) is taken into account.

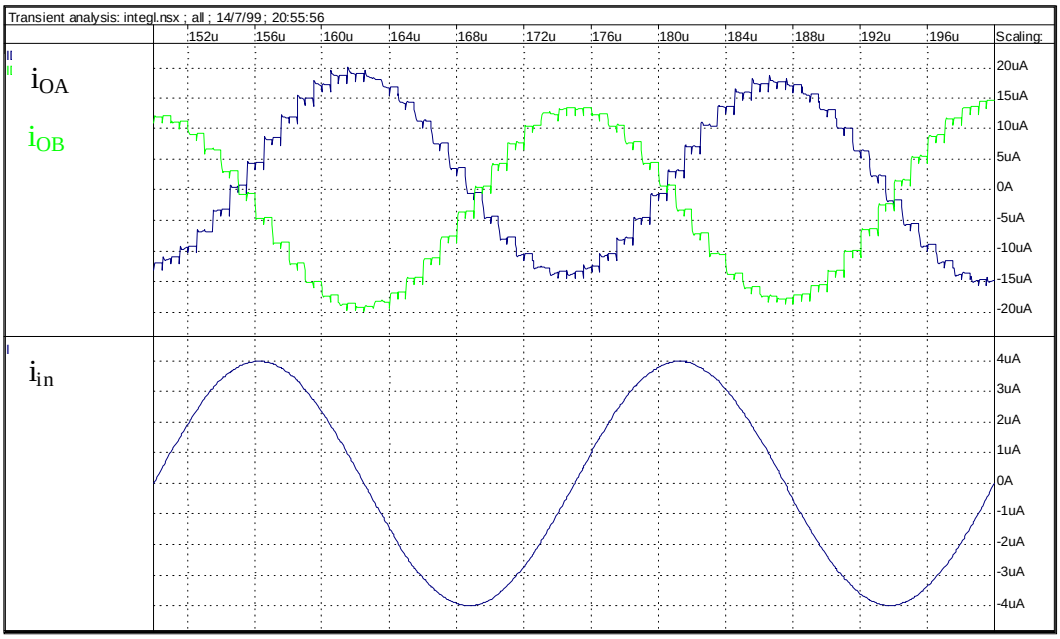


Fig. 3.3. Sinusoidal steady state response of the low-voltage integrator.

In this section, we analyze the effects of the op-amp offsets on the output voltage. The offset voltages have been considered as time-invariant signals and the input current is zero. The analysis of the SI second generation integrator leads to:

$$V_{OA}^{o} = \frac{B' + A - Az^{-1}}{A(1-z^{-1})} V_{OFF1}^{o} + \frac{z^{-1/2}}{1-z^{-1}} V_{OFF1}^{e} - \frac{B}{A(1-z^{-1})} V_{OFF2}^{o} - \frac{A' z^{-1/2}}{A(1-z^{-1})} V_{OFF2}^{e} \quad (3.5.a)$$

$$V_{OA}^{e} = \frac{B' z^{-1/2}}{A(1-z^{-1})} V_{OFF1}^{o} + \frac{1}{1-z^{-1}} V_{OFF1}^{e} - \frac{Bz^{-1/2}}{A(1-z^{-1})} V_{OFF2}^{o} - \frac{A' z^{-1}}{A(1-z^{-1})} V_{OFF2}^{e} \quad (3.5.b)$$

$$V_{OB}^{o} = -\frac{B' z^{-1}}{B(1-z^{-1})} V_{OFF1}^{o} - \frac{Az^{-1/2}}{B(1-z^{-1})} V_{OFF1}^{e} + \frac{1}{(1-z^{-1})} V_{OFF2}^{o} + \frac{A' z^{-1/2}}{B(1-z^{-1})} V_{OFF2}^{e} \quad (3.5.c)$$

$$V_{OB}^{e} = -\frac{B' z^{-1/2}}{B(1-z^{-1})} V_{OFF1}^{o} - \frac{A}{B(1-z^{-1})} V_{OFF1}^{e} + \frac{z^{-1/2}}{(1-z^{-1})} V_{OFF2}^{o} + \frac{A' + B - Bz^{-1}}{B(1-z^{-1})} V_{OFF2}^{e} \quad . \quad (3.5.d)$$

$A\alpha(W/L)_{MA1}$, $B\ \alpha\ (W/L)_{MB1}$, $A' = A + \sum K_{in}^{e}$, $B' = B + \sum K_{in}^{o}$ and $K^{o}_{in}\ \alpha\ (W/L)_{Min}$

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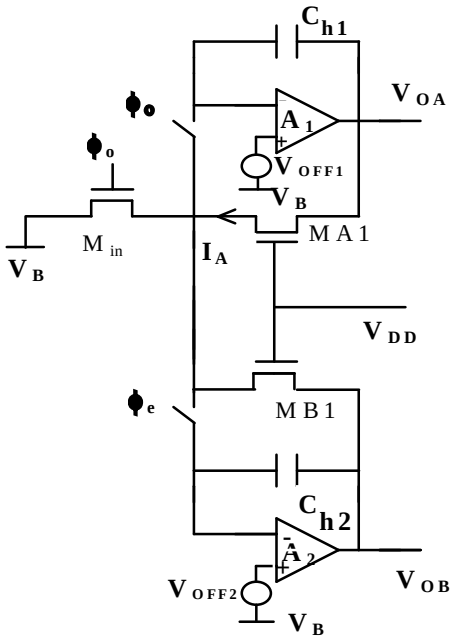

Fig. 3.4. Scheme of the low-voltage SI integrator including op-amp offset voltages.

The error in the output current I_A at odd phase is denoted by ΔI_A^{o}

$$\Delta I_A^{o}(Z) = A\left[(V_{OA}^{o} - V_{OFF1}^{o}) - Z^{-1/2}(V_{OA}^{e} - V_{OFF2}^{e})\right] \tag{3.6}$$

Assuming zero initial condition and zero input (no current at M_{in} due to offset voltages), the output current (I_A) due to the offset voltages is

$$I_A^{o}(1 - z^{-1}) = B(V_{OFF1}^{o} - V_{OFF2}^{o}) \tag{3.7}$$

Therefore, if the two op-amps have equal offset voltages, the current error will tend to zero. However, for the general case $V_{OFF1} \neq V_{OFF2}$, and the difference in the offset voltages will affect the dynamic range of the circuits. Thus, the op-amp offset presents a major problem for the proposed integrator. So it is important to overcome this drawback by using dynamic [39] or offset compensation techniques as in SC circuit [40].

- **OFFSET COMPENSATION [40]**

Fig. 3.5.(a) illustrates an SI sample-hold circuit with offset compensation. The circuit works as follows. When ϕ_c is high, the offset voltage is stored into C_c. Consequently, when ϕ_c is low the offset appears as an input signal and its effects are ideally canceled out.

The switches in Fig. 3.5.(a) still work at constant DC voltage. Thus, this circuit avoids the conduction gap. The offset-insensitive second generation SI integrator is shown in Fig. 3.5.(b).

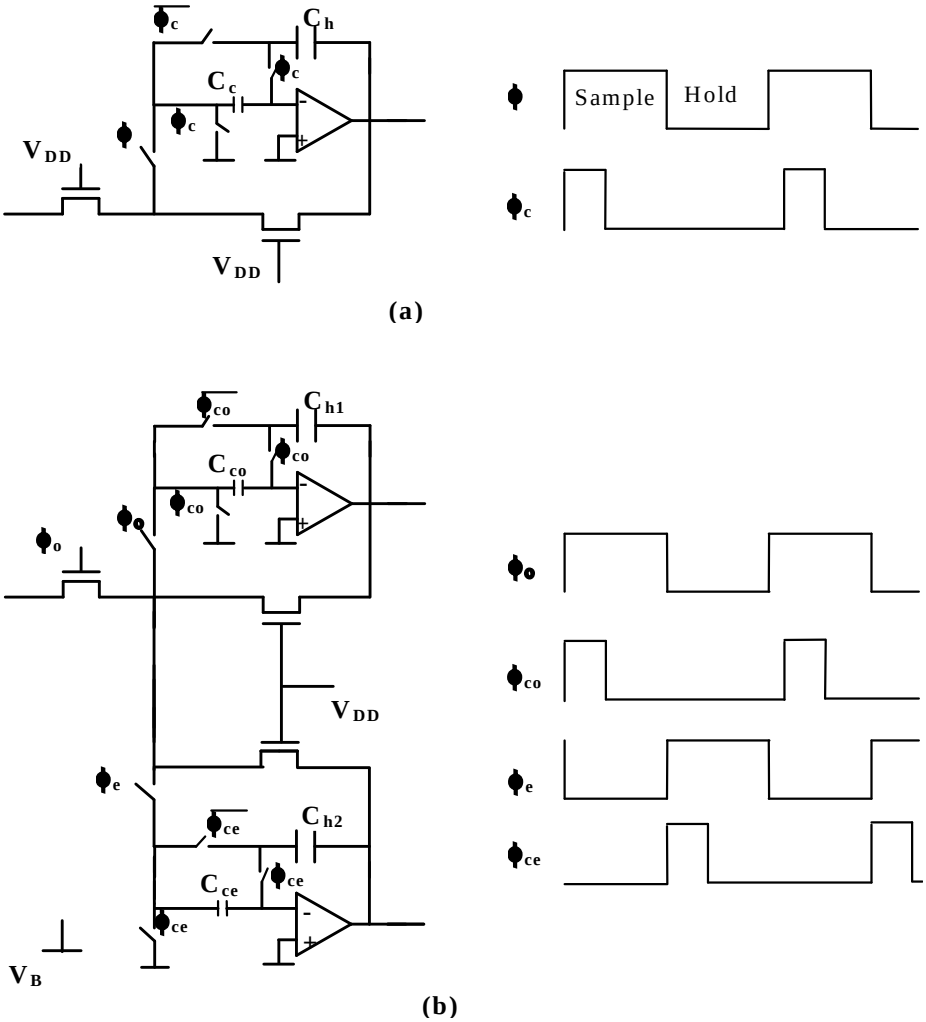

Fig. 3.5. Offset compensation for the SI technique [40].

(a) Sample hold circuit.

(b) Second generation integrator and clock diagram.

- **EXPERIMENTAL RESULTS** [1]

The SI lossy integrator shown in Fig. 3.2.(a) was implemented using operational amplifiers TL 082, MOS integrated transistors (W=48μm, L=1.2 μm), MOS switches CD 4007 and holding capacitors of 1.8nF. The loss factor (β) was set by a 6-bit MOSFET-Only Current Divider (MOCD). The 6-bit MOCD was integrated on a Sea-of-Transistors (SoT) array, in a 1.2μm technology from ES2 [41]. The MOCD is switched by "ANDing" the digital word and the even phase waveforms $\{\phi_e.\mathbf{b}(b_{N-1} .....b_o)\}$. The integrator has been simulated using the ASIZ program [42]. The simulated and experimental frequency responses presented in Fig. 3.6 show excellent agreement.

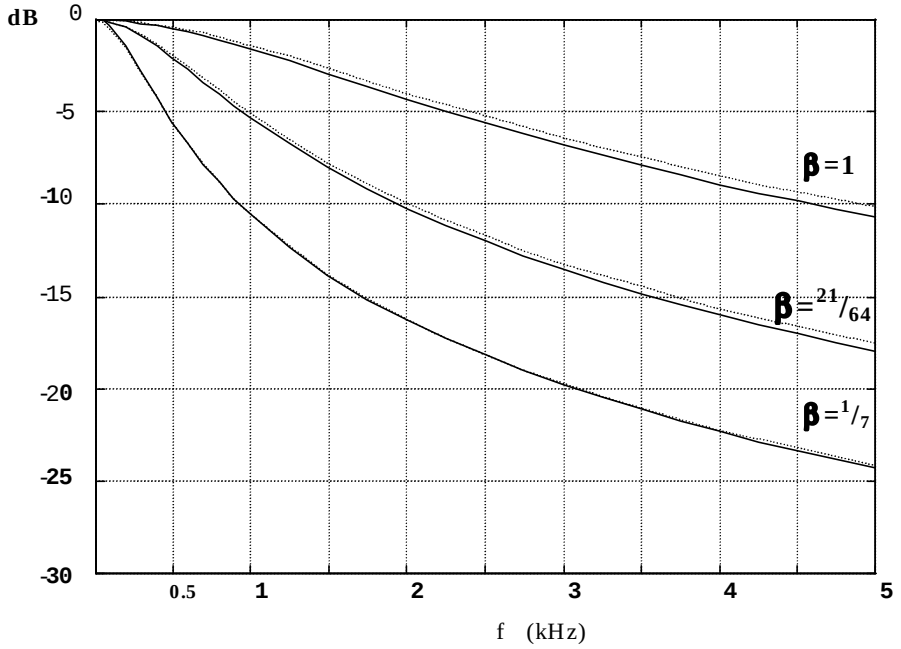

Fig. 3.6. Frequency response of the low-voltage second generation SI integrator in Fig.3.2 ..... -Theoretical and __-Experimental.

[1] The experimental work has been done by M. Sc. Renato Faustino.

3.3 SECOND ORDER SECTION

The second generation SI integrator has been applied to a programmable second order biquad. In this biquad section, the normalized center frequency (ω_O T) and the quality factor (Q) can be controlled independently. The design algorithm, the prewarped error and the switched current realization of the biquad section are described next.

3.3.1 GENERAL BLOCK DIAGRAM

The block diagram of a second order filter is shown in Fig. 3.7. The general transfer function is

$$\frac{X_{O/P}(S)}{X_{IN}(S)} = -\frac{K_3S^2 + K_2a_1fS + K_1a_1a_2}{S^2 + a_1fS + a_1a_2} \tag{3.8}$$

where S=sT is the normalized frequency.

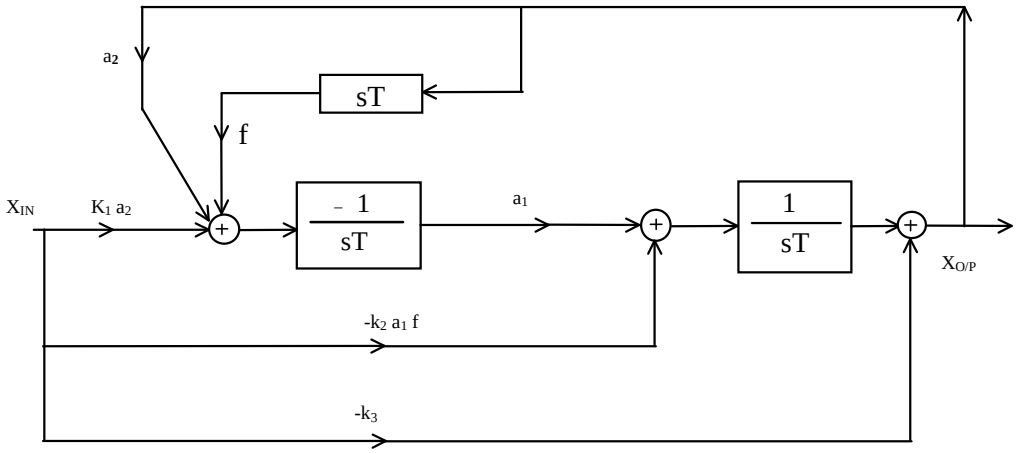

Fig. 3.7. Block diagram of a biquad.

In (3.8), the normalized center frequency and quality factor of the biquad are described as

$$\omega_o T = \sqrt{a_1 a_2} \tag{3.9.a}$$

$$Q = \frac{1}{f}\sqrt{\frac{a_2}{a_1}} \qquad (3.9.b)$$

where ω_o is center frequency and Q is the quality factor.

This biquad allows one to obtain low-pass (K_2 and K_3 = 0), bandpass (K_1 and K_3 = 0), high-pass (K_1 and K_2 =0), band-reject (K2=0), and all-pass filters.

3.3.2 MAPPING ERROR ANALYSIS

A common approach to design sampled-data filter is to obtain H (z) from the s-domain transfer function H (S). The mapping from the S- to the Z-domain is achieved via a transformation of the frequency variable. In this work, we will obtain the biquad circuit parameters directly from the analog specifications, namely, the center frequency (ω_O), the quality factor (Q) and the gain (K_o) at the center frequency. The errors in center frequency, quality factor and gain owing to frequency mapping must be taken into account. The error in both ω_O and Q due to prewarping have been studied elsewhere [43]. In this section, the magnitude error {|H (i ω_O)|} at the center frequency has been analyzed as follows.

The power series of the z-domain variable up to the second order term is

$$z^{-1} = e^{-i\,\omega T} \approx 1 + (-i\,\omega T) + (-i\,\omega T)^2/2! + (-i\,\omega T)^3/3! \qquad (3.10)$$

The application of backward Euler transformation ($ST=1-z^{-1}$) to the bandpass filter (K_1 and K_3 =0 in equation 3.8) leads to

$$H(z) = \frac{K_2 \frac{\omega_o T}{Q}(1-z^{-1})}{(1-z^{-1})^2 + \frac{\omega_o T}{Q}(1-z^{-1}) + (\omega_o T)^2} \qquad (3.11)$$

From (3.10) and (3.11), the magnitude of the transfer function at the center frequency {|H ($i\omega_O$ T)|} is

$$\left|H(i\omega_O T)\right| \approx \frac{K_2}{\omega_O TQ + 1} \tag{3.12}$$

which is equal to K_2 if $Q\omega_o T << 1$

Fig.3.8 shows the magnitude error at the center frequency as function of the normalized frequency (F_o/F_{CK}) for different quality factors. F_o is equal to $2\pi/\omega_o$ and F_{CK} is equal to 1/T. The error can be very large specially for high-Q filters and large F_o/F_{CK} ratios. The error of the backward LDI transformation [43] leads to a considerably smaller magnitude error at F_o, as shown in Fig. 3.9.

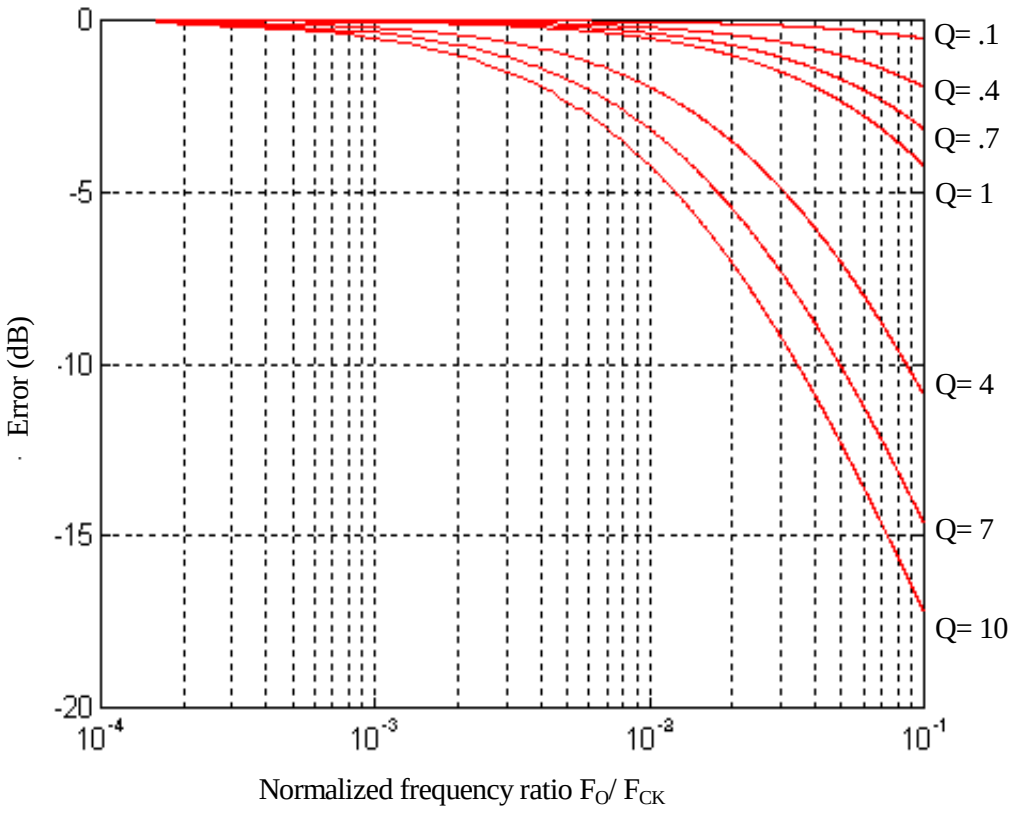

Fig. 3.8. Magnitude error at the center frequency for backward Euler transformation.

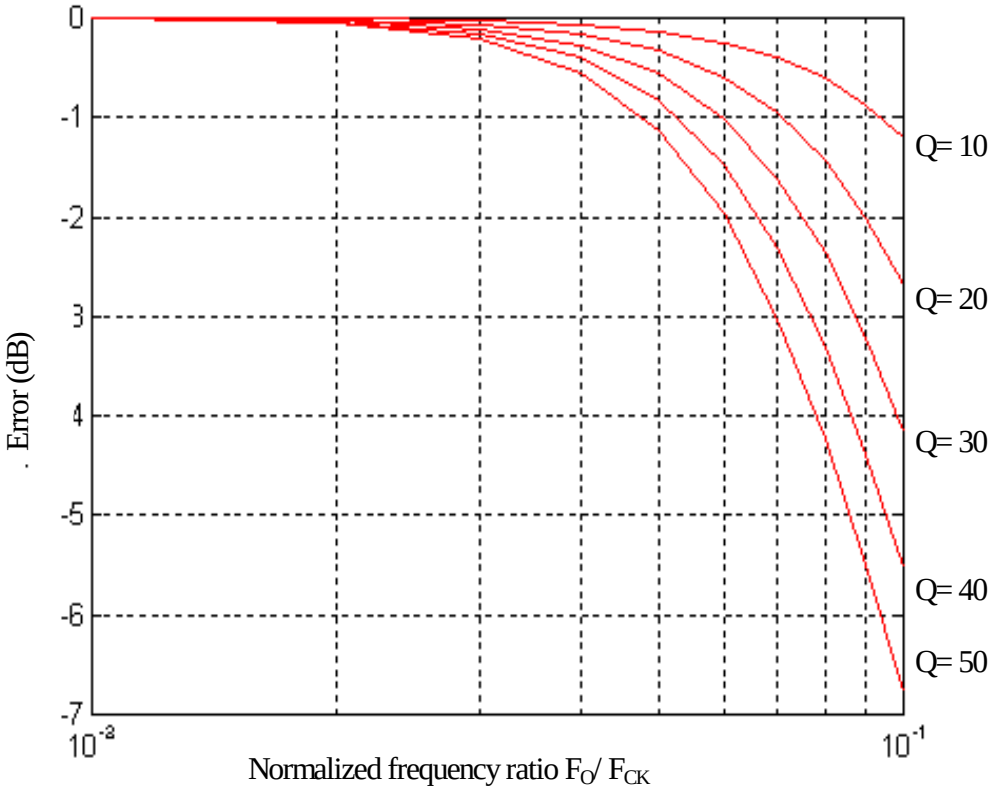

Fig. 3.9. Magnitude error at the center frequency for the backward LDI transformation.

3.3.3 IMPLEMENTATION OF THE SWITCHED-CURRENT BIQUAD

As an application of the proposed SI integrator, we have designed a biquadratic section by using backward LDI transformation [43]. The biquad presented in Fig. 3.7 has been realized as shown in Fig. 3.10. The output current as function of the inputs is

$$I_o(z) = -\frac{K_3.I_3.(1-z^{-1})^2 + K_2.I_2 a_2.f.(1-z^{-1})z^{-1} + K_1.I_1.a^2 z^{-1}}{1-(2-a_1.f-a_1 a_2)z^{-1} + (1-a_1 f)z^{-2}} \qquad (3.13)$$

Using $z \cong 1+sT+ (sT)^2/2!$ in (3.13), the normalized center frequency ($\omega_o T$) and the quality factor (Q) can be approximated as

$$\omega_o T = \sqrt{\frac{a_1 a_2}{1 - a_1 f}} \qquad (3.14.a)$$

$$Q = \frac{\sqrt{(1 - a_1 f) a_1 a_2}}{a_1 - f} \qquad (3.14.b)$$

When $a=a_1=a_2$, $a << 1$ and $af<<1$, both $\omega_o T$ and Q are controlled independently if the sampling frequency is much higher than the center frequency. In this case:

$$\omega_o T \cong a \qquad \text{and} \qquad Q \cong 1/f$$

The programmability of the biquad is achieved using the MOCD device [33]. In Fig. 3.10, the term "ϕ.x" means that the digital word "x" is ANDing with clock "ϕ" to implement the switching of the MOCD.

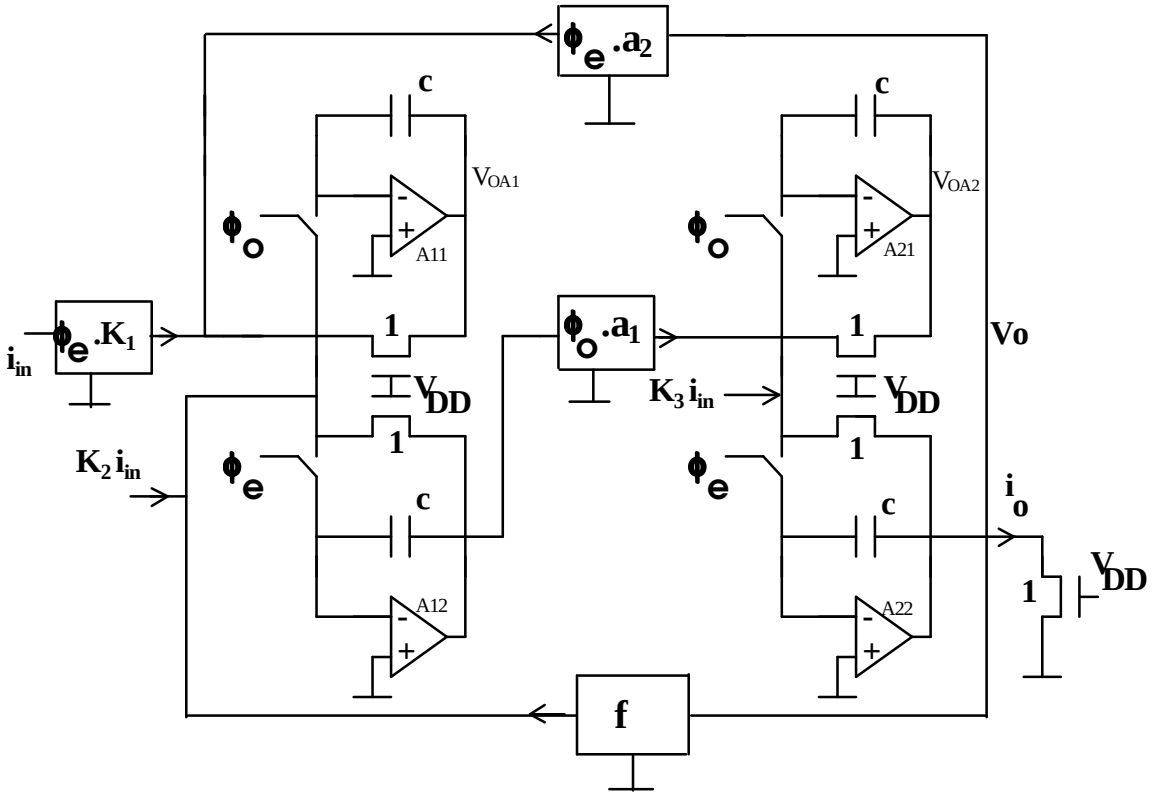

Fig. 3.10. Biquadratic section using second-generation SI integrators**.**

- **EXPERIMENTAL RESULTS**[1]

A discrete prototype of the filter has been implemented and tested. In this experimental work, transistors were replaced by resistors. The programmability of the filter was obtained by scaling the resistances. The unit resistor is 20kΩ, and the holding capacitors are C=100pF. The bandpass filter has been programmed for center frequencies f_o=150, 300 and 600Hz. The sampling frequency was 15kHz and the quality factor was equal to 8. The simulation and experimental results are shown in Fig. 3.11. In the case of very low $\omega_o T$, the error in the center frequency is large due to the variability of the resistors. To reduce this error we have to decrease the variability of the resistance or, for an IC implementation, increase the resolution of the MOCD.

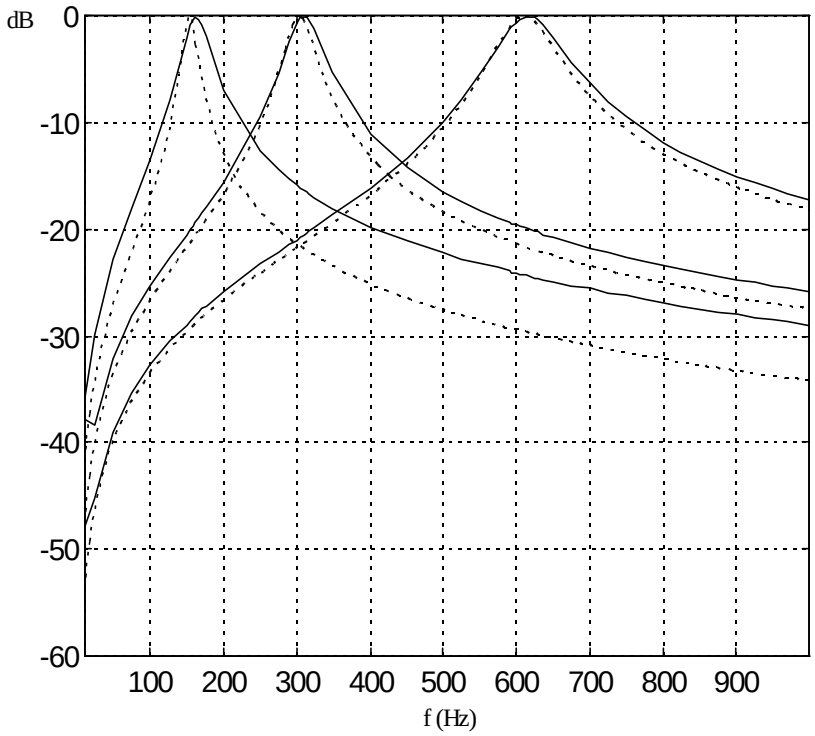

Fig. 3.11. Theoretical (....) and experimental (___) magnitude response of the bandpass filter. f_o=150, 300 and 600 Hz (Q=8 and F_{CK}=15kHz).

[1] The experimental work has been done by the M. Sc. Renato Faustino.

3.3.4 EFFECT OF THE OFFSET VOLTAGE OF THE OP-AMPS ON THE BIQUAD OUTPUT

As we have seen, the proposed SI integrator suffers from mismatch between the op-amp offset voltages. The output voltages due to op-amp offsets are:

$$V_{OA2}^{o}\{(1-z^{-1})^2 + a_1a_2z^{-1} + a_1fz^{-1}(1-z^{-1})\} =$$
$$\begin{aligned}&(2+k_3)\ (1-z^{-1})\ V_{12}\\ &-(1+(1+a_1+k_2+k_3)z^{-1})(1-z^{-1})\ V_{22}\\ &+a_1z^{-1}(k_1+a_2+f+2)\ V_{11}\\ &-a_1z^{-1}(1+(1+f)z^{-1})\ V_{21}\end{aligned} \qquad (3.15.a)$$

$$V_{OA1}^{e}\{(1-z^{-1})^2 + a_1a_2z^{-1} + a_1fz^{-1}(1-z^{-1})\} =$$
$$\begin{aligned}&+\{1+(k_1+a_2+f+1)z^{-1}\}(1-z^{-1})\ V_{11}\\ &-(2+f)z^{-1}(1-z^{-1})V_{21}\\ &(2+k_3)\{a_2+f(1-z^{-1})\}V_{12}\\ &-(1+(1+a_1+k_2+k_3)z^{-1})\quad (a_2+f(1-z^{-1})\ V_{22}\end{aligned} \qquad (3.15.b)$$

where V_{ij} is offset voltage of op-amp A_{ij} in Fig. (3.10), with i=1,2 and j=1,2.

To simplify expressions (3.15), we assume the offset to be a DC signal (z=1). Thus (3.15.a) and (3.15.b) become

$$V_{OA2}^{o} = \frac{k_1+a_2+f+2}{a_2}V_{11} - \frac{2+f}{a_2}V_{21} \qquad a_2 = \omega_oT \langle\langle \quad 1 \qquad 3.16.a)$$

$$V_{OA1}^{e} = \frac{k_3+2}{a_1}V_{12} - \frac{2+K_2+K_3+a_1}{a_1}V_{22} \qquad a_1 = \omega_oT \langle\langle \quad 1 \qquad (3.16.b)$$

where $K_1/a_2 = G_{DC}$ (DC gain), $f/a_2 = 1/(Q\ \omega_oT)$, $K_2/a_1 = Q\ G\ (\omega_oT)$ and $K_3/a_1 = G_{HF}/\omega_oT$.

Finally, the DC output caused by the op-amp offsets, Eqn. (3.16.a), is written as

$$V_O = (1+G_{DC})V_{off1} + (2+\frac{1}{Q})\frac{\Delta V}{\omega_oT} \qquad (3.17)$$

where ΔV is the offset mismatch $\{V_{off1}(A_{11})-V_{off2}(A_{12})\}$.

The DC component of the output, as given by (3.17), is not large provided that the sampling frequency is not very much higher than the center frequency of the biquad or the offset mismatch is not high. The dynamic technique presented in section (3.2.2) can be employed to reduce the effects of the offset mismatch.