CHAPTER 6

FILTER LAYOUT AND TESTING

6.1 INTRODUCTION

The layout art is one important step in silicon implementation. Many circuits such as switched-capacitor and switched-current are analog circuits but digital circuits control them. Recently, analog and digital circuits have been fabricated on the same chip, resulting in a mixed-analog-digital IC chip. The mix of analog and digital generates several problems for circuit designers.

This chapter includes a short brief about the obstacles concerning the layout of mixed analog-digital chips. Layout guidelines are described to reduce coupling between the analog and digital parts. A short paragraph about CAD tools is written. Finally, a description of the layout of some circuits designed during the preparation of this work together with experimental results is presented.

6.2 CONSIDERATIONS ON LAYOUT FOR ANALOG CIRCUITS

Generally, analog integrated circuits suffer from mismatch between circuit elements. Also, any noise coupled to the analog circuit will be processed like an input signal. Mismatch is caused by process variation such as the non-uniform temperature distribution in furnace during wafer processing. All process parameters, for example oxide thickness or doping implant diffusion are dependent of temperature. Moreover, there are other error sources during the photolithography processing and etching. All these errors cause the performance of the integrated circuit to differ from the ideal one.

For example, the offset of op-amps, an important parameter for analog circuit design, must be as low as possible. The offset voltage has two components, the random offset and the systematic offset. The first one is caused by random mismatch while the second one is caused by asymmetry in circuit configuration. The circuit layout must try to minimize the effects of mismatch by using common centroid layout or trimming techniques [61]. To improve matching, several layout design guidelines have been collected in [63-chpt. 6, 64-chpt. 16].

One of the analog layouts for CMOS cells is the stacked layout method [64, 65]. In this method, the large W/L ratio of the designed transistor is implemented as n elementary transistors connected in parallel, as shown in Fig. 6.1 (c).

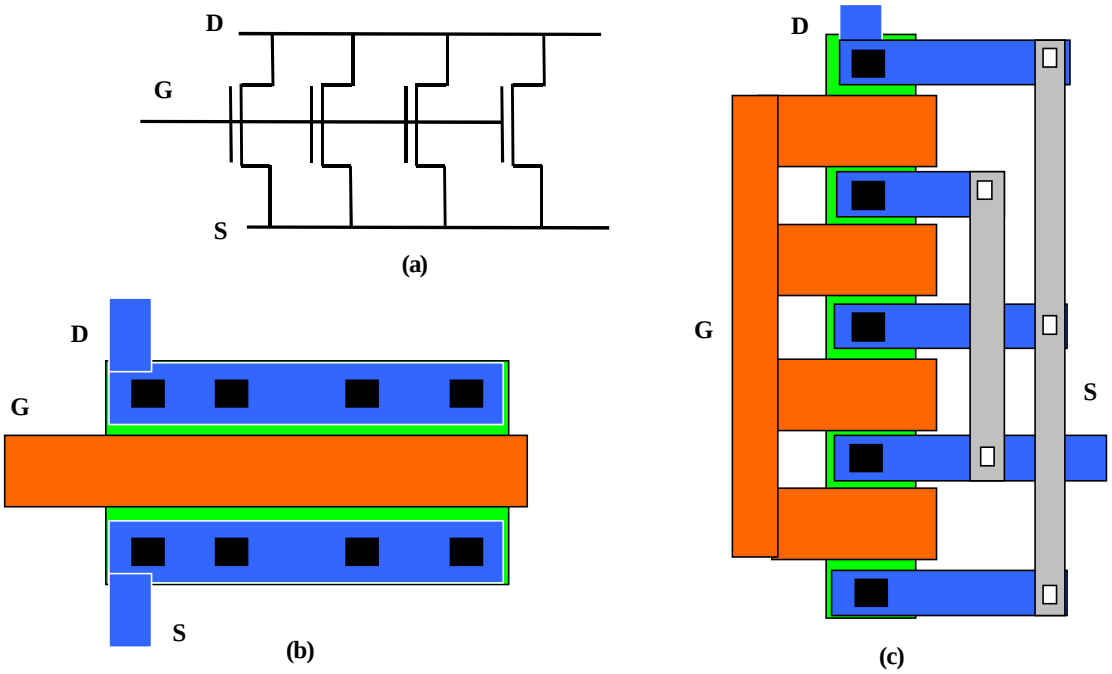

Fig. 6.1. Different layouts for wide MOS transistors.

(a) Transistor schematic.

(b) Layout of a single MOST.

(c) Layout using stack method.

The source and the drain of two-adjacent transistors are overlapped; thus, the overall area is smaller and the parasitic capacitor C_{sb} and C_{db} are reduced by the same factors, which is quite important for high-speed applications. With shrinking process geometry ($L<2\mu m$), boundary effects are becoming more important due to fringing or anisotropic photo-lithographic processing. Dummy elements have been used to match boundary effects [65].

6.3 CONSIDERATIONS ON LAYOUT FOR MIXED ANALOG-DIGITAL CHIPS

In addition to mismatch, mixed analog-digital IC chips suffer from noise coupling (cross-talk) between analog and digital circuits. For example, in the circulating SI analog FIR filter presented here, the digital control circuit that rotates the FIR coefficients generates digital switching noise that can degrade the performance of the filter. As regards layout, the most obvious solution to avoid digital noise to interact with the analog section is a reasonable distance between the digital and analog parts of the chip. An appropriate floor plan for mixed chips is shown in Fig. 6.2. In the mixed chip, there are different ways for the noise to be coupled between the chip parts (analog and digital). The most significant part of the noise is coupled through the common power supply line and into the substrate. Also the noise can be coupled into the signal lines. Some important guidelines that were utilized in our design to reduce noise coupling, are

1- Separate routing for analog and digital power supply (digital and analog power supplies are separated and tied only at a common pad).

2- Guard rings around digital part have been designed (n-well guard ring connected to V_{DD} and P^+ ring connected to V_{SS}).

3- The sensitive circuit parts such as capacitors are shielded.

4- Bottom-plates of the capacitors are connected to op-amp outputs.

More details about layout guidelines can be found in [62-chpt.6, 63-chpt.16]

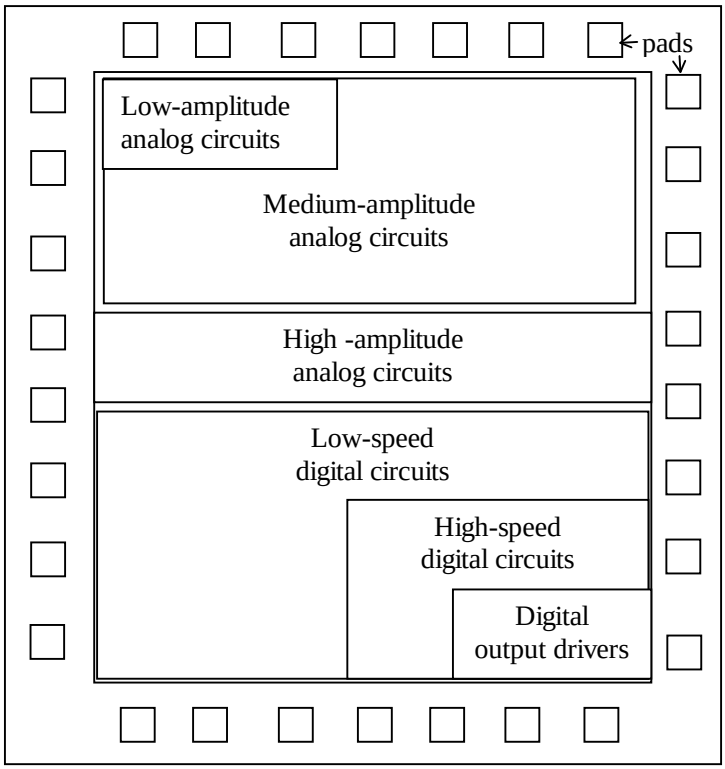

Fig. 6.2. General floor plan for mixed analog-digital chip [62-chpt. 6].

6.4 CAD TOOLS[1]

We used the TANNER TOOLS package [49] to assist us in designing the integrated circuits. The Tanner tools system consists of simulation, front-end and netlist, and mask-level simulation.

The simulation part includes an analog/digital simulator (T-Spice), a gate-level simulator, a waveform viewer (W-Edit) and a 3-D finite element thermal analyzer (L-Edit/Therm).

The front-end and netlist tools include a schematic editor (S-Edit) which can generate netlists for use with the gate-level simulator, T-Spice, and L-Edit/SPR (place and route tool). Another existing tool is the layout-versus-schematic (LVS). This program allows comparing an exported netlist from S-edit and an extracted netlist from L-Edit/Extract, or any two Spice file – compatible netlists.

The mask-level tool consists of a layout editor (L-Edit). L-Edit is a graphical mask layout editor. The program includes a unique cross-section viewer that allows the user to simulate grow/deposit, implant/diffusion and etch steps. In addition, the mask-level tool includes an automatic standard cell placement and routing package (L-Edit/SPR), which allows one to generate layouts for standard cells and automatically construct entire chips. The program accepts the netlists of S-Edit and creates masks ready for fabrication.

L-Edit/Extract generates Spice-compatible circuits netlists from the mask-level layout. It can recognize active, passive devices files and most common device parameters. The extracted file can be easily simulated by T-Spice and the layout-versus-schematic can be readily checked.

Finally, the package includes a design rule check (DRC) routine that can test the designed layout file according to the technology rules. The program allows checking minimum width, exact width, minimum space between the layers, overlap, surroundings, etc. The DRC can handle full chip or part of it.

The program supports three output formats. The program can handle Tanner Database (TDB), Caltech intermediate form (CIF) and GDS II format files.

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[1] Some parts of this section have been transcribed from the user manual of the Tanner tools.

6.5 LAYOUT OF THE SINGLE-ENDED 4-TAP FIR FILTER

The 4-tap switched-current filter designed in chapter 5 has been laid out using L-Edit. The stacked layout technique [64, 65] has been used for the analog circuits. The digital circuit has been designed using standard cells of AMS. Layout guidelines have been taken into account to minimize the coupling between sections. The common centroid technique has been applied in the analog circuit to reduce mismatch effects, especially in differential pairs of op-amps, as shown in Fig. 6.3.

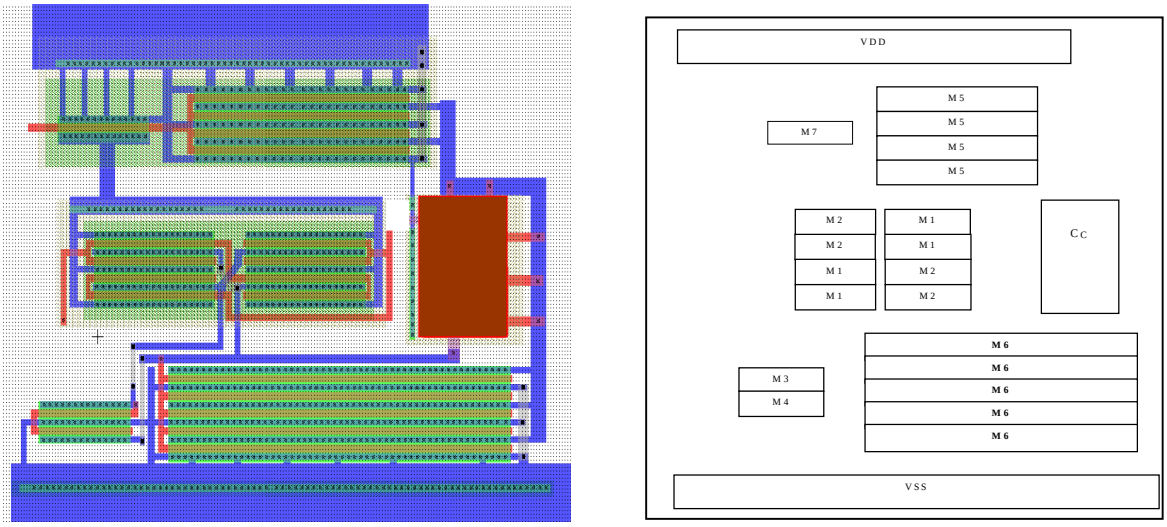


Fig 6.3. Op-amp layout (see schematic in Fig. B.1).

The complete layout of the test chip is illustrated in Fig. 6.4. (a). In this figure, h_1, h_2, h_3, and h_4 are 6-bit digital words for the MOCDs that perform as the FIR filter coefficients. Fig. 6.4. (b) exhibits the floor plan of the chip. The circuit occupies $4mm^2$ die area with pads. The chip has been designed and fabricated in the 0.8μm CMOS technology from AMS.

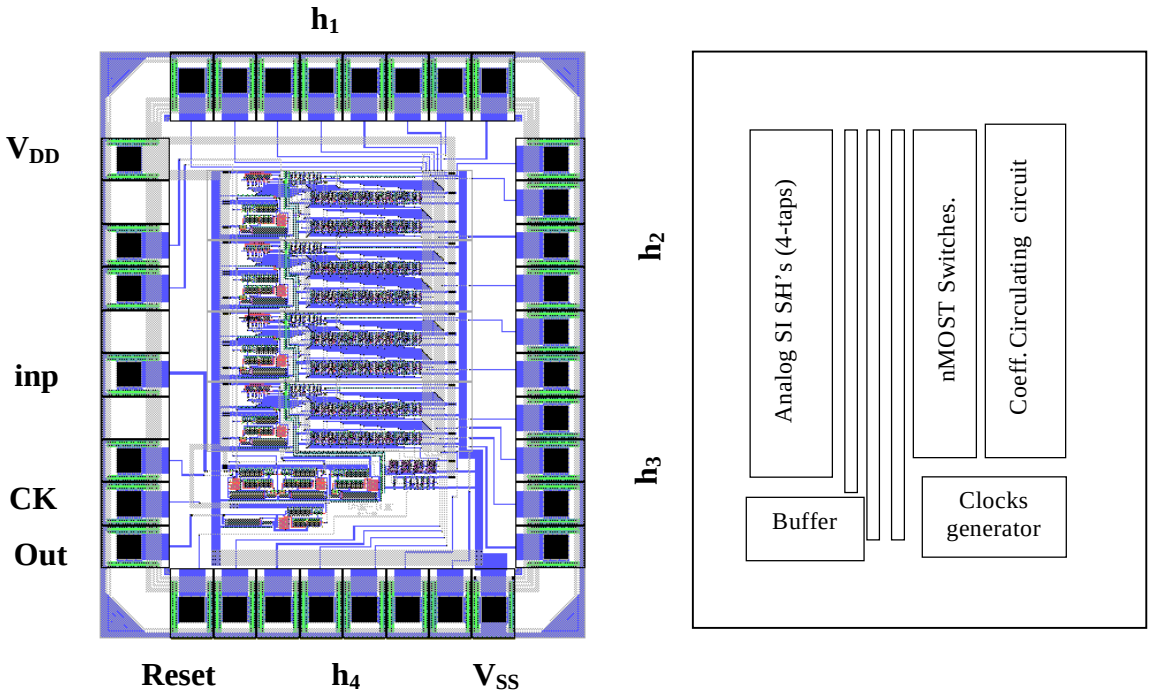


Fig. 6.4. The layout of the single-ended 4-tap FIR filter.

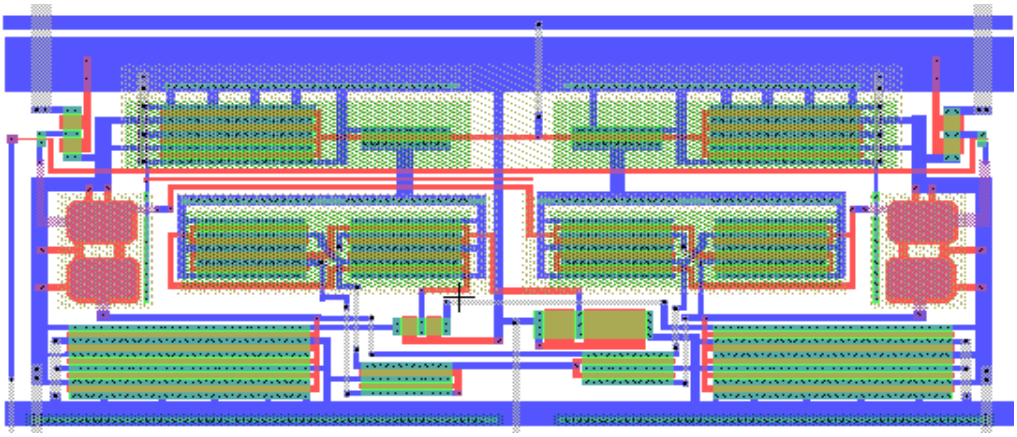
(a) Chip layout.

(b) Floor plan.

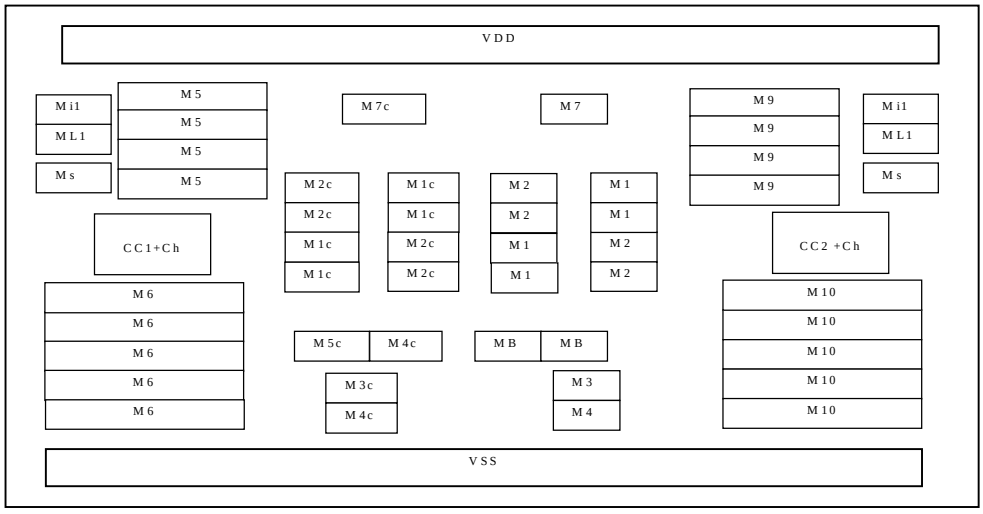
6.6 LAYOUT OF THE FULLY BALANCED SAMPLE-HOLD

The layout of the fully balanced S/H is shown in Fig. 6.5. The layout of the test chip is shown in Fig. 6.6 (a). The total area is 3.5mm^2 including the pads. The test chip includes a complete programmable tap (V-I converter, full programmable SI S/H and I-V converter sections), fully balanced differential op-amp and single-ended to balanced-output converter section. The digital part [1] includes one shift register to load the digital word in serial form. The circuit has been sent to fabricate in the 0.8μm CMOS technology from AMS. The floor plan of the test chip is shown in Fig. 6.6 (b).

[1] This part of the circuit has been designed by undergraduate student William Prodanov.



(a)



(b)

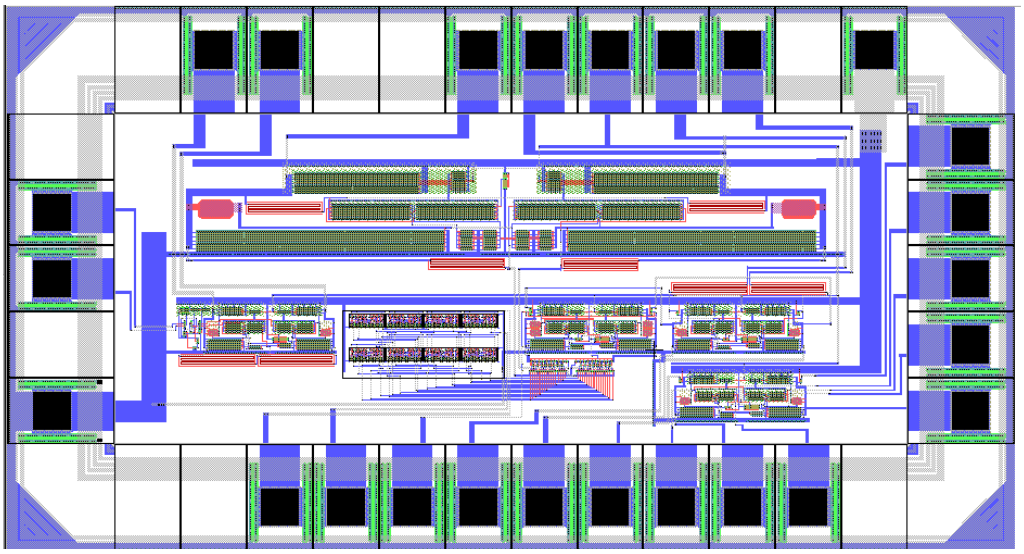
Fig.6.5. Layout of the fully balanced sample-hold and transistor placement.

(a) Layout of the fully balanced S/H.

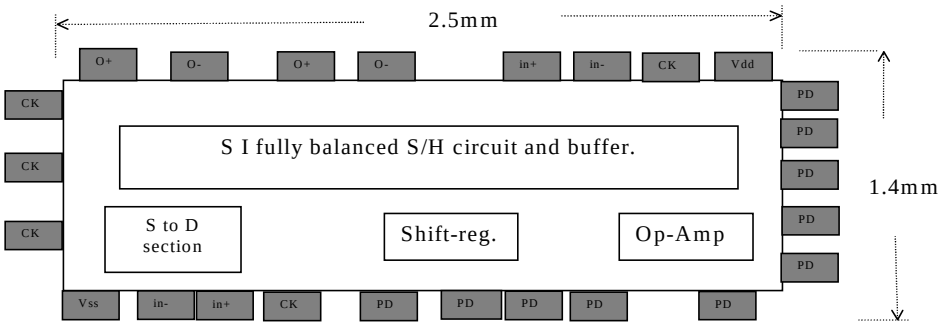
(b) Transistor placement.

6.7 CHIP TESTING AND MEASUREMENTS

A 4-tap switched-current FIR filter was fabricated in the double-poly double-metal 0.8µm CMOS process from AMS. A micrograph of the integrated filter is shown in Fig. 6.7. The entire chip measures 4.0mm^2. Fig. 6.8 shows some details about the single-ended SI S/H circuit.



(a)



(b)

Fig. 6.6. The fully balanced test chip.

(a) Layout of the fully balanced test chip.

(b) Floor plan.

The frequency response has been measured using the 3588A spectrum analyzer. The measured results for different digital words are depicted in Fig. 6.9. The figure shows good agreement between each of the theory, simulation and the experimental results. The time response of the circuit shown in Fig. 6.10 has been obtained for a programmed 4-clock cycle delay.

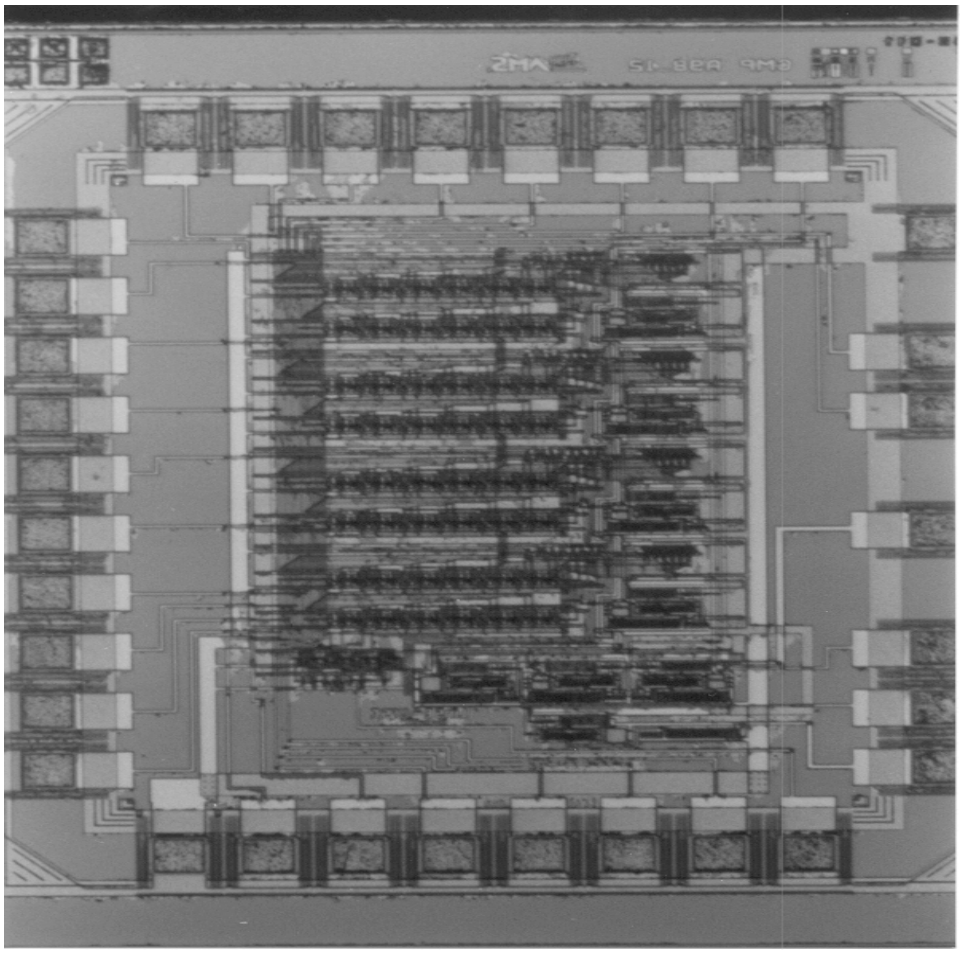


Fig. 6.7 The single-ended 4-tap FIR filter chip micrograph.

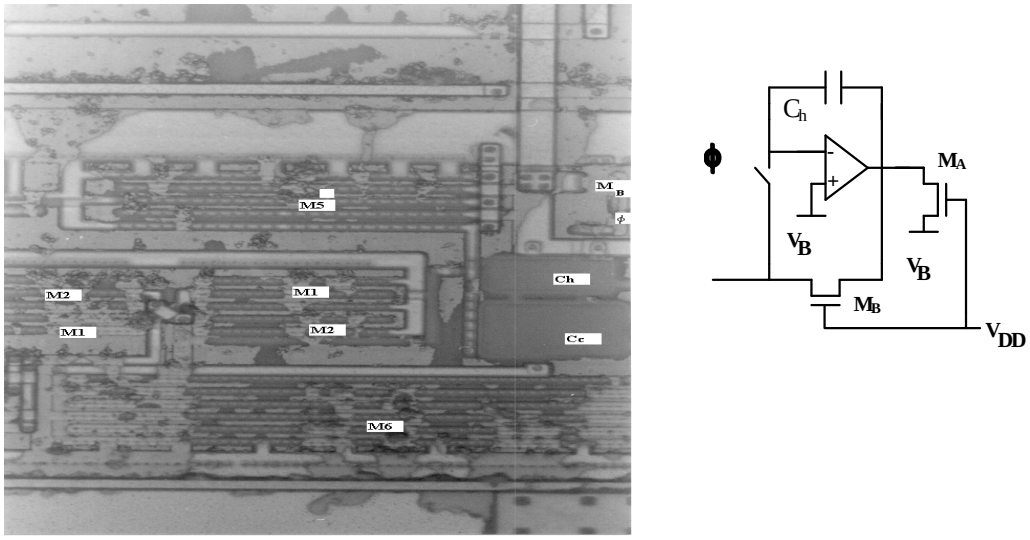
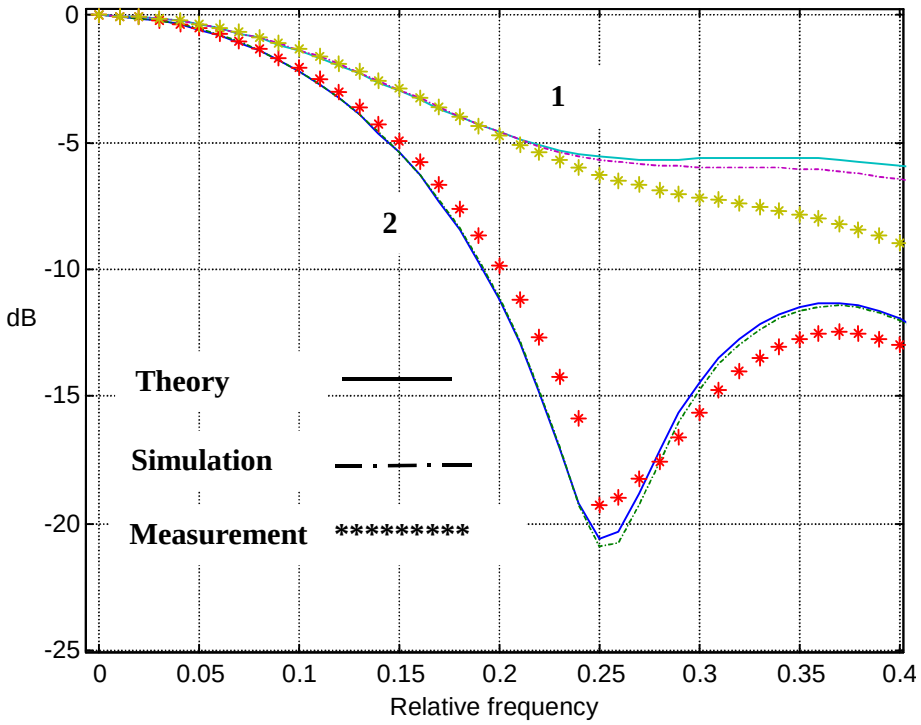


Fig. 6.8 The switched-current S/H.

Obs: M_1, M_2, M_5, M_6 and C_c are the op-amp elements (Fig. B.1).



1 h_1 *=3F ,* h_2 *=15,* h_3 *=0B and* h_4 *=06.*

2 h_1 *=3F ,* h_2 *=36,* h_3 *=2E and* h_4 *=27.*

Fig. 6.9. Measured, simulated and theoretical frequency response of the 4-tap FIR filter.

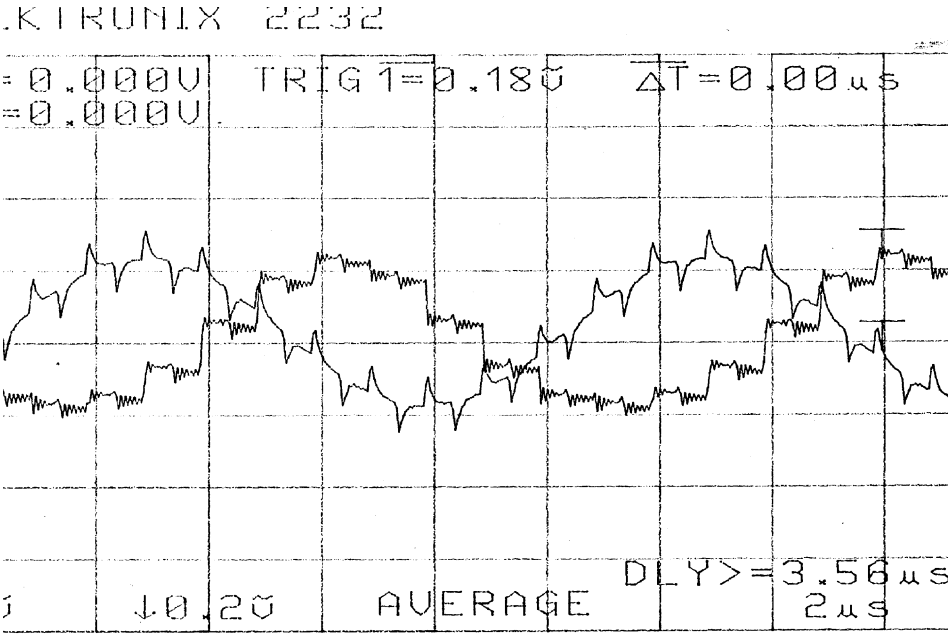


Fig. 6.10. Pure delay measurement.