CHAPTER 5

CIRCULATING FINITE IMPULSE RESPONSE (FIR) FILTER -ARCHITECTURE AND IMPLEMENTATION

5.1 INTRODUCTION

The limited bandwidth of communication channels and multi-path reflections cause inter-symbol interference (ISI). The ISI limits the density of many storage systems and the speed of many communication systems. A finite impulse response (FIR) filter can be used to implement the inverse transfer function of the channel and thus equalize the frequency response. The input-output relationship of an FIR filter is given by

$$y(n) = \sum_{k=0}^{N-1} h_k x(n-k) \tag{5.1}$$

Analog tapped-delay line has been used for the FIR filter realization [54] as shown in Fig. 5.1. As shown in this figure, the signal is delayed with added transition errors (sampling errors) which are known as multiple re-sampling errors. A significant increase in the FIR performance can be gained if the system design avoids the re-sampling errors of the traditional analog delay line. For this purpose, the circulating technique [55] for FIR filter realization has been proposed.

5.2 APPLICATIONS

The Decision Feedback Equalizer (DFE) has been used for ISI cancellation thus increasing the speed of data transmission [56] and the storage capability [57, 58, 59].

Generally, the two main components of the DFE are a forward equalizer and a feedback equalizer that eliminate the ISI before and after each symbol, respectively.

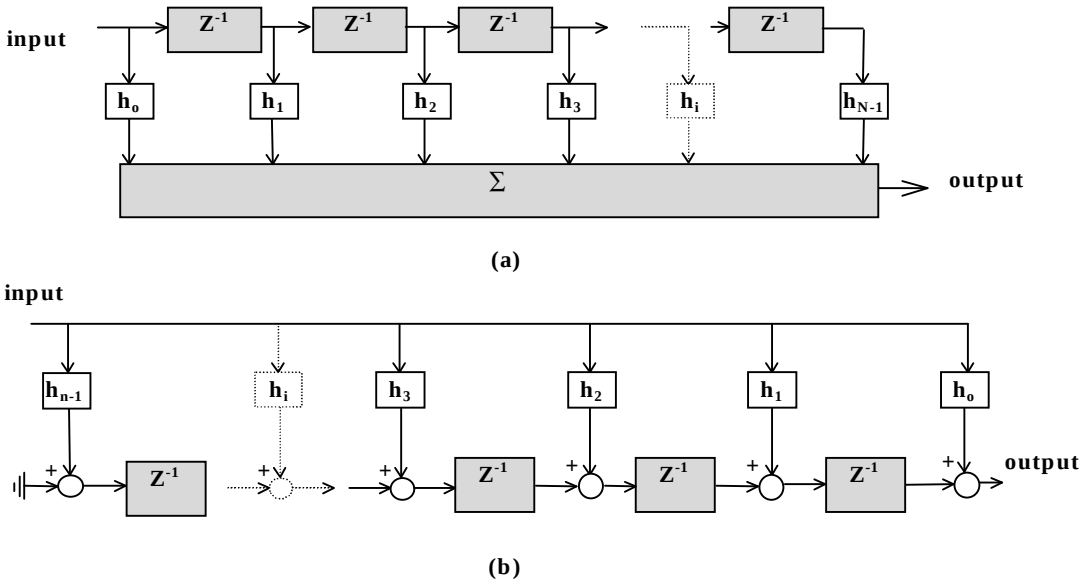


Fig. 5.1. Realization forms of the analog delay line.

(a) Direct-form realization.

(b) Transposed form realization.

Modern magnetic storage channels, which usually use the partial response maximum likelihood (PRML) detection method, require an adaptive equalizer for the reduction of ISI [57, 58, 59]. Also, for time-variant channel characteristic (such as mobile wireless communication), the adaptive DFE is necessary to compensate the channel variation. The general block diagram of the adaptive DFE is shown in Fig. 5.2. The forward and backward equalizers are realized using fully programmable FIR filters. In this work, we introduce a fully balanced programmable FIR filter suitable for read channel disk-drive and for mobile wireless communications applications at low supply voltage.

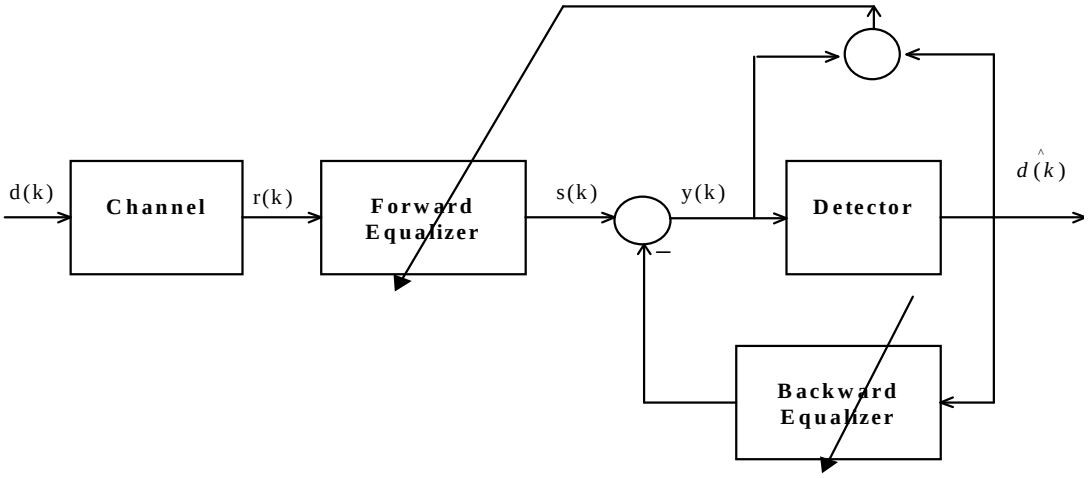
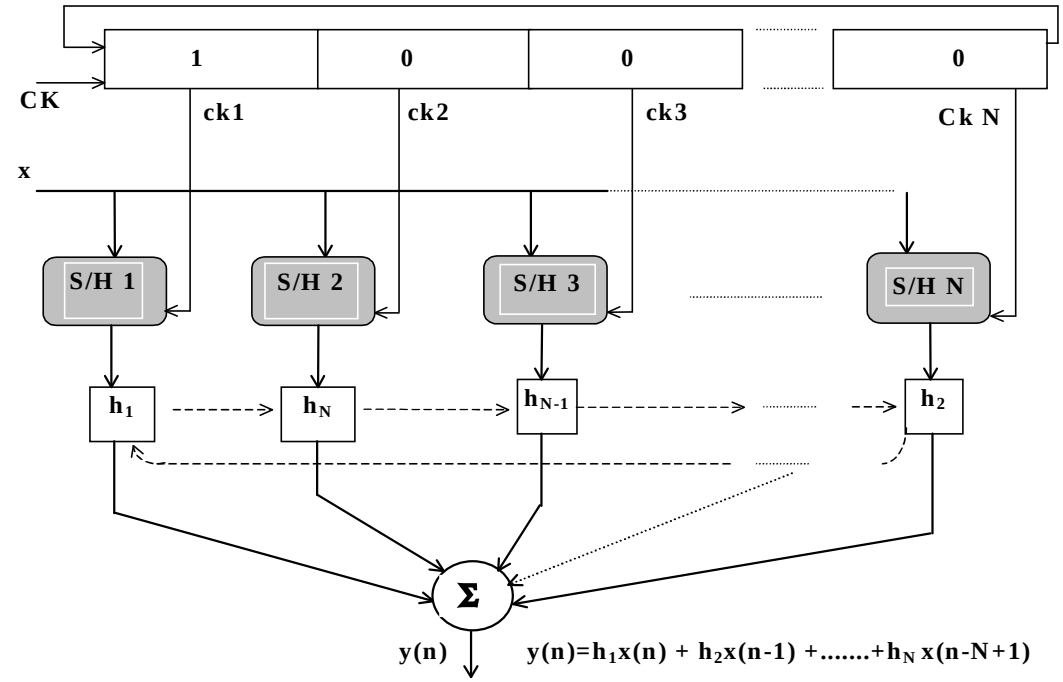


Fig. 5.2. Block diagram of an adaptive DF equalizer.

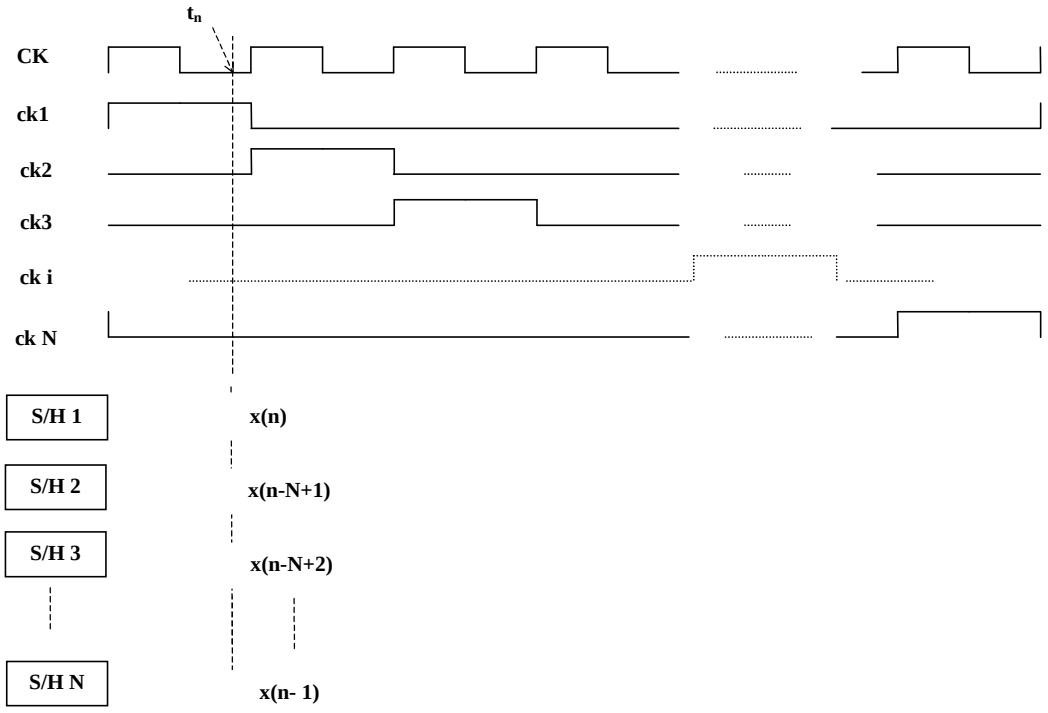
5.3 CIRCULATING FORM OF THE FIR FILTER

The circulating form of the FIR filter is shown in Fig. 5.3.(a). Each S/H samples the input signal only once every N clock cycles and holds the signal value for the remaining N-1 cycles. To simulate the analog delay line, h_1 is always associated with the most recent sample (denoted as zero time reference), h_2 associates with S/H that has been sampled at -T from the reference time, h_3 with the S/H that has been sampled at –2T and so on. So, the coefficients of the FIR filter must rotate one position for each clock phase as shown in Fig. 5.3.(a). The clock phases are illustrated in Fig. 5.3.(b).

The circulating technique simulates a tapped delay line without passing the sampled value into series delay taps on each clock cycle. Consequently, this structure has the advantage of avoiding the propagation of the re-sampling errors from each cell to the following. Table 5.1 illustrates the details of the signal and the distribution of coefficients for the first N clock cycles [51]. Moreover, Table 5.2 shows the signal and coefficients after the first N clock cycles. Also Tables 5.1 and 5.2 show the static property of the stored signal in S/H's and the dynamic property of the FIR coefficients.



(a)



(b)

Fig.5.3. General schematic of an N-tap FIR filter.

(a) Circular FIR filter structure (coefficients during ck1).

(b) The control clocks and the currents of the S/H's at t_n.

Table 5.1. Stored signals and distribution of coefficients through the first N clock cycles.

Time	S/H 1		S/H 2		S/H 3		.....	S/H N		O/p
	Data	**Coef.**	**Data**	**Coef**	**Data**	**Coef.**	**.....**	**Data**	**Coef.**	
0T (ck1)	x_0	h_1	-----	-----	---	------	.....	-------	-------	y_0
1T (ck2)	x_0	h_2	x_1	h_1	----	------	.....	-------	-------	y_1
2T (ck3)	x_0	h_3	x_1	h_2	x_2	h_1	.....	-------	-------	y_2
3T (ck4)	x_0	h_4	x_1	h_3	x_2	h_2	.....	-------	-------	y_3
.....	x_0	....	x_1	h_4	x_2	h_3	.....	-------	-------	.....
.....	x_0	..	x_1	....	x_2	h_4	.....	-------	-------	.....
.....	x_0	....	x_1	..	x_2	....	.....	-------	-------	.....
(N-1)T (ck N)	x_0	h_N	x_1	h_{N-1}	x_2	h_{N-2}	.....	x_{N-1}	h_1	y_{N-1}

Table 5.2. Stored signals and distribution of coefficients after the first N clock cycles.

Time	S/H_1		S/H_2		S/H_3		.....	S/H_N		O/P
	Data	**Coef**	**Data**	**Coef**	**Data**	**Coef**	**.....**	**Data**	**Coef.**	
NT (ck1)	$\underline{\mathbf{x_N}}$	$\underline{\mathbf{h_1}}$	$\mathbf{x_1}$	$\mathbf{h_N}$	$\mathbf{x_2}$	$\mathbf{h_{N-1}}$	.....	$\mathbf{x_{N-1}}$	$\mathbf{h_2}$	$\mathbf{y_N}$
(N+1)T (ck2)	x_N	h_2	$\underline{x_{N+1}}$	$\underline{h_1}$	x_2	h_N	.....	x_{N-1}	h_3	y_{N+1}
(N+2)T (ck3)	x_N	h_3	x_{N+1}	h_2	$\underline{x_{N+2}}$	$\underline{h_1}$	.....	x_{N-1}	h_4	y_{N+2}
(N+3)T (ck4)	x_N	h_4	x_{N+1}	h_3	x_{N+2}	h_2	.	x_{N-1}	h_5	y_{N+3}
.....	x_N	....	x_{N+1}	h_4	x_{N+2}	h_3	.....	x_{N-1}	.....	.....
.....	x_N	..	x_{N+1}	....	.....	h_4	.....	x_{N-1}	.....	.....
	x_N	....	x_{N+1}	..	.....	....	.....	x_{N-1}	.....	.....
(2N-1)T (ckN)	x_N	h_N	x_{N+1}	h_{N-1}	x_{N+2}	h_{N-2}	.....	$\underline{x_{2N-1}}$	$\underline{h_1}$	y_{2N-1}

5.4 DIGITAL CONTROL CIRCUITS

As previously shown, the FIR coefficients must rotate one position after each clock cycle. The rotating switch matrix [60] was used to achieve this function. In this work, the FIR filter coefficients are controlled by the MOCD and the rotating switch matrix is simulated by rotating the control digital words <bi> of the MOCDs. The circulating process can be achieved using combinational or sequential logic circuit. Firstly we used the combinational logic circuit to circulate the coefficients. Fig. 5.4 shows the one-bit circulating circuit. Thus, for each M-bit MOCD, M blocks must be used to circulate the coefficients.

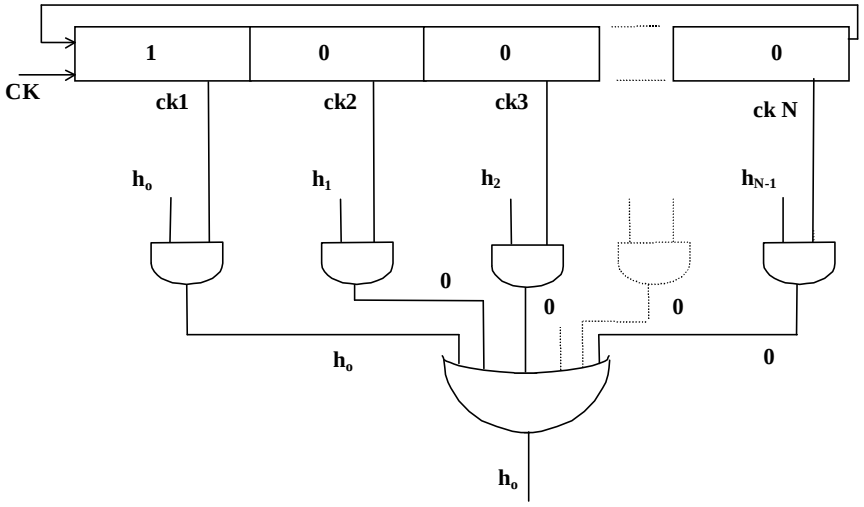
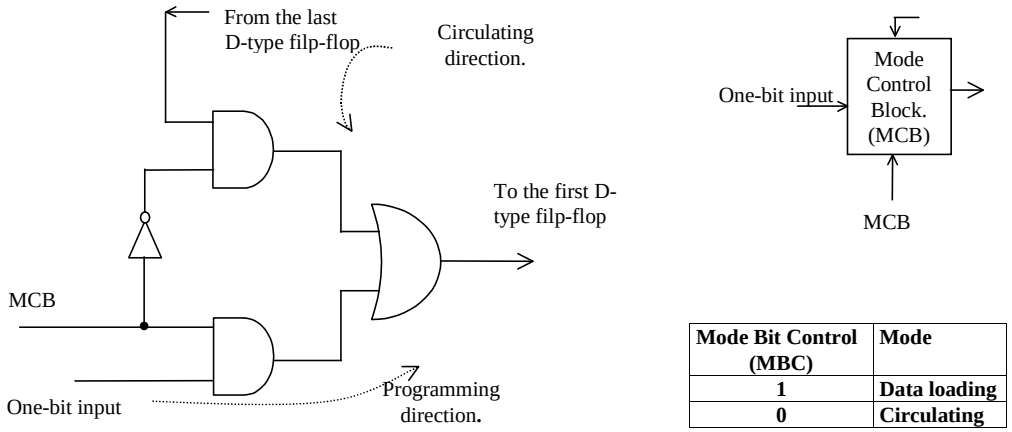


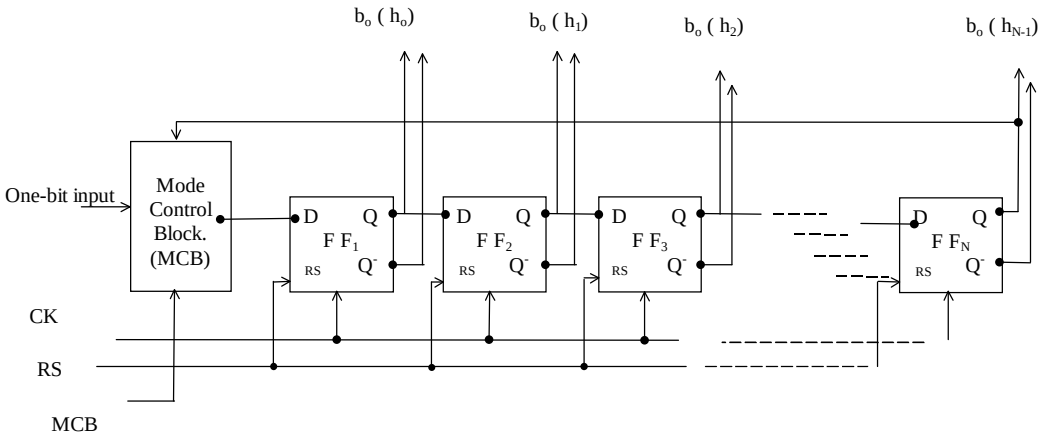
Fig. 5.4. The schematic of the one-bit circulating circuit.

The shifting process of the FIR filter coefficients can be achieved using shift registers. To reduce the total number of pads, the shift register has been used to load the data serially. So another circuit is necessary to select the operating mode, loading (programming) or circulating, as shown in Fig. 5.5.(a). The complete one-bit circulating block is depicted in Fig.5.5.(b). Also, the clock phases (ck1, ck2,.....ckN) are generated by using cascaded D-type flip- flops as shown in Fig. 5.6. The RS terminal is necessary to set the initial word to 100000.... and then circulate it.



Mode Bit Control (MBC)	Mode
1	Data loading
0	Circulating

(a)



(b)

Fig. 5.5. The sequential control circuit.

(a) The mode control block.

(b) One-bit circulating block (b_o).

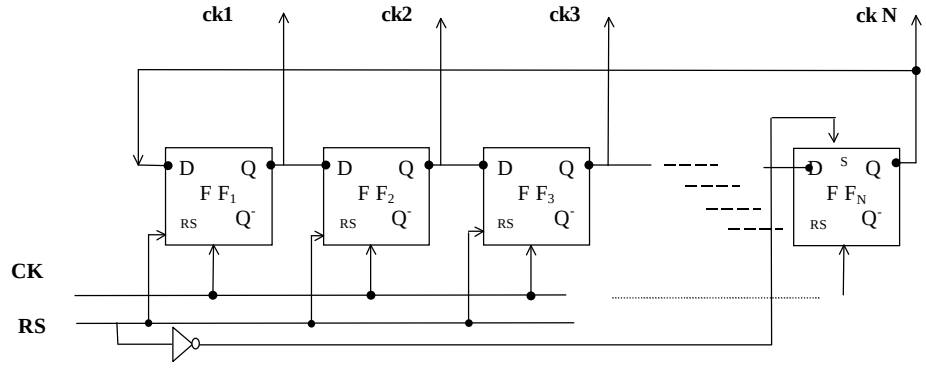


Fig. 5.6. Clock generator.

5.5 SWITCHED-CURRENT REALIZATION OF THE CIRCULATING FIR FILTER

In this section, we present the design of two FIR filters. A 4-tap single-ended FIR filter and a fully balanced 8-tap filter are presented. They can be used for time recovery [56] and disk drive applications, respectively.

5.5.1 SINGLE-ENDED 4-TAP SWITCHED-CURRENT FIR FILTER

The S/H circuit and the programmable MOCD has been used for the SI implementation of a 4-tap circular FIR filter as shown in Fig. 5.7.(a). The front-end section is a linear voltage-to-current converter. After the V-I conversion, the signal is fed to the S/H's according to the timing diagram shown in Fig. 5.7.b. The stored signals, multiplied by their corresponding coefficients, are summed in the output section, which is a linear current-to-voltage converter.

In practice, an internal MOCD operates as a (large area) switch (M_{3L} Fig. 5.8). Thus, a significant amount of charge can be transferred to the holding capacitor due to both the channel charge and the capacitive coupling between gate and source. Fig. 5.8. (a) illustrates details about the switching methodology of the FIR filter structure shown in Fig. 5.7. (a), at clock cycle ck1. Generally, the injected charge due to the switch "S2" is minimized by using a CMOS transmission gate or a dummy transistor technique.

Here we propose a clock scheme to reduce the injected charge into the holding capacitor due to MOCD M_{3L}. The scheme is shown in Fig. 5.8. (b). Switch "S2" has to open before M_{3L} turns off to avoid the charge injected by M_{3L} to be stored into the holding capacitor. So, the MOCD clock (ck_{1s}) must be delayed with respect to ck1 as

shown in Fig. 5.8. (b). This delay time must be as short as possible in order to not increase the settling time error.

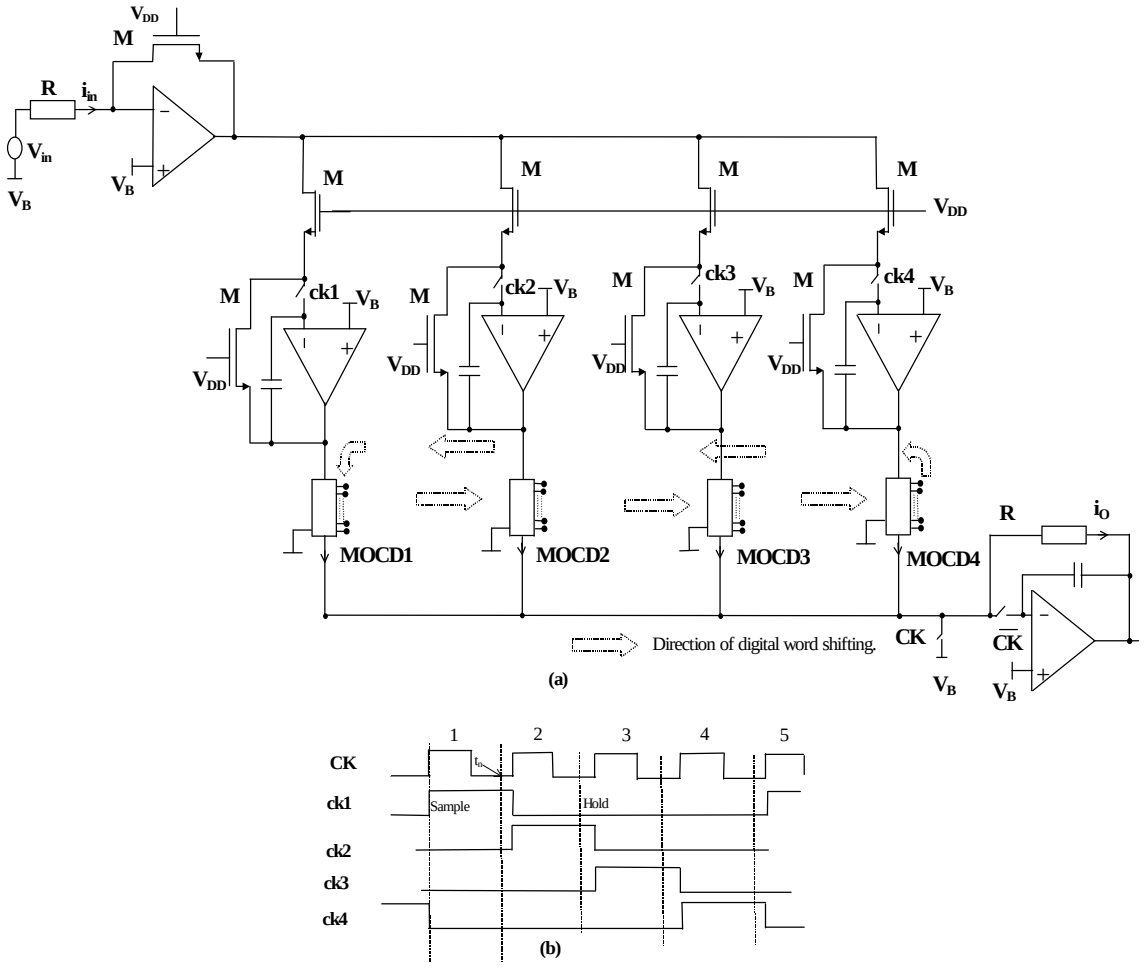


Fig. 5.7. The 4-tap FIR filter in circulating form.

(a) Scheme .

(b) Clock phases.

To validate our analysis, the circuit shown in Fig. 5.8. (a) has been simulated with SMASH [38] for a 10μA input current and using 3μm/0.8μm n-channel switches at 20MHz clock frequency. The ACM MOSFET model [22] has been used for the simulations. M and M_{3L} have aspect ratios equal to 6μm/5μm and the holding capacitor is 0.5 pF. The two-stage CMOS op-amp designed in Appendix B has been used in the simulation. The delay time between the main clock (ck1) and the delayed one ($ck1_s$)

was 0.4nsec, which is equivalent to two cascaded logic inverters from the AMS library of the 0.8μm double-poly double-metal CMOS technology. The circuit has been simulated using both the proposed clock and the conventional clock (without any delay) schemes. The simulation results are depicted in Fig. 5.9. The DC offset current (output-2) is due to the charge accumulation into the holding capacitor which disappears after using the proposed clock.

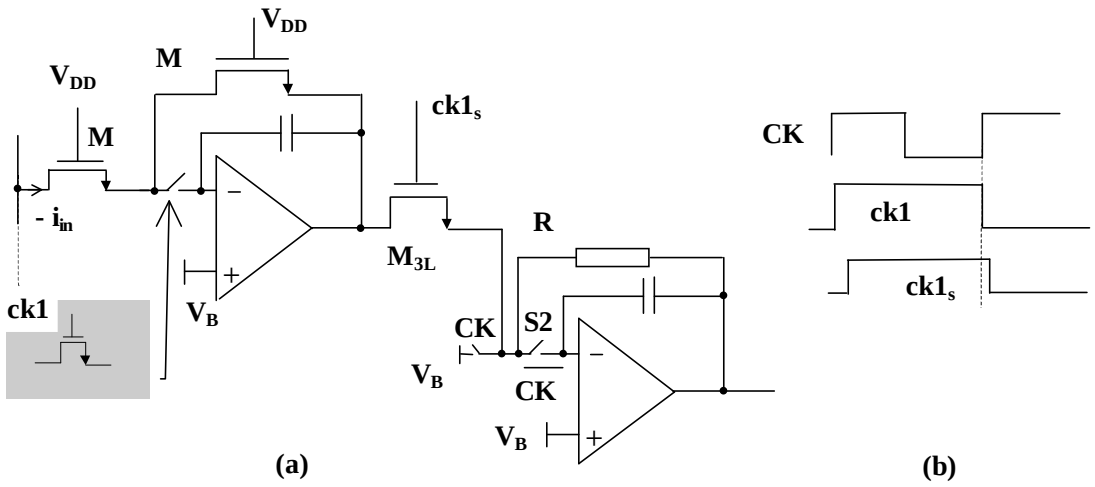


Fig. 5.8. Switching methodology to reduce charge injection.

(a) The basic S/H cell and the summer block.

(b) Proposed clock scheme.

Obs: M_{3L} is equivalent to an MOCD in Fig. 5.7. (a).

The 4-tap filter shown in Fig. 5.7.(a) has been designed and laid out using the Tanner Tools package [49]. L-edit has been used to extract the netlist for the full chip. The FIR filter coefficients have been set to h_1=00, h_2=00, h_3=00, and h_4=3F. These coefficients realize a pure 4-clock cycle delay. The output and input currents are illustrated in Fig. 5.10. The DC offset current and spikes have been suppressed using the clock scheme of Fig. 5.8. (b).

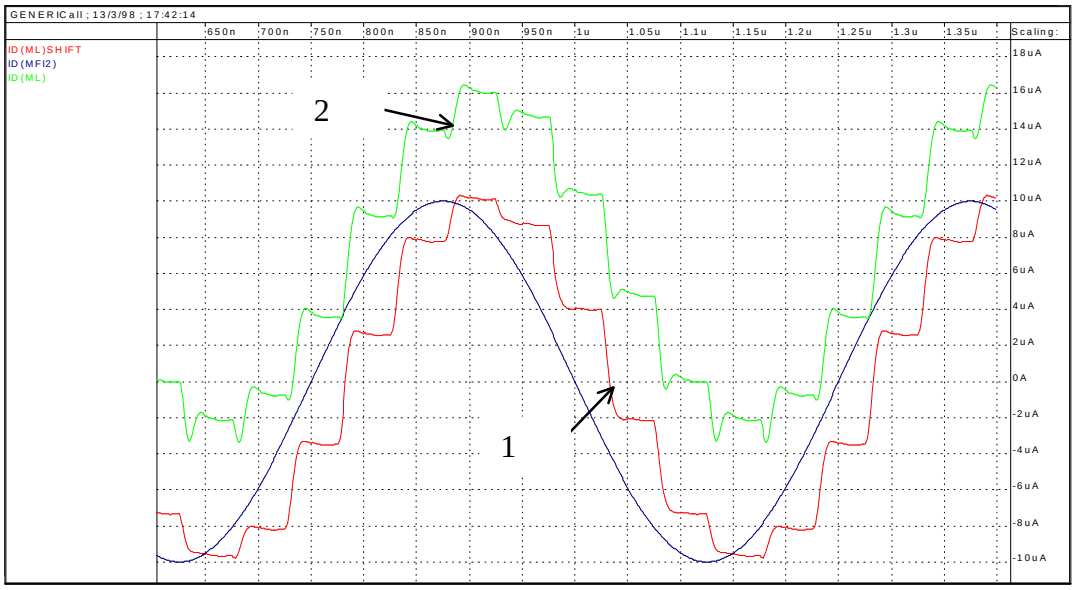


Fig. 5.9. Simulation results for the circuit of Fig. 5.8.

1- Proposed clock. 2- Conventional clock.

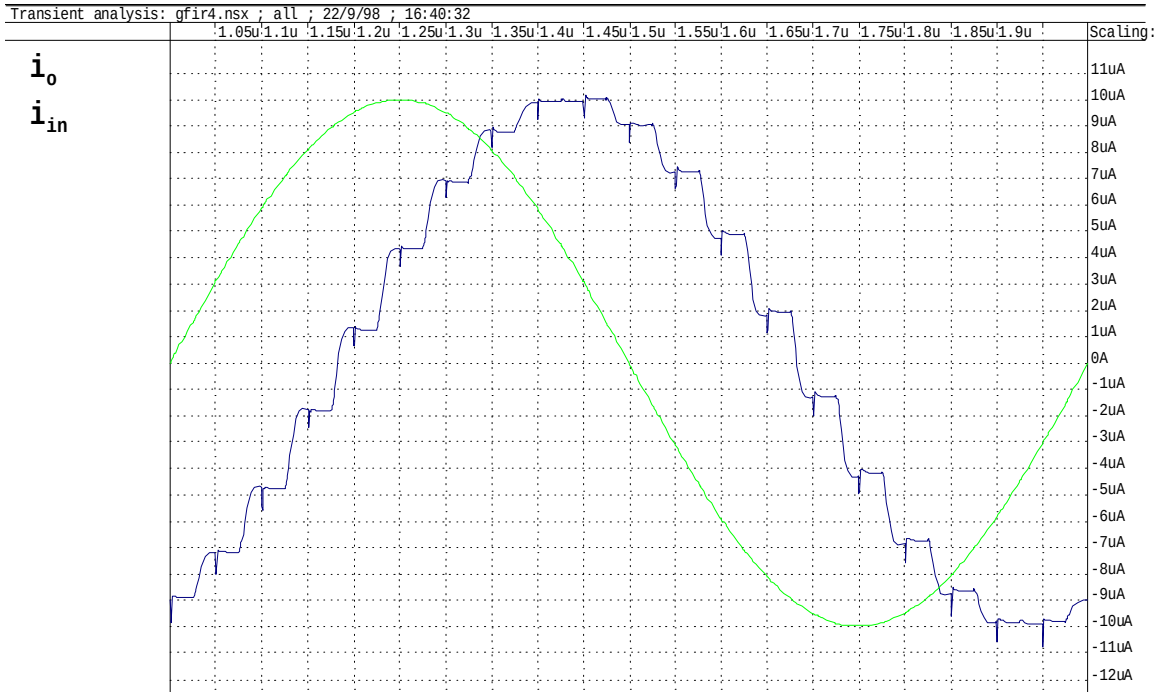
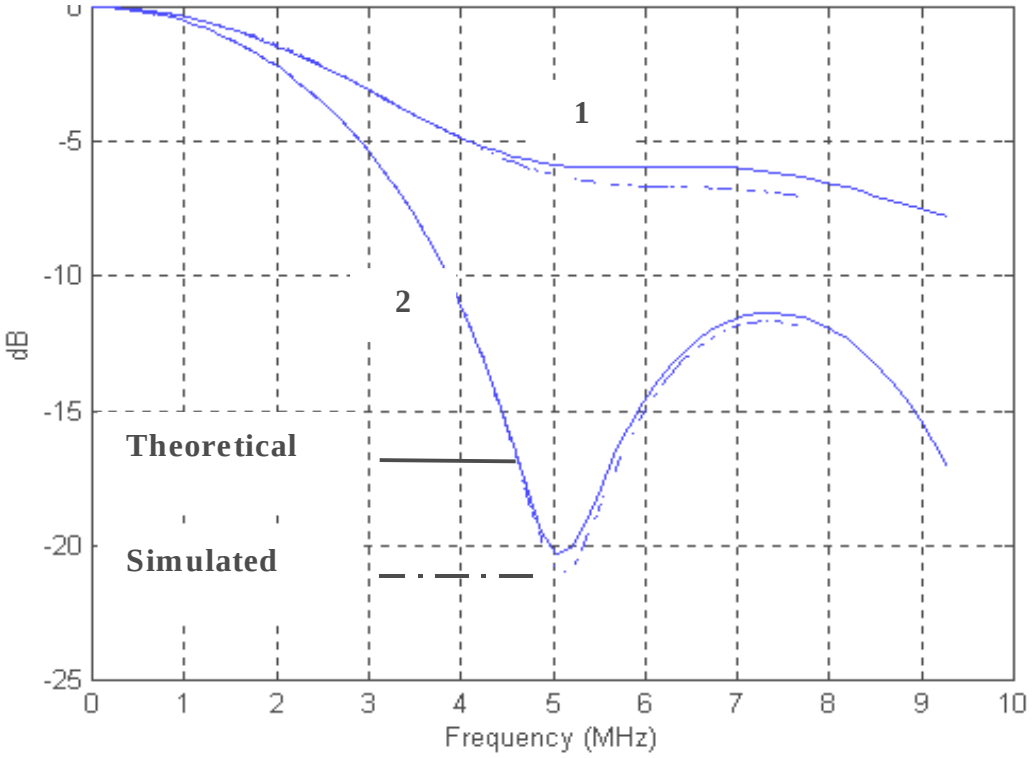


Fig. 5.10. Pure delay of 4 clock cycles (h_1=h_2 = h_3 =00 and h_4 =3F).

T-Spice [49] has been used to obtain the impulse response of the FIR filter for different coefficients (digital words). The MATLAB FFT routine has been used to obtain the frequency response. The theoretical curves have been obtained using the ideal

freqz-routine from the MATLAB package. Fig. 5.11 shows the programmability of the filter for different digital words.

In the SI circuit shown in Fig. 5.7. (a), the currents are continuously fed to all S/H's through the input transistors (M). Thus, for an N-tap FIR filter, the input amplifier (V-I converter circuit) must be able to drive (N+1) transistors.



$h_1 = 3F$, $h_2 = 15$, $h_3 = 0B$ *and* $h_4 = 06$ (curve 1).

$h_1 = 3F$, $h_2 = 36$, $h_3 = 2E$ *and* $h_4 = 27$ (curve 2).

Fig. 5.11. The magnitude response of the FIR filter for different digital words.

5.5.2 FULLY BALANCED FIR SWITCHED-CURRENT FILTER

Here we design a fully balanced programmable FIR filter using the circulating technique. An 8-tap FIR filter has been implemented using the fully balanced S/H circuit presented in chapter 4. The switched-current realization of the 8-tap FIR filter is depicted in Fig. 5.12. The figure shows tap number i which is clocked at phase cki.

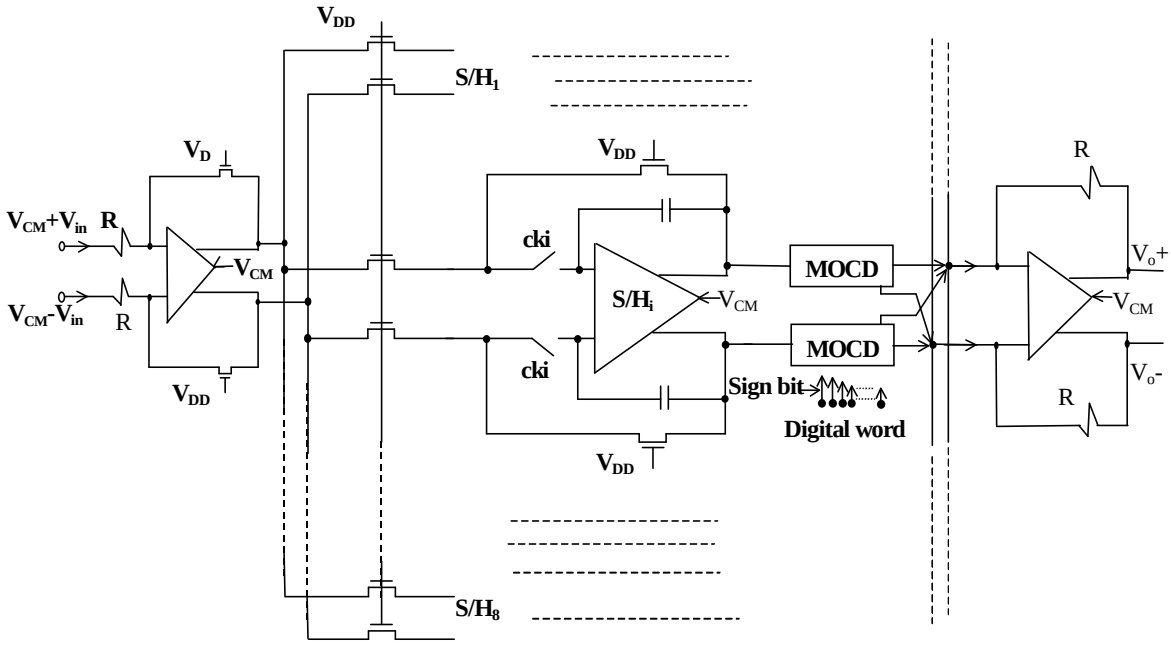


Fig. 5.12. 8-tap fully balanced switched-current FIR filter.

The programmability of the FIR filter has been tested for low-pass and bandpass filters. The filter coefficients have been determined using the Parks-McClellan optimal equiripple FIR filter design from the MATLB package. The coefficients and their equivalent digital words are shown in Table 5.3.

- **SIMULATION APPROXIMATION**

To simplify the overall switched-current circuit for the purpose of simulation, the fully balanced op-amp has been modeled as shown in Fig. 5.13. Each single-ended op-amp is modeled by an ideal voltage-controlled voltage source. Also, to obtain the impulse response, the coefficients have been circulated only through the first MOCD (S/H 1) while the other MOCD's words have been set to (10000000); particularly, the stored data in S/H2,.....and S/H8 are zero.

Table 5.3. The attenuation factors of the MOCDs for low- and bandpass FIR filters.

Coeffs. of low-pass Filter			**Coeffs. of bandpass filter-I**			**Coeffs. of bandpass filter-II**		
MATLAB	Digital word	SI*	MATLAB	Digital word	SI*	MATLAB	Digital word	SI*
-0.0698	1 0001000	-0.06	-0.0140	1 0000001	-0.0032	-0.0234	1 0000011	-0.02
0.1142	0 1110001	0.123	-0.2049	1 0011010	-0.200	-0.2031	1 0011010	-0.2
0.2233	0 1100011	0.232	-0.0134	1 0000001	-0.0032	-0.0234	1 0000011	-0.02
0.3254	0 1010110	0.335	0.2128	0 1100100	0.215	0.2187	0 1100100	0.2215
0.3254	0 1010110	0.335	0.2128	0 1100100	0.215	0.2187	0 1100100	0.2215
0.2233	0 1100011	0.232	-0.0134	1 0000001	-0.0032	-0.0234	1 0000011	-0.02
0.1142	0 1110001	0.123	-0.2049	1 0011010	-0.200	-0.2031	1 0011010	-0.2
-0.0698	1 0001000	-0.06	-0.0140	1 0000001	-0.0032	-0.0234	1 0000011	-0.02

* Coefficients of the FIR filters from the SI simulation.

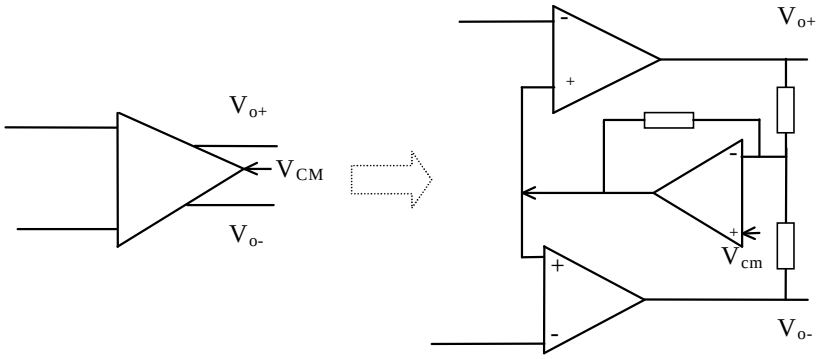


Fig. 5.13. A fully balanced op-amp and its simulated model.

The switched-current FB filter shown in Fig. 5.12 has been simulated to test the programmability for low-pass and bandpass filters. The simulation result (impulse response) has been used to obtain the filter frequency response using MATLAB FFT. Fig. 5.14 and Fig. 5.15 illustrate the ideal (MATLAB result) and simulated (SI filter response) frequency response of the low-pass and bandpass filters, respectively. The feedthrough error due to the internal switching of the MOCD's is canceled out due to the cross connection of the DUM and SUM terminals as shown in Fig 5.12. In Fig. 5.15,

the error between the theory (MATLAB) and simulated result is due to limited resolution of the MOCD (7'bit). This error is reduced as long as the maximum error between the real coefficients and its SI implementation to be minimum, as shown in Fig. 5.16.

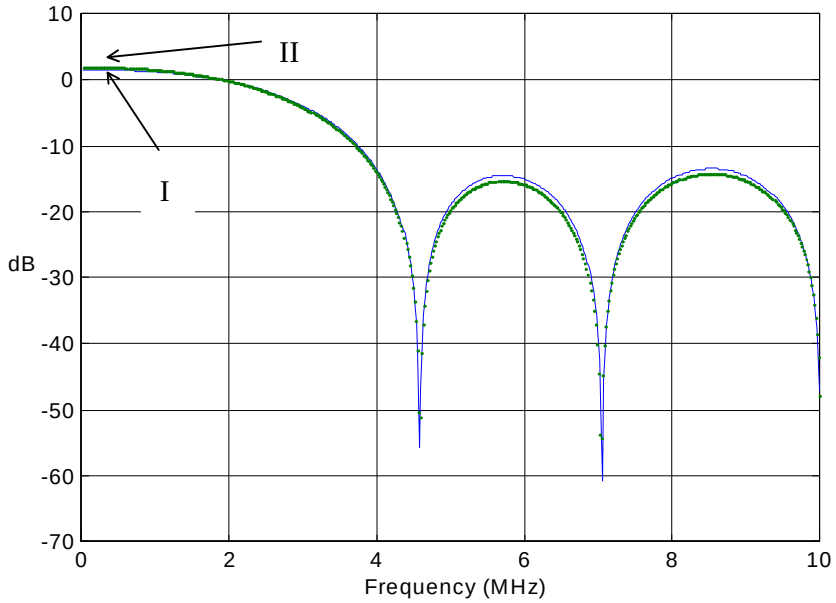


Fig. 5.14. The frequency response of the low-pass filter.
(I) theory and (II) Simulation.

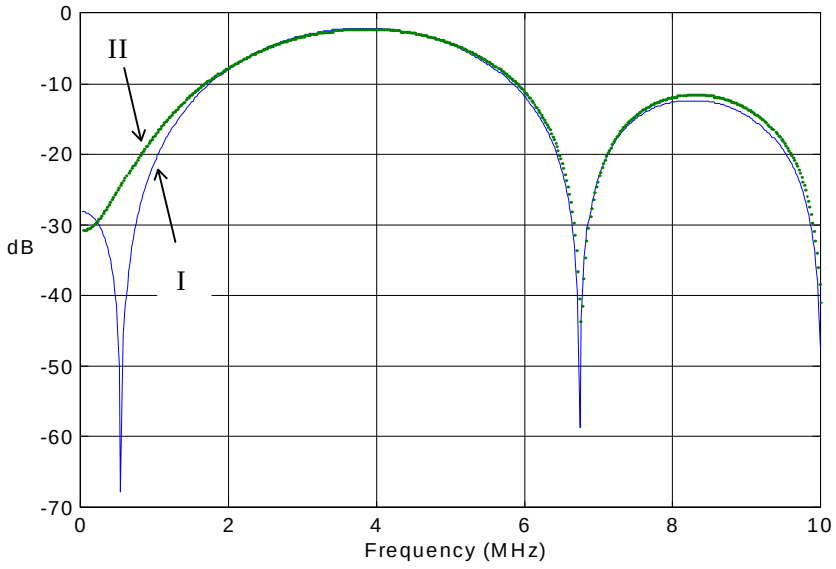


Fig. 5.15. The frequency response of the bandpass filter-I.
(I) Theory and (II) Simulation.

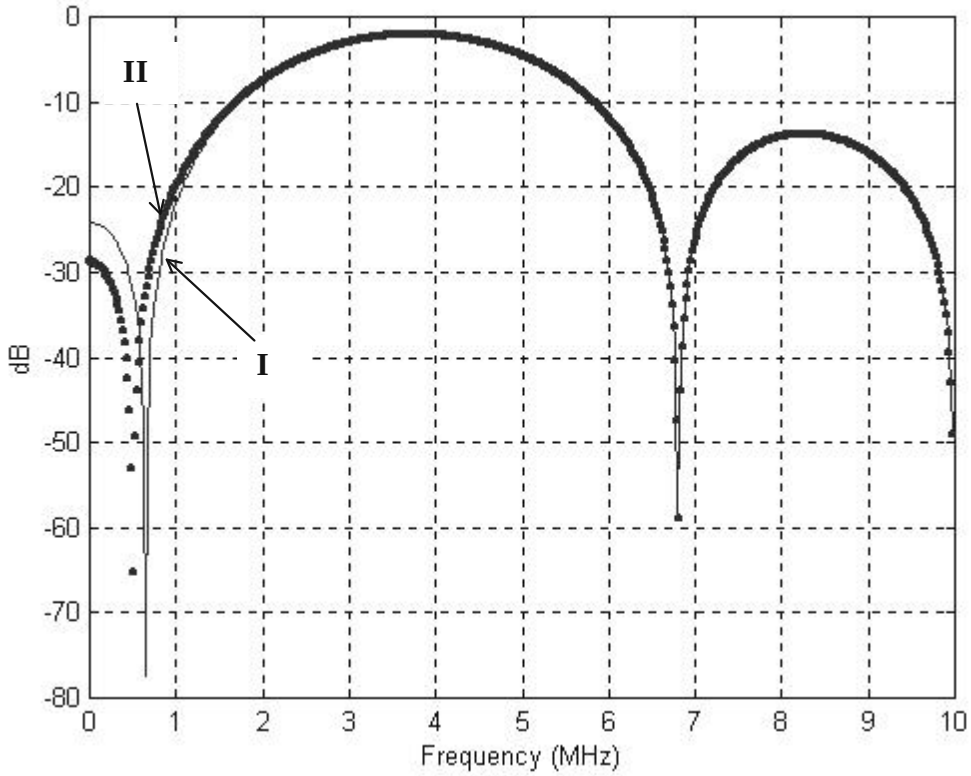


Fig. 5.16 The frequency response of the bandpass filter-II.

(I) Theory and (II) Simulation.