# CHAPTER 2

# SWITCHED-CURRENT TECHNIQUES AND LOW-VOLTAGE OPERATION

## 2.1 INTRODUCTION

Sampled-data circuits have been intensively employed in VLSI chips. The switched-capacitor (SC) technique has been the prevailing one over the last two decades. Using MOS amplifiers, switches, and precision linear capacitors, SC filters achieve high accuracy with low distortion. The basic building block of SC circuits is the sampled-data integrator in Fig. 1.4. (a).

In the late 1980s, a new sampled-data technique called switched-current (SI) was introduced [19, 20]. The major advantage of the SI technique compared to the SC technique is the compatibility with standard digital VLSI processes, because it does not need linear capacitors. In this chapter, the conventional switched-current technique is briefly reviewed. It is shown that the conduction gap problem for the conventional SI at low voltage operation is much the same as for the standard SC technique. Finally, a new SI technique that has been proposed in [21] is reviewed.

## 2.2 CONVENTIONAL SWITCHED-CURRENT (SI) TECHNIQUE

### 2.2.1 BASIC OPERATION

Generally, current-mode signal-processing circuits employ the current mirror as their main block. The conventional current mirror is based on matching properties of

transistors. Ideally, the drain current ($I_D$) of the MOS transistor working in saturation [22] can be described in terms of the terminal voltages as

$$I_D = \left(\frac{W}{L}\right)\{f(V_G, V_S)\} \tag{2.1}$$

where W is channel width, L is channel length of MOS transistor, $V_G$, $V_S$ are the gate and source potentials referred to the substrate.

From (2.1), two matched MOS transistors biased in saturation with the same gate and source potentials have ideally the same drain current if their aspect ratios (W/L's) are equal. In the current mirror illustrated in Fig. 2.1.(a), the current enters in a diode-connected MOS transistor (master) to generate a terminal voltage ($V_g$) that depends on the input current ($i_{in}$). The resulting voltage, $V_g$, forces the second transistor (mirror) to draw the same current as the first one.

The basic cell of conventional SI circuits is the current mode sample-hold (S/H) [19] depicted in Fig. 2.1.(b). In this figure, transistor $M_1$ operates in saturation and the output voltage is assumed to drive $M_2$ into saturation also. The input current is stored as a voltage across the gate capacitor of $M_1$. When switch $M_s$ is closed, the drain currents of $M_1$ and $M_2$ are equal, that is, the output current follows the input current (sample). After switch $M_s$ is open, the drain current of $M_2$ ($i_{d2}$) is held constant at its previous value. The circuit shown in Fig. 2.2.(b) is a half delay cell and all conventional SI circuits are derived from it.

The basic SI S/H suffers from certain limitations, such as mismatch between the MOS transistors, finite output impedance and charge injection from the switches. All these error sources limit the accuracy of the sample-hold circuit.

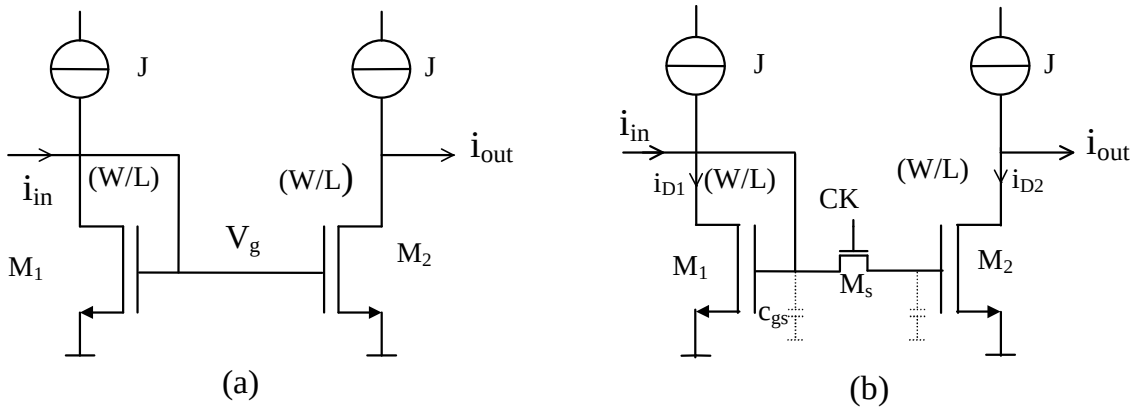



**Fig. 2.1.** Basic block for current mode signal processing.

**(a)** Simple current mirror.

**(b)** Conventional S/H circuit.

The device mismatching is due to the gradual variation during chip fabrication (more details about this subject can be found in chapter 6) and is a common problem in analog integrated circuits. Mismatch can be minimized using special layout techniques. In the SI technique, the dynamic current mirror (current copier) [23, 24] has been proposed to avoid errors due to mismatch because it uses only one MOS transistor to realize the S/H, as shown in Fig. 2.2.(a). Furthermore, the silicon area and the power consumption have been ideally reduced by 50% compared with the simple technique. Fig. 2.2.(a), illustrates dynamic current mirrors controlled by a two-phase clock.

The non-ideal input/output impedances causes errors in current gain in case of two cells in cascade. In a simple current mirror, the typical current gain error is around 1% [25]. To improve the accuracy, the cascode current mirror technique can be used [26]. The cascode SI cell schematic is illustrated in Fig. 2.2. (b). Also, the active current mirror shown in Fig. 2.3.(a) has been used [27, 28] to reduce the effects of the finite output impedance.

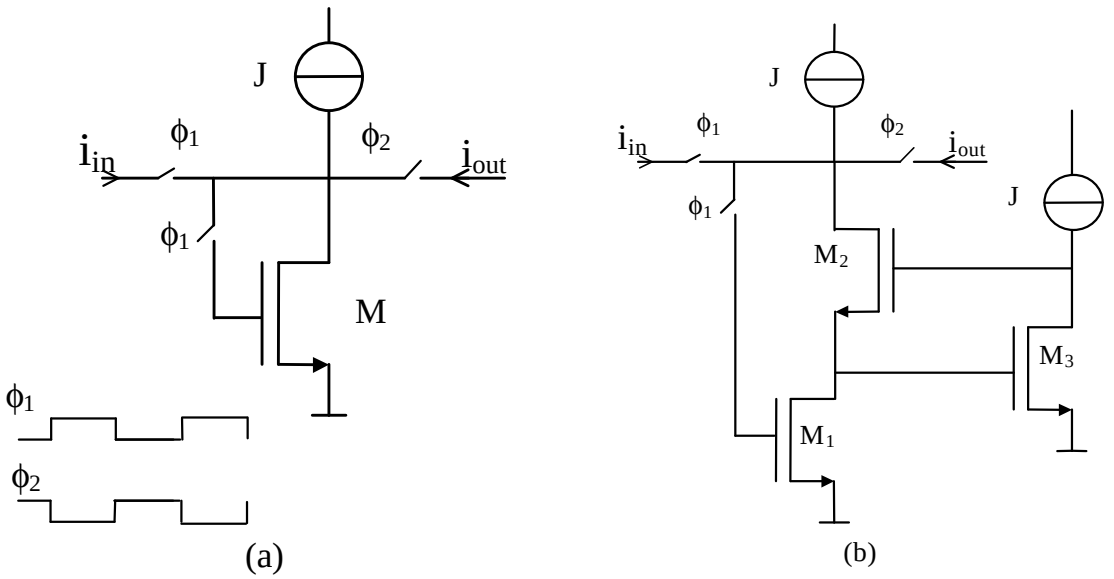



**Fig. 2.2.** Switched-current sample-hold circuits -I.

**(a)** Current copier.

**(b)** Regulated cascode.

Another error source in SI circuits is the charge injected into the holding capacitor during transition of the switch from on to off. This charge results from both the overlap capacitance between gate and the switch terminal to which the holding capacitance is connected and from the channel charge released when the transistor turns off. A portion of the charge injected ($\Delta Q$) into the holding capacitor ($C_G$) during the switching off process changes the gate voltage by $\Delta V_G$. This gate voltage changing produces an error in the drain current

$$\Delta i \approx g_m \Delta Q / C_G \tag{2.2}$$

Thus, a high value of $C_G$, a minimum size switch, or some compensation technique must be used to minimize the charge injection effect.

A common technique used in SC circuits for compensation of the charge injection effect is the dummy MOS switch. Several other techniques, such as the one shown in [25], have been proposed for reducing the effects of charging injection in SI circuits.

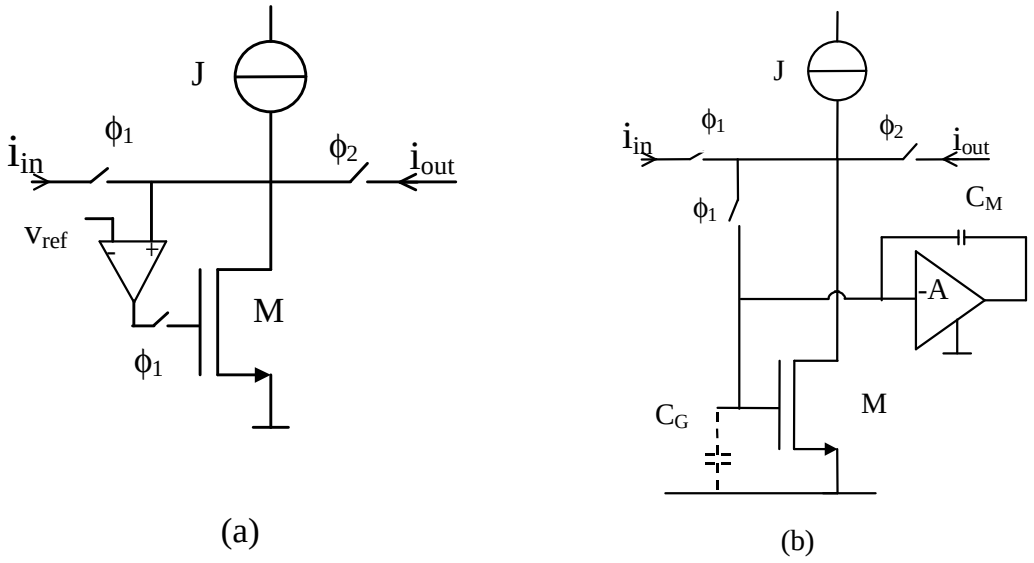



**Fig. 2.3.** Switched-current sample-hold circuits-II.

**(a)** SI sampler with active-negative feedback.

**(b)** Miller-enhanced memory cell.

The dummy transistor with the Miller enhancement method has been proposed in [29] to reduce the effect of charge injection. This method simulates a large capacitor using the Miller effect as shown in Fig. 2.3. (b). The total gate capacitance becomes $(A+1)C_M+C_G$, therefore reducing the charge injection effect (equation 2.2).

### 2.2.2 FIRST AND SECOND GENERATION INTEGRATORS

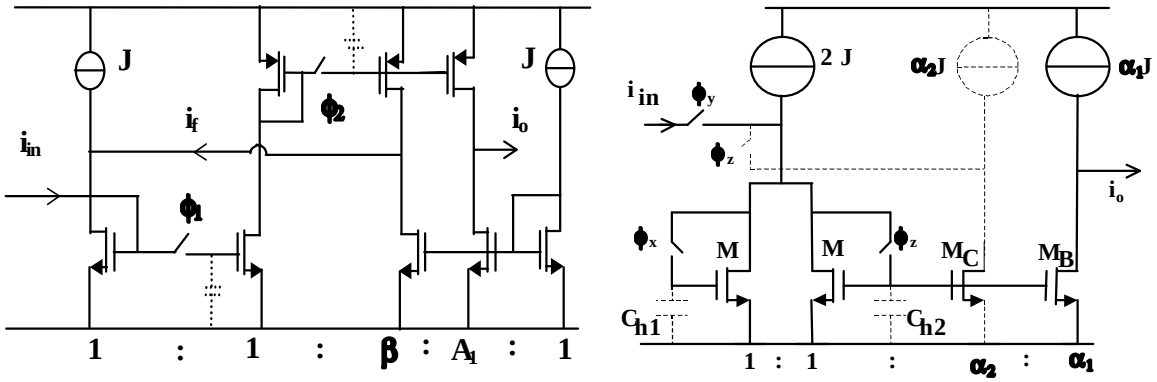
The conventional SI technique presents two integrator architectures [19, 20]. The first generation SI integrator [19], depicted in Fig. 2.4. (a), is composed of two cascaded sample-hold circuits and a feedback path. The first generation integrator suffers from mismatch error and high current consumption.

The second generation SI integrator [20] is illustrated in Fig. 2.4. (b). It is constructed of two dynamic current mirror cells in cascade. The most important advantages of the second generation integrator compared to the first generation integrator are insensitivity to mismatch and small current consumption. The switching

sequence shown in Fig. 2.4.(c) is necessary to avoid the loss of information during clock transition in a practical implementation. The input/output transfer function is given by

$$\frac{I_0^{\phi_1}(z)}{I_{in}^{\phi_1}(z)} = A_1 \frac{z^{-1}}{1-\beta z^{-1}} \tag{2.3}$$

where $A_1 = \alpha_1/(1+\alpha_2)$ and $\beta = 1/(1+\alpha_2)$.



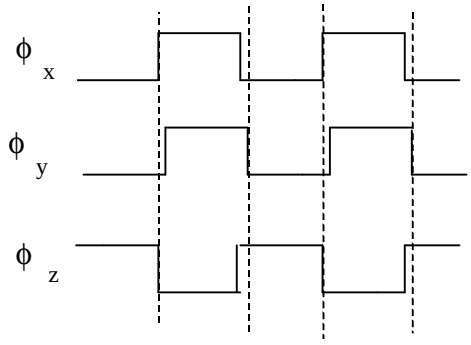




**Fig. 2.4.** Conventional switched-current integrators.

**(a)** First generation SI integrator.

**(b)** Second generation SI integrator.

**(c)** Clock phases.

### 2.2.3 LOW-VOLTAGE OPERATION

Each switch in conventional SI circuits operates at a signal dependent voltage as can be seen in Figs. 2.1 and 2.2. Thus, for low voltage operation, each switch is susceptible to the conduction gap [10]. Therefore, conventional SI circuits, like standard SC circuits, are not suitable for low-voltage operation.

For proper operation, the output voltage of the current copier (Fig. 2.2.a) is limited by the drain-source saturation voltage of the transistor and by a maximum critical voltage ($V_{crit}$) related to the maximum allowable settling time. $V_{crit}$ should not be larger than a certain value that would ensure a minimum on-conductance of the n-MOS switch. At low supply voltage , the biasing current J must be adjusted to force the output voltage to be within this voltage range. Note that both the on-conductance and the channel charge of the n-MOS switch are dependent of the signal level. Consequently, charge injection becomes signal-dependent, and thus difficult to compensate.

## 2.3 NEW METHODOLOGY FOR LOW-VOLTAGE

### 2.3.1 DELAY/AMPLIFIER CELL

Recently a new SI technique has been developed in [21]. The basic cell in this method is the current mirror circuit shown in Fig. 2.5. (a). Assuming that the operational amplifier is ideal, transistors $M_1$ and $M_2$ are both biased with the same set of voltages. Neglecting transistor mismatch, we obtain:

$$i_o = -\left[(W/L)_{M2}/(W/L)_{M1}\right] i_{in} \qquad (2.4)$$

Therefore, the output current $i_o$ is an inverted replica of the input current $i_{in}$.

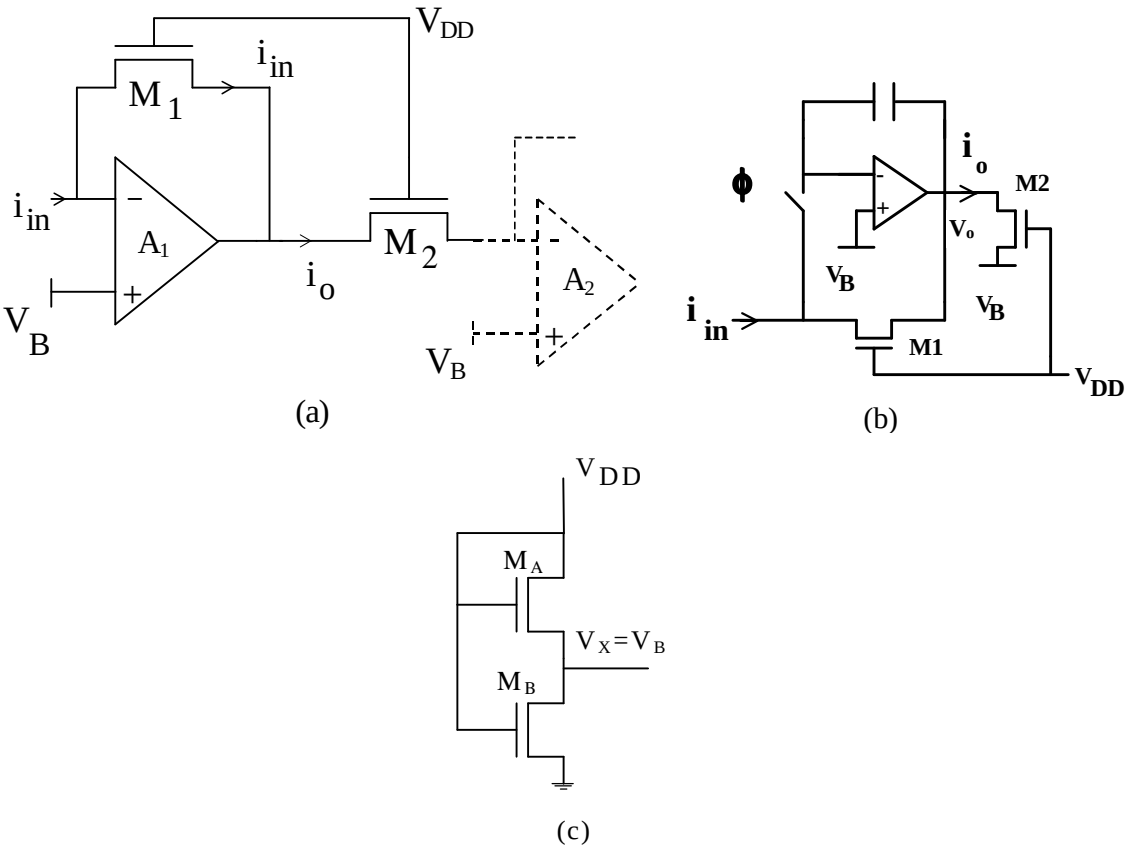



**Fig. 2.5.** The basic cells of the switched-current technique [21].

**(a)** Current mirror.

**(b)** Switched-current S/H block.

**(c)** The bias voltage generation.

Based on this current mirror, the sample-hold circuit illustrated in Fig. 2.5.(b) was proposed in [21]. The circuit operates as follows :

1. When the switch is closed, the hold capacitor is charged to a voltage V whose value depends on the input current $i_{in}$, the transistor parameters, and the gate voltage. The output current is such that $i_o = -\beta i_{in}$, where $\beta = (W/L)_{M2}/(W/L)_{M1}$.
2. When the switch opens, a voltage equal to V is held on the capacitor and the current is sustained at the output.

An important property of the proposed current mirror is that the switches operate at a constant voltage $V_B$ provided by the bias circuit shown in Fig. 2.5. (c). Therefore, the

conduction gap [8, 10] of the switches at low power supply voltages is avoided. Furthermore, the holding capacitor is not necessarily a linear capacitor. Also, the charge injected during turn-off is signal-independent, which improves the accuracy of the S/H circuit.

An appropriate choice of the bias voltage ($V_B$) allows for the highest current swing. Fig. 2.5.(c) illustrates the bias voltage generation [21, 30]. $M_A$ and $M_B$ are identical transistors. Thus, $V_x$ ($V_B$) can be calculated as:

$$V_X = V_P\left(1 - 1/\sqrt{2}\right) \tag{2.5}$$

where $V_P = (V_G - V_{Ton})/n$ is the pinch-off voltage [30,31], $V_G$ is the gate-to-bulk voltage, $V_{Ton}$ is the threshold voltage and n is the slope factor.

## 2.3.2 ANALOG ERRORS IN A CURRENT MIRROR [21 , 32]

### *2.3.2.1 Op-amp finite gain*

The finite gain of the op amp of Fig. 2.5. (a) causes an error in the current gain equal to

$$\varepsilon = \frac{-1}{A_{vo}}\left\{\frac{g_{ms1}}{g_o}\left(1 + A_i\right) + 1\right\} \tag{2.6}$$

where $A_{vo}$ is DC open-loop gain of the op amp, $g_{ms1}$ is the source transconductance of $M_1$, $g_o$ is output conductance of the op amp and $A_i$ is the current gain.

### *2.3.2.2 Op-amp finite bandwidth*

The bandwidth of the current mirror in Fig. 2.5. (a) is determined by the op-amp gain-bandwidth product provided that the intrinsic cutoff frequencies of $M_1$ and $M_2$ are higher than the op amp gain-bandwidth product.

### *2.3.2.3 Op-amp offset voltage*

A difference ($\Delta V_{OS}$) between the offset voltages of the op-amps ($A_1$ and $A_2$) in Fig. 2.5.(a) gives rise to a DC error $\Delta i_o$ in the output current given by

$$\frac{\Delta i_o}{i_{o\,max}} = 2\sqrt{2}\,\frac{\Delta V_{OS}}{V_P} \tag{2.7.a}$$

where

$$i_{o\,max} = \frac{\beta_2 n}{4} V_P^2 \tag{2.7.b}$$

### *2.3.2.4 Transistor mismatch*

A difference in the transconductance parameters produces a relative gain error proportional to the mismatch in the transconductance parameters. A mismatch in the threshold (pinch-off) voltage causes gain error and harmonic distortion, summarized by the following expression:

$$x_2 = \left(1 + \frac{\Delta V_P}{V_P}\right) x_1 + \frac{\Delta V_P}{V_P}\left(\frac{x_1^2}{8} + \frac{x_1^3}{32} + ..\right) \tag{2.8}$$

where $\frac{\Delta V_P}{V_P} = \frac{\Delta V_{TO}}{V_{DD} - V_{TO}}$ is the threshold voltage mismatch normalized to the overdrive voltage and $x_1 = i_{in}/i_{in\,max}, x_2 = i_o/i_{o\,max}$ are the normalized input and output currents.

### *2.3.2.5 Noise*

The noise component of the output current is due to the op-amp noise, the noise generated by transistors $M_1$ and $M_2$ as well as the input noise. The mean square value of the output current noise component is given by

$$\overline{i_o^2} = \left(\frac{g_{ms2}}{g_{ms1}}\right)^2 \left(\overline{i_{in}^2} + \overline{i_1^2}\right) + \overline{i_2^2} + g_{ms2}^2\,\overline{v_{ao}^2} \tag{2.9}$$

where $\overline{i_{in}^2}$, $\overline{i_1^2}$ and $\overline{i_2^2}$ are the mean square values of the input current noise and the current noise of $M_1$ and $M_2$ respectively. $\overline{v_{ao}^2}$ is the mean square value of the op-amp noise voltage referred to its input. Finally, $g_{ms2}$ is the source transconductance of $M_2$.

### 2.3.3 FIRST GENERATION INTEGRATOR

The low-voltage SI technique proposed in [21] introduced the first generation SI integrator using the sample-hold circuit shown in Fig. 2.5. (b). The first generation SI lossy integrator is depicted in Fig. 2.6. (a). The timing clock diagram is illustrated in Fig. 2.6.(b).

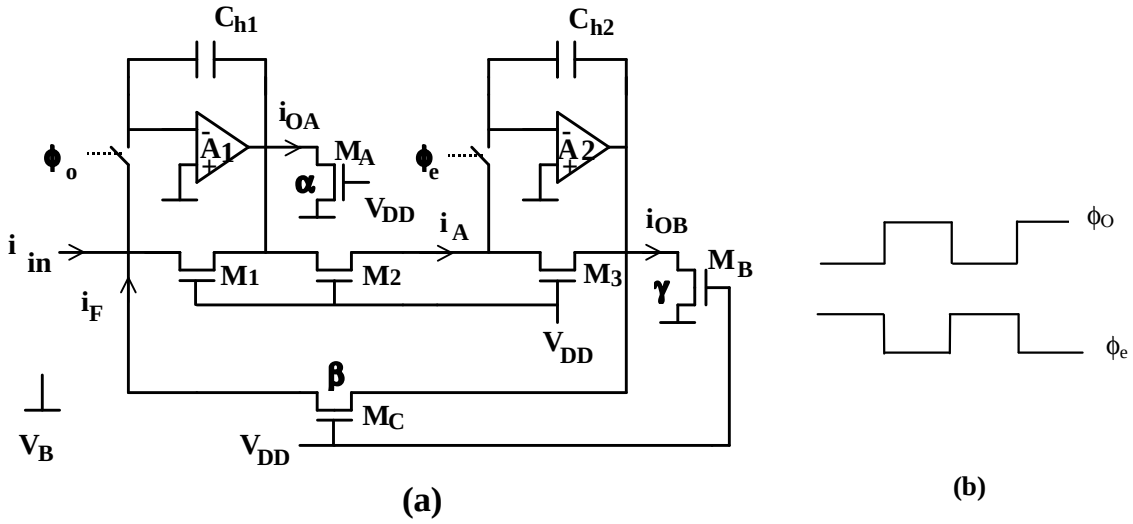



**Fig. 2.6.** First generation SI integrator for low-voltage applications.

**(a)** Circuit schematic**.**

**(b)** Clock sequence.

The integrator works as follows:

- During $\phi_o$, the sum of the input and feedback currents is written in the first memory cell as a voltage across $C_{h1}$;
- During $\phi_e$, the input ($i_A$) to the second cell is stored as a voltage signal across $C_{h2}$.

Assuming $M_1$, $M_2$ and $M_3$ to be matched and to have the same aspect ratios, the integrator presents the following transfer functions at its outputs

$$\frac{I_{0A}^{\phi_o}(z)}{I_{IN}^{\phi_o}(z)} = -\alpha \frac{1}{1-\beta z^{-1}} \qquad (2.10.a)$$

$$\frac{I_{0B}^{\phi_o}(z)}{I_{IN}^{\phi_o}(z)} = \gamma \frac{z^{-1}}{1-\beta z^{-1}} \qquad (2.10.b)$$

Where $\alpha=(W/L)_{MA}/(W/L)_{M1}$, $\beta=(W/L)_{MC}/(W/L)_{M3}$ and $\gamma=(W/L)_{MB}/(W/L)_{M3}$.

## 2.4 THE CURRENT DIVISION TECHNIQUE AND THE MOCD STRUCTUTRE

The MOSFET-only current division technique was reported in [33]. In this work, the programmability of the SI filters is achieved through the MOSFET-only current dividers (MOCD's). The general schematic of the MOCD and its symbol [21, 33] are illustrated in Fig. 2.7. All transistors of the MOCD are connected to $V_{SS}$ through a common substrate and have equal (W/L) aspect ratios. Therefore, the circuit operates as a binary current divider. Each binary fraction of the input current is injected into the SUM or DUMP lines according to the following rule:

$$b_i \begin{cases} 1 & \text{Current flows to SUM terminal.} \\ 0 & \text{Current flows to DUMP terminal.} \end{cases}$$

i = 1,2,3,.....M, and M is the MOCD resolution.

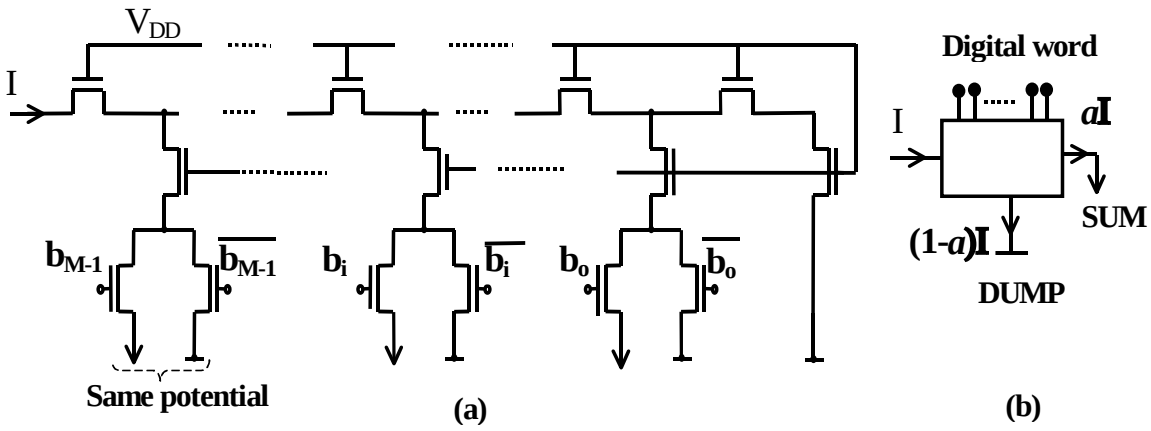



**Fig. 2.7.** The MOCD circuit scheme and its symbol.

The output current of the MOCD is a digitally controlled fraction (a) of the input current. This fraction is related to the digital control word as

$$a = \sum_{i=0}^{M-1} b_i 2^{(i-M)} \tag{2.11}$$

Here, we use the MOCD as a digitally programmable coefficient with capability to implement the sign-bit. The MOCD has an input impedance which is independent of both the digital word and the number of bits, thus providing a constant load impedance to the op amps.

Several non-ideality parameters such as mobility degradation due to vertical field, velocity saturation, mismatch and noise produce errors. Analysis of these error sources and their influence on the performance of the MOCD is reported in [34]. The high linearity of the MOSFET-only current division technique has been proved adequate for analog signal processing [33, 34, 35].

- **AC ANALYSIS**

As regards DC analysis, the MOCD is equivalent to one transistor whose aspect ratio is one half the aspect ratio of a single transistor of the MOCD. For transient analysis,

the MOCD is equivalent to a nonlinear RC network. The exact AC analysis of the MOCD is relatively complicated. In a digital to analog (D/A) converter [35], only the parasitic capacitor associated with $M_3$ and $M_4$ in Fig. 2.8 has been considered for transient analysis. In other words, the MOCD time constant is the necessary time for the current to be deviated from one branch to the other (DUMP and SUM).

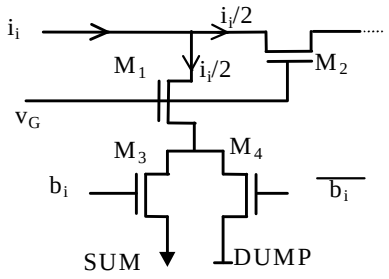



**Fig. 2.8.** The $i^{th}$ bit of the MOCD in Fig. 2.7.

In this work, we will approximate each one-bit section as one transistor. From the MOST model [22], the intrinsic cutoff frequency of an MOS transistor can be approximated as:

$$f_T = \frac{\mu\phi_t}{2\pi L^2} 2\left(\sqrt{1+i_f} - 1\right) \tag{2.12}$$

Details about MOS transistor modeling are presented in Appendix A.

An M-bit MOCD can be considered as the cascade of M sections, where each section is equivalent to a single transistor. For worst case analysis, we will assume that the bits are settled in cascade. The total delay time can be approximated as

$$\tau_{Total} = \sum_{i=1}^{M} \tau_{ui} \cong M\ \tau_u \tag{2.13}$$

where $\tau_{ui}$ is the delay of the $i^{th}$ section and all sections are assumed to have equal delays.

The intrinsic cutoff frequency for the MOCD can be approximated as $(1/2\pi\tau_{Total.})$. Thus, the maximum MOST channel length (L) that can be used is

$$L \le \sqrt{\frac{\mu.\phi_t}{M.2\pi.f_T} 2\left(\sqrt{1+i_f} - 1\right)} \qquad (2.14)$$

The MOSFET maximum channel length can be approximated using (2.14), assuming $f_T=10F_{CK}$.

To verify our analysis, a 6-bit MOCD for 20 MHz clock frequency has been designed and simulated with 40μA (1 MHz) input current. The time and frequency responses are illustrated in Fig.2.9. The frequency response shows that the cutoff frequency is approximately 180 MHz, which is satisfactory for our application (10 MHz cutoff frequency).

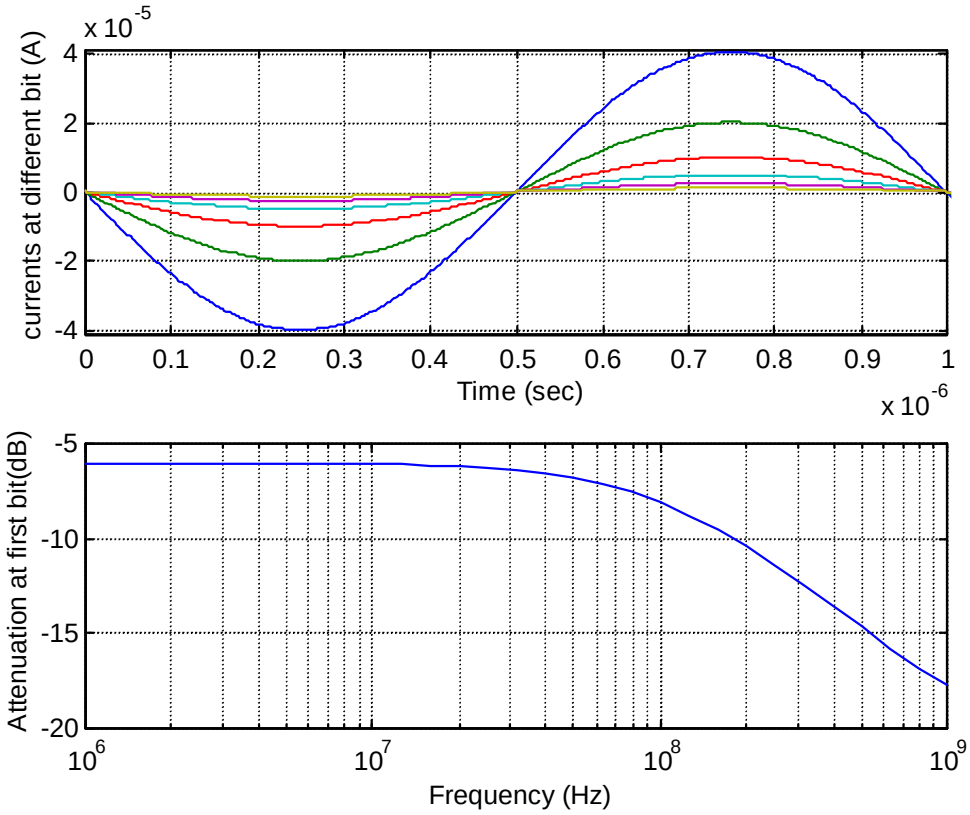



**Fig. 2.9.** The time and frequency response of the MOCD in Fig. 2.7.