

CONTENTS

• List of figures	iv
• List of tables	viii
• Preface.....	ix
1 Low-Voltage Analog Design	
1.1 Introduction.....	1
1.2 Limitations of low-voltage operation	3
1.3 Low-voltage circuit design techniques	
1.3.1 Technology considerations for low-voltage analog circuits	6
1.3.2 Design strategy for low-voltage circuits.....	7
2 Switched-Current Techniques and Low-Voltage Operation	
2.1 Introduction.....	9
2.2 Conventional switched-current (SI) technique	
2.2.1 Basic operation	9
2.2.2 First and second generation integrators	13
2.2.3 Low-voltage operation.....	15
2.3 New methodology for low-voltage	
2.3.1 Delay/amplifier cell.....	15
2.3.2 Analog errors in a current mirror.....	17
2.3.3 First generation integrator.....	19
2.4 The current division technique and the MOCD structure.....	20
3 Programmable Second Generation Switched-Current Integrator and Biquad for Low-Voltage Applications	
3.1 Introduction	24
3.2 Second generation integrator	
3.2.1 Basic cell.....	24
3.2.2 The effect of the op-amp offset voltage.....	28

3.3 Second order section

3.3.1	General block diagram.....	33
3.3.2	Mapping error analysis.....	34
3.3.3	Implementation of the switched-current biquad	36
3.3.4	Effect of the offset voltage of the op-amps on the biquad output.....	39

4 Programmable Switched-Current Sample-Hold Circuits

4.1	Introduction	41
4.2	Single-ended sample-hold	42
4.3	A fully balanced switched-current sample-hold circuit.....	46
4.3.1	Fully balanced op-amp design.....	47
4.3.2	Fully balanced SI sample-hold circuit architecture	50
4.3.3	Sign-bit realization	51
4.3.4	Programmable fully balanced sample-hold.....	53
4.4	Interface blocks	53
4.4.1	Single-ended input to balanced-output converter.....	54
4.4.2	Voltage-to-current and current-to-voltage converters.....	56

5 Circulating Finite Impulse Response (FIR) Filter-Architecture and

Implementation

5.1	Introduction.....	57
5.2	Applications.....	57
5.3	Circulating form of the FIR filter.....	59
5.4	Digital control circuits.....	62
5.5	Switched-current realization of the circulating FIR filter	
5.5.1	Single-ended 4-tap switched-current FIR filter	64
5.5.2	Fully balanced FIR switched-current filter	68

6 Filter Layout and Testing

6.1	Introduction.....	73
-----	-------------------	----

6.2 Considerations on layout for analog circuits	73
6.3 Considerations on layout for mixed analog-digital chips.....	75
6.4 CAD tools	76
6.5 Layout of the single-ended 4-tap FIR filter.....	78
6.6 Layout of the fully balanced sample-hold	79
6.7 Chip testing and measurements	80
Conclusions	84
Appendix A. MOSFET Model in Strong Inversion	85
Appendix B. Design of The Two-Stage CMOS Operational Amplifier	87
References	92