

# LIST OF FIGURES

<b>Fig. 1.1.</b> The common-mode input range and output range of an op-amp.....	4
<b>Fig.1.2.</b> The sample-hold circuit.....	5
<b>Fig.1.3.</b> On-conductance of a CMOS switch for $V_{DD}=5V$ and $1.5V$ .....	5
<b>Fig.1.4.</b> Switched-opamp technique [10] .....	8
<b>Fig. 2.1.</b> Basic block for current mode signal processing.....	11
<b>Fig. 2.2.</b> Switched-current sample-hold circuits-I.....	12
<b>Fig. 2.3.</b> Switched-current sample-hold circuits -II.....	13
<b>Fig. 2.4.</b> Conventional switched-current integrators.....	14
<b>Fig. 2.5.</b> The basic cells of the switched-current technique [21].....	16
<b>Fig. 2.6.</b> First generation SI integrator for low-voltage applications .....	19
<b>Fig. 2.7.</b> The MOCD circuit scheme and its symbol. ....	21
<b>Fig. 2.8.</b> The $i^{th}$ bit of the MOCD in Fig. 2.7.....	22
<b>Fig. 2.9.</b> The time and frequency response of the MOCD in Fig. 2.7.....	23
<b>Fig. 3.1.</b> The low-voltage SI integrator on different phases.....	25
<b>Fig. 3.2.</b> The low-voltage second generation SI integrator.....	26
<b>Fig. 3.3</b> Sinusoidal steady state response of the low-voltage integrator.....	29
<b>Fig. 3.4.</b> Scheme of the low-voltage SI integrator including op-amp offset voltages.....	30
<b>Fig. 3.5.</b> Offset compensation for the SI technique [40].....	31
<b>Fig. 3.6.</b> Frequency response of the low-voltage second generation SI integrator in Fig. 3.2 .....	32
<b>Fig. 3.7.</b> Block diagram of a biquad.....	33
<b>Fig. 3.8.</b> Magnitude error at the center frequency for backward Euler transformation..	35
<b>Fig. 3.9.</b> Magnitude error at the center frequency for the backward LDI transformation.	36

<b>Fig. 3.10.</b> Biquadratic section using second-generation SI integrators.....	37
<b>Fig. 3.11.</b> Theoretical (....) and experimental ( ____ ) magnitude response of the bandpass filter.....	38
<b>Fig. 4.1.</b> The switched-current sample-hold circuit.....	42
<b>Fig. 4.2.</b> Digitally programmable sample-hold.....	44
<b>Fig. 4.3.</b> The step response of the sample-hold circuit.....	45
<b>Fig. 4.4.</b> The sinusoidal response of the sample-hold circuit.....	46
<b>Fig. 4.5.</b> Block diagram of op-amps.....	47
<b>Fig. 4.6.</b> Circuit used to detect the common-mode input voltage.....	48
<b>Fig. 4.7.</b> Fully balanced op-amp schematic.....	48
<b>Fig. 4.8.</b> The frequency and DC responses of the balanced op-amp..	49
<b>Fig. 4.9.</b> Fully balanced sample-hold circuit.....	50
<b>Fig. 4.10.</b> The sinusoidal and step responses of the sample-hold in Fig.4.9.....	51
<b>Fig. 4.11.</b> The sign-bit implementation using two MOCD inputs [51].....	52
<b>Fig. 4.12.</b> Proposed method for sign-bit realization.....	53
<b>Fig. 4.13.</b> The time response of the programmable SI sample-hold circuit.....	54
<b>Fig. 4.14.</b> Block diagram for current-mode signal processing.....	54
<b>Fig. 4.15.</b> Differential-input to balanced-output converter [52].....	55
<b>Fig. 4.16.</b> The DC and frequency responses of the circuit shown in Fig. 4.15.....	55
<b>Fig. 4.17.</b> ( a ) V/I converter. ( b ) I/V converter.....	56
<b>Fig. 5.1.</b> Realization forms of the analog delay line.....	58
<b>Fig.5.2.</b> Block diagram of an adaptive DF equalizer.....	59
<b>Fig.5.3.</b> General schematic of an N-tap FIR filter.....	60
<b>Fig. 5.4.</b> The schematic of the one-bit circulating circuit.....	62
<b>Fig. 5.5.</b> The sequential control circuit.....	63
<b>Fig. 5.6.</b> Clock generator.....	63

<b>Fig. 5.7.</b> The 4-tap FIR filter in circulating form.....	65
<b>Fig. 5.8.</b> Switching methodology to reduce charge injection .....	66
<b>Fig. 5.9.</b> Simulation results for the circuit of Fig. 5.8.....	67
<b>Fig. 5.10.</b> Pure delay of 4 clock cycles ( $h_1=h_2=h_3=00$ and $h_4=3F$ ).....	67
<b>Fig. 5.11.</b> The magnitude response of the FIR filter for different digital words.....	68
<b>Fig. 5.12.</b> 8-tap fully balanced switched-current FIR filter.....	69
<b>Fig. 5.13.</b> A fully balanced op-amp and its simulated model.....	70
<b>Fig. 5.14.</b> The frequency response of the low-pass filter.....	71
<b>Fig. 5.15.</b> The frequency response of the bandpass filter-I.....	71
<b>Fig. 5.15.</b> The frequency response of the bandpass filter-II.....	72
<b>Fig. 6.1.</b> Different layouts for wide MOS transistors.....	74
<b>Fig. 6.2.</b> General floor plan for mixed analog-digital chip .....	76
<b>Fig. 6.3.</b> Op-amp layout.....	78
<b>Fig. 6.4.</b> The layout of the single-ended 4-tap FIR filter.....	79
<b>Fig. 6.5.</b> Layout of the fully balanced sample-hold and transistor placement .....	80
<b>Fig. 6.6.</b> The fully balanced test chip.....	81
<b>Fig. 6.7.</b> The single-ended 4-tap FIR filter chip micrograph .....	82
<b>Fig. 6.8</b> The switched-current S/H .....	82
<b>Fig. 6.9.</b> Measured, simulated and theoretical frequency response of the 4-tap FIR filter .....	83
<b>Fig. 6.10.</b> Pure delay measurement.....	83
<b>Fig. A.1.</b> NMOS transistor.....	85
<b>Fig. B.1.</b> Two-stage Miller OTA configuration.....	87
<b>Fig B.2.</b> Small signal equivalent circuit of the amplifier in Fig. B.1.....	88
<b>Fig. B.3.</b> The frequency response and DC transfer characteristic of the op-amp.....	90

**Fig. B.4.** Unity gain configuration for measuring the settling time ..... 91

**Fig. B.5.** The step response of the circuit in Fig. B.4..... 91