APPENDIX B.

DESIGN OF THE TWO-STAGE CMOS OPERATIONAL AMPLIFIER

B.1 GENERAL BACKGROUND [68, 69]

The configuration of a two-stage CMOS Miller Operational Transconductance Amplifier (OTA) is shown in Fig.B.1. The first stage consists of the differential input stage with p-channel MOS transistors ($M_{1,2}$), the biasing current mirror ($M_{7,8}$) and the nMOST ($M_{3,4}$) active load. The second stage is made up of M_6 as the current driver and M_5 as the active load.

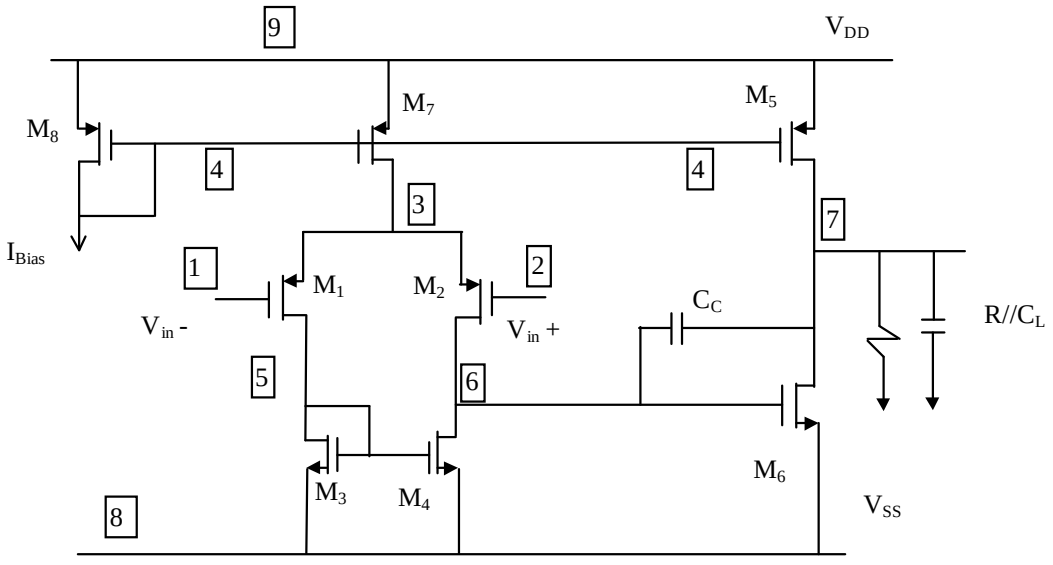

Fig. B.1. Two-stage Miller OTA configuration.

The small signal equivalent circuit is illustrated in Fig. B.2.

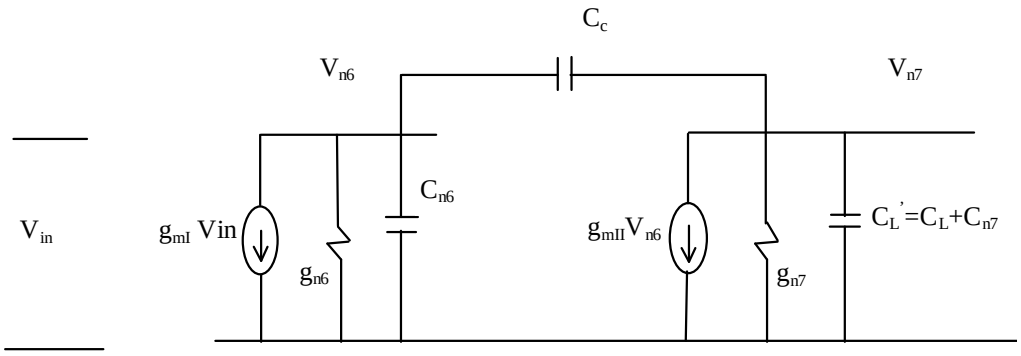

Fig B.2. Small signal equivalent circuit of the amplifier Fig. B.1.

where g_{mI} the transconductance of the first stage (M_1).

g_{mII} the transconductance of the second stage (M_6).

C_{n6} the equivalent parasitic capacitor at node 6.

C_{n7} the equivalent parasitic capacitor at node 7.

g_{n6} the equivalent conductance at node 6 ($g_{d4} + g_{d2}$).

g_{n7} the equivalent conductance at node 7 ($g_{d5} + g_{d6}$).

The basic equations for poles, zero and gain-bandwidth can be written as:

$$f_{p1} = \frac{g_{mI}}{2\pi\ A_O Cc} \qquad (B.1)$$

$$f_{p2} = \frac{g_{mII}}{2\pi C_L} \qquad (B.2)$$

$$f_z = \frac{g_{mII}}{2\pi Cc} \qquad (B.3)$$

$$GB = \frac{g_{mI}}{2\pi Cc} \qquad (B.4)$$

The DC open loop gain A_o is given by

$$A_o = \frac{g_{mI} g_{mII}}{g_{n6} g_{n7}} \qquad (B.5)$$

The ratio C_c/C_L can be approximated as:

$$\frac{Cc}{C_L} \cong \frac{f_{p2}}{GB} tg(90^o - PM) - 1 \qquad (B.6)$$

where PM is the phase margin.

The small circuit parameters ($g_{mI,}$ $g_{mII,}$ C_C) are fully defined if Cc/C_L and f_{p2}/GB are chosen. From the MOS transistor model [22], the aspect ratio (W/L) can be calculated as:

$$\frac{W}{L} = \frac{g_{ms}}{\mu n C'_{ox} \phi_t} \frac{1}{\sqrt{1+i_f} - 1} \tag{B.7}$$

when g_{ms} is source transconductance. More details about the op-amp design methodology are presented in [68, 69]

B.2 OP-AMP DESIGN AND SIMULATION

In the SI technique [21] employed here, the load capacitor of the op-amp is the holding capacitor (C_h) and the parasitic capacitors attached to the output node (C_{n7}). The parasitic capacitors are the gate-drain, overlap and the drain-bulk capacitors of the MOS transistor. The load capacitor is approximated by 2pF. For the sampled–hold circuit designed in chapter 4, the op-amp specifications are presented in Table B.1.

Table B.1: Op-amp specifications.

Parameters of OTA	Values	Dimension
Supply voltage ……..	3($\pm$1.5)	V
Transconductance(g_m)……	~55	mA/V
GB(Gain Bandwidth Product)……	~100	MHz
Phase Margin ……	>50^o	
Load resistance (MOST W=6µm and L=5µm)…….	~10	kΩ
Load capacitance (C_L).	2.0	pF

-Design steps

- Select (P_2/GB)=5 $\rightarrow$ g_{mI}=630 µA/V, g_{mII}=6.3 mA/V and C_C =1pf .

- Select $\gamma = 0.5$.

The geometry of transistors and the simulation results are given in Table B.2. The frequency response and DC transfer function are shown in Fig. B.3.

Table B.2. Design parameters of the op-amp and simulated specifications.

$\mathbf{i_{f6}}$	*300*
$\mathbf{i_{f1}}$	*176*
W of M1,2	*165* µm
W of M3,4	*32* µm
W of M7,8	*32* µm
W of M_5	*300* µm
W of M_6	*600* µm
Total Current	*4* mA
I_{Bais}	*350* µA
GB	*100* MHz
Phase margin	64^o
A_O	*65* dB

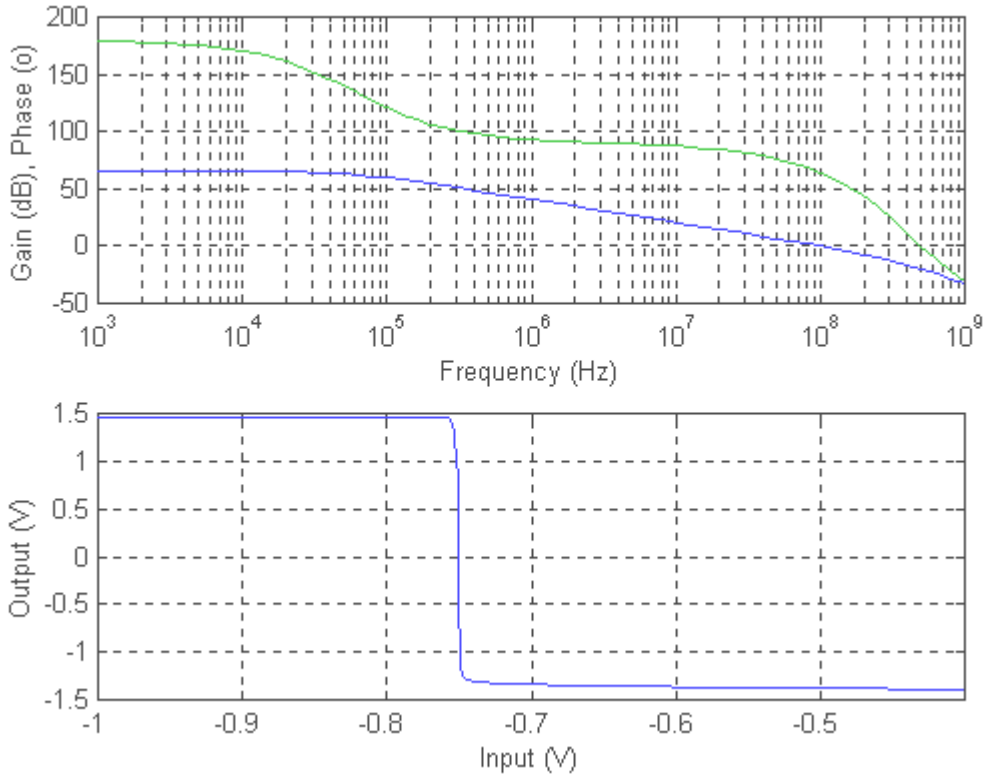

Fig. B.3. The frequency response and the DC transfer characteristic of the op-amp.

To measure the settling time, the op-amp is connected as shown in Fig. B.4. In the simulation result shown in Fig. B.5, the 1% settling time is around 9n sec.

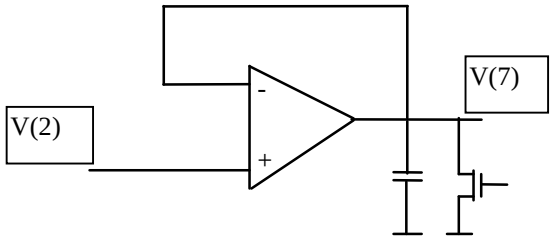

Fig. B.4. Unity gain configuration for measuring the settling time.

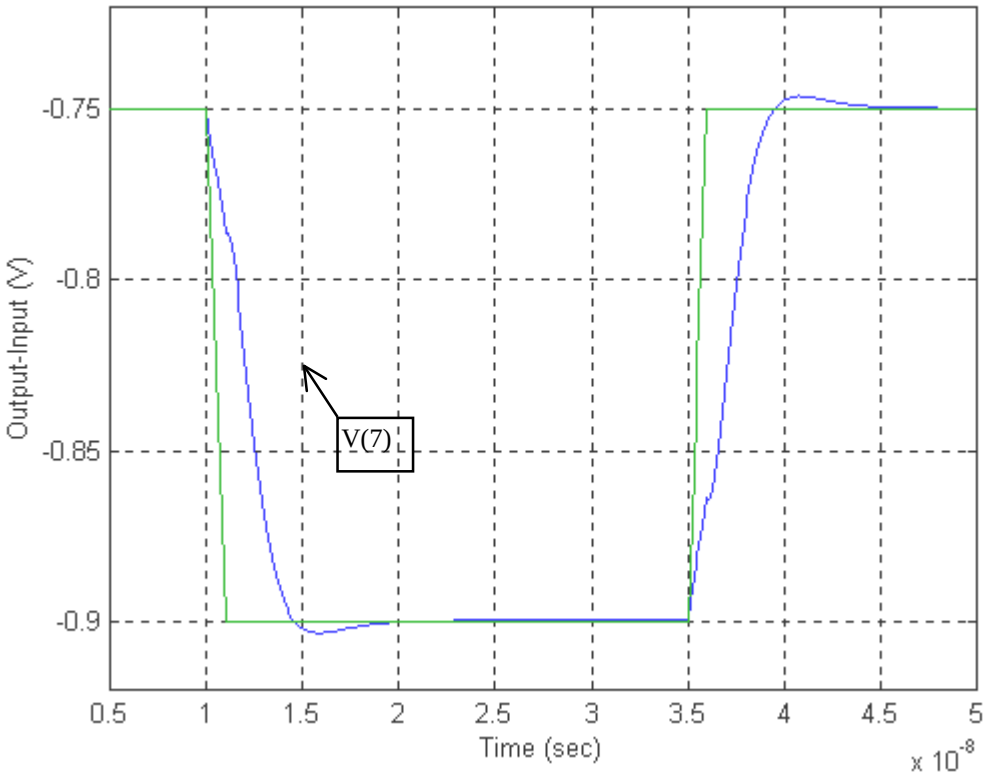

Fig. B.5. The step response of the circuit in Fig. B.4.