PREFACE

This thesis is concerned with digitally programmable switched-current technique suitable for low voltage power supply. Programmable single-ended and fully balanced filter (IIR and FIR) blocks are designed and tested. The programmability of the switched-current circuits is achieved by using the current division technique. The thesis is organized as follows.

In the first chapter, we review some key limitations in analog circuit design at low power supply voltage.

In Chapter 2, the conventional switched-current technique is briefly reviewed. It is shown that the conduction gap problem for the conventional SI technique at low voltage operation is much the same as for the standard SC technique. Finally, a new SI technique that has been used in this work is reviewed.

In Chapter 3, a second generation SI integrator is proposed. A programmable integrator-based biquad, which allows independent tuning of the center frequency and the quality factor has been implemented.

Chapter 4 is dedicated to the analysis and design of programmable single-ended and fully balanced SI sample-hold circuits for 20 MHz sampling rate.

Chapter 5 is dedicated to the design and simulation of a finite impulse response (FIR) filter. The circulating form realization of the FIR filters (single-ended and fully balanced) is used to reduce the multiple re-sampling errors.

In Chapter 6, a description of the layout of some circuits designed during the preparation of this work together with experimental results is presented.