CHAPTER 4

PROGRAMMABLE SWITCHED-CURRENT SAMPLE-HOLD CIRCUITS

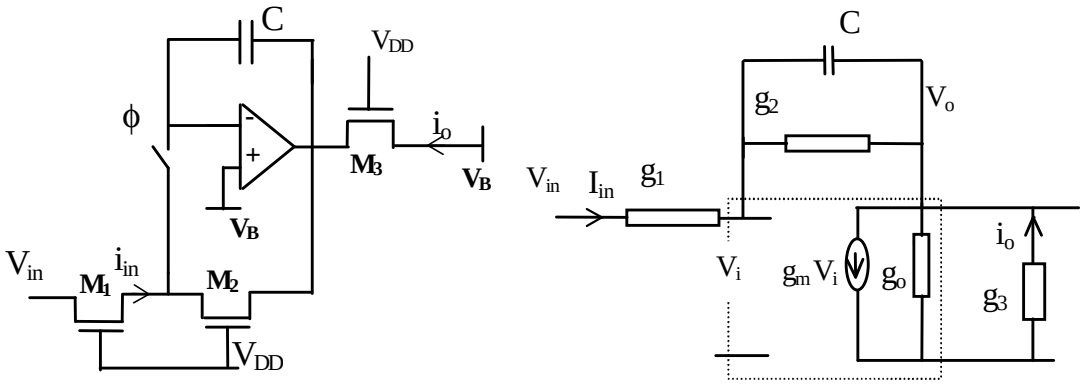
4.1 INTRODUCTION

Field programmable integrated circuits (ICs) are receiving increased attention. Particularly, programmable filters can be used in signal processing applications such as adaptive filters, spectral analysis, equalization, waveform synthesis and many others. CMOS programmable filters are typically implemented by using charge coupled devices (CCD) and switched-capacitor techniques. In the SC technique, digitally controlled binary-weighted C-arrays [44] or charge-programmability [45] are used to digitally program a filter. The C-array technique requires large silicon area compared with the SI technique while the charge programmability approach is slow. The most common methodologies to design programmable SI filters employ either digitally programmable conventional current mirrors [46, 47] or digitally controlled MOSFET-only attenuators [33]. Both approaches take advantage of the reduced area required to implement programmable current mode filters.

This chapter is dedicated to the analysis and design of programmable single-ended and fully balanced SI sample-hold circuits using the SI methodology of [21]. The programmability is achieved via the current division technique. The complete programmable S/H circuit has been designed for 20 MHz sampling rate.

4.2 SINGLE-ENDED SAMPLE-HOLD

In this section, the design of a switched-current S/H circuit for low-voltage applications is presented. The main objectives are to obtain the op-amp specification, the holding capacitor value and the MOS transistor aspect ratios. Fig. 4.1.(a) shows the circuit of the S/H.



(a) (b)

Fig. 4.1. The switched-current sampled-hold circuit.

(a) Scheme.

(b) Small-signal equivalent circuit.

In the small signal equivalent circuit illustrated in Fig.4.1.(b), the op-amp is assumed to have infinite bandwidth and the switch to be ideal. The transfer function H(s) of the S/H can be written as:

$$H(s) = \frac{G_o}{1+s\tau} \tag{4.1}$$

where

$$G_O = -\frac{g_1}{g_2}\frac{1-g_2/g_m}{1+\dfrac{g_1+g_L+g_Lg_1/g_2}{g_m}} \tag{4.2.a}$$

and

$$\tau = \frac{C}{g_2}\frac{1}{1+\frac{g_L g_1 / g_2}{g_m + g_L + g_1}} \quad (4.2.b)$$

$g_L=g_3+g_o$ and g_1, g_2 and g_3 are the drain-source conductances of the MOSFETs, which in strong inversion are given by:

$$g_{mS} = \mu n C'_{ox} \frac{W}{L}(V_P - V_s) \quad (4.3)$$

The circuit in Fig. 4.1.(a) performs as an ideal inverting amplifier ($G_O \cong -g_1/g_2$) when

$$g_m >> g_1 + g_L + g_L g_1 / g_2 \quad (4.4.a)$$

In this case

$$\tau \approx \frac{C}{g_2} \quad (4.4.b)$$

Moreover, in high-speed applications, the settling error is an important issue. Using (4.1) at the end of the sampling phase (t = T/N) (N is the number of phases) the settling error is given by

$$\gamma = e^{(-T/N\,\tau)} \quad (4.5)$$

which affects the sample-hold transfer function [48] according to

$$H(z) = \frac{(1-\gamma)}{1-\gamma z^{-1}} z^{-1/2} \quad (4.6)$$

Moreover, the maximum value of the holding capacitance (C) such that the settling error is less than γ, can be expressed as

$$C < T g_2 / \{N \ln(1/|\gamma|)\} \quad (4.7)$$

However, C should be large enough to reduce the (kT/C) noise.

- **DESIGN STEPS**

As a conclusion about the previous analysis, the design steps are:

- The MOSFET maximum channel length can be approximated using (2.14), assuming $f_T=10F_{CK}$.
- (4.7) is used to obtain the required holding capacitor and channel width for a certain settling error.
- The total op-amp transconductance required can be approximated using (4.4.a) and the op-amp gain bandwidth product is selected as 10 g_2/ C.

- **PROGRAMMABLE S/H CIRCUIT**

This section is dedicated to the design of a programmable switched-current S/H circuit for 20MHz sampling rate applications. The programmability has been implemented using the MOCD structure. The programmable S/H circuit is depicted in Fig. 4.2. The circuit is designed for 1% settling error and 10MHz cutoff frequency. The design parameters are given in Table 4.1.

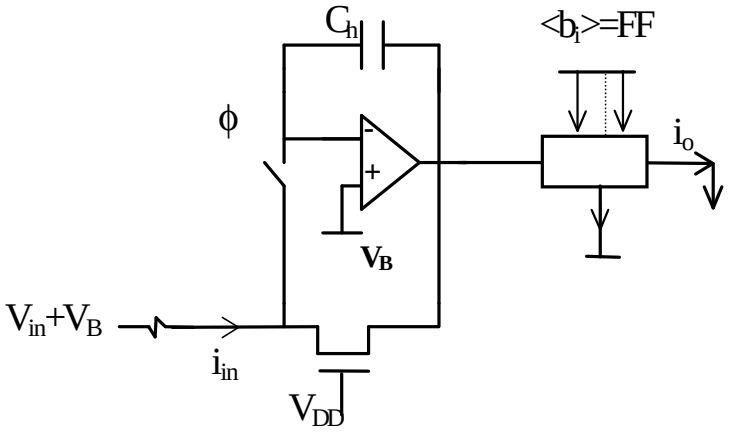


Fig. 4.2. Digitally programmable sampled-hold.

Table 4.1. Parameters of the sample-hold circuit.

(W/L) of any transistor of the MOCD	6μm/2.5μm	
Holding capacitor	0.5pF	$\sqrt{\frac{kT}{C}} \cong 91\mu V$.
(W/L) of nMOST switch	3μm/0.8μm	
Op-amp bandwidth	100MHz	
G_m(OTA)	55mA/V	Open loop gain >40dB

- **VERIFICATION**

To verify our design, the S/H circuit shown in Fig. 4.2 has been simulated using T-Spice [49]. The step and sinusoidal responses are shown in Fig. 4.3 and Fig. 4.4, respectively. Fig.4.3 shows that the output settles within 1% after 24ns from clock transition. In Fig. 4.4, the input noise is due to switch ϕ in Fig. 4.2. In Figs 4.3 and 4.4, the inputs are the current response of step and sinusoidal input voltages, respectively. Fig. 4.3 is simulated with typical MOSFET parameter. To study the effect of MOSFET parameter variation, the circuit must be simulated with fast and slow MOSFET parameter.

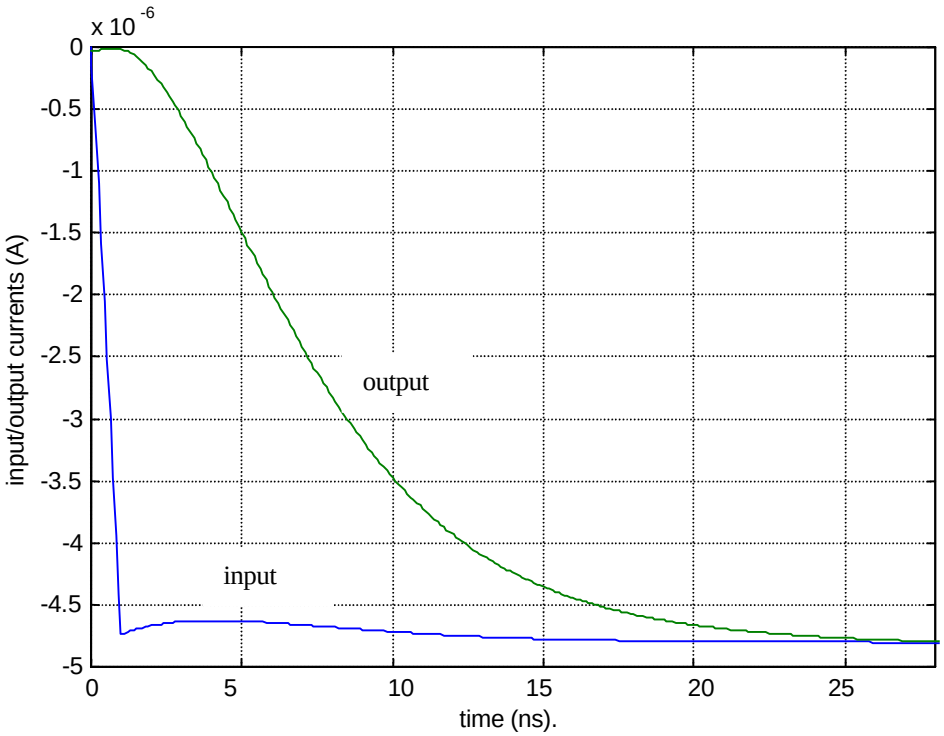


Fig. 4.3. The step response of the sample-hold circuit.

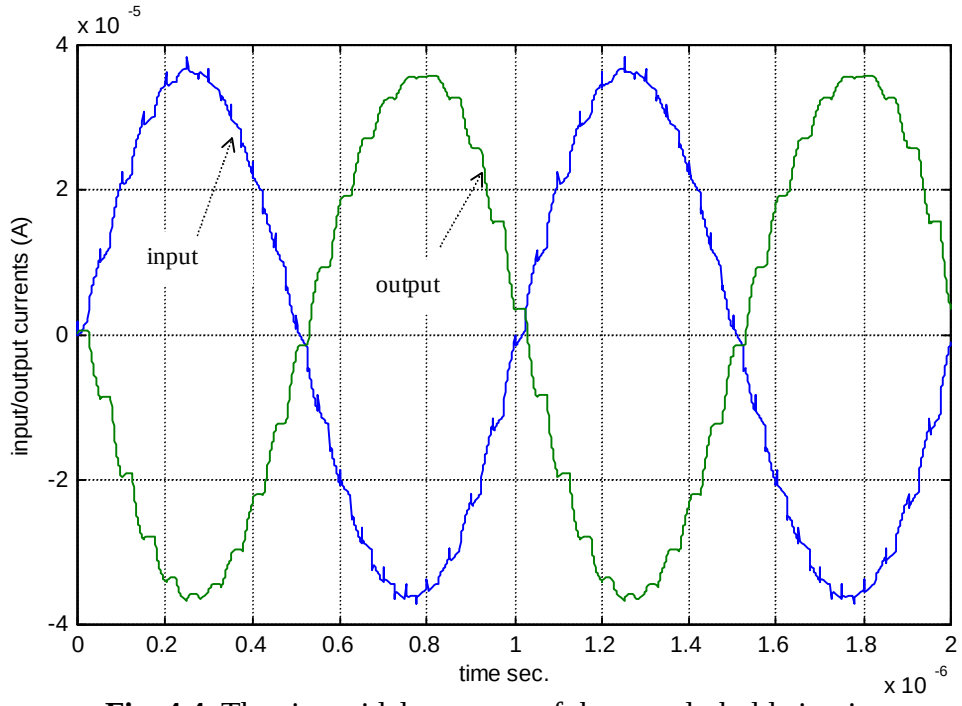


Fig. 4.4. The sinusoidal response of the sample-hold circuit.

4.3 A FULLY BALANCED SWITCHED-CURRENT SAMPLE-HOLD CIRCUIT

Fully Balanced Circuits (FBCs) are widely used in analog-signal-processing applications because they ensure high power supply rejection, improve linearity and increase the dynamic range. Also, in sampled-data circuit (switched-capacitor or switched-current), FBC reduce the effects of charge injection.

In this section, we propose a fully balanced switched-current sample-hold circuit based on the switched-current technique described in [21], which is appropriate for low voltage operation. The programmability of the sample-hold circuit is achieved via the MOSFET Only Current Division (MOCD) technique [33]. Also, we present a new method for the sign-bit realization using the two output currents of the MOCD.

4.3.1 FULLY BALANCED OP-AMP DESIGN

The block diagrams of a single-ended op-amp and a fully balanced one are shown in Fig. 4.5. In fully differential balanced circuits one major problem must be overcome. Because the signals are no longer referred to ground, as in a single-ended circuit, the operating point of the amplifier is not well defined. A Common Mode Feedback Loop (CMFB) block has to be added as shown in Fig. 4.5. (b).

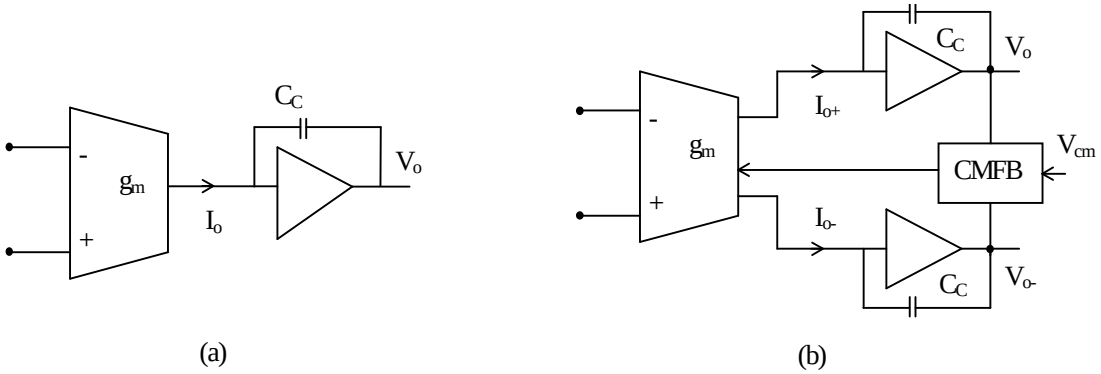


Fig. 4.5. Block diagram of op-amps.

(a) Single-ended.

(b) Fully balanced.

In the switched-current method [21], the MOS transistor is used as a feedback nonlinear resistor as illustrated in Fig.4.6. (a). The common-mode voltage detector is composed of the transistors M_3 and M_4 and operates as follows. Assume the two pairs of transistors (M_1-M_2 and M_3-M_4) to be matched and the input currents (I and –I) to be equal and opposite. The series connected transistors M_3-M_4 ensure that the current through them is the same. The values V_o^+ and V_o^- are generated by equal input currents. Therefore, the value of V_y is equal to V_{CM} since the current through M_3 is the same as the one through M_4.

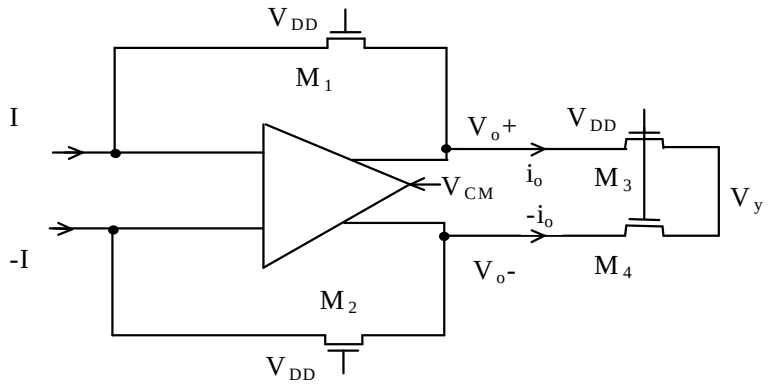


Fig. 4.6. Circuit used to detect the common-mode input voltage.

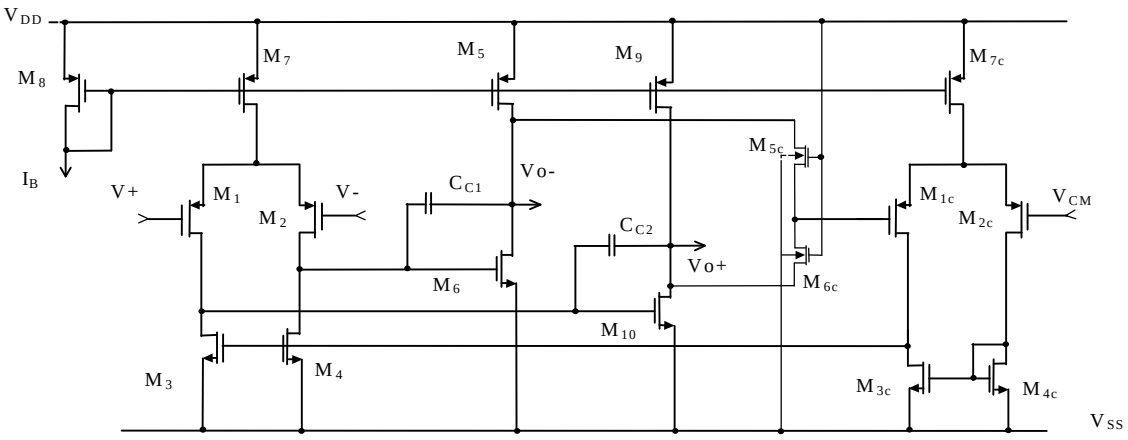


Fig. 4.7. Fully balanced op-amp schematic.

For the SI method [21], at 20 MHz clock, the op-amp specifications can be as those illustrated in Table 4.2. Transistor dimensions and bias currents are calculated using the methodology shown in Appendix B. The design parameters are shown in Table 4.3. The design results are presented in Table 4.4. The op-amp in column 2 is a buffer for a 20pF load. The op-amp illustrated in Fig. 4.7 has been simulated using T-Spice [49]. The simulated AC and DC responses of the op-amp are shown in Fig.4.8.

Table 4.2. Specifications of the op-amp.

Parameter	Value
Supply voltage	±1.5 V
Open loop gain	>40 dB
GB(Gain Bandwidth Product)	~100 MHz
Phase Margin	>50°
Load resistance (R_L)	9 KΩ
Load capacitance (C_L)	2 pF

Table 4.3. Design parameters of the op-amp and simulated specifications.

C_c =0.5pF	P2/GB =5
g_{mI}= 315µA/V	g_{mII}=6.3µA/V
I_{SQN}= 36 nA	I_{SQP}=12 nA
K_p= 35 µA/V^2	K_n= 95 µA/V^2

Table 4.4. Channel widths and simulation results (L=2µm).

Op-amp	1	2
C_L (pF)	2	20
i_{f6}*	219	219
i_{f1}*	60	60
i_{f5}*	595	595
I_B (µA)	120	120
I_{total}(mA)	2.0	28
CEF*	36	49
$W_{1,2,1c,\ 2c}$ (µm)	150	1500
$W_{3,4}$(µm)	30	300
W_8 (µm)	30	30
$W_{7,7c}$(µm)	30	300
$W_{3c,4c}$ (µm)	30	300
$W_{5,9}$ (µm)	200	3000
$W_{6,10}$ (µm)	400	6000
$W_{5c,\ 6c}$ (µm)/L(µm)	5/5	5/5
A_o (dB)	62	75
GB (M Hz)	99	97
Phase margin	54°	50°
C_c	0.5pF	5pF

- I_{norml}=57.8 µA (GB ≅100M Hz, C_L=2pF and i_f =3)

* The definitions are in Appendix A

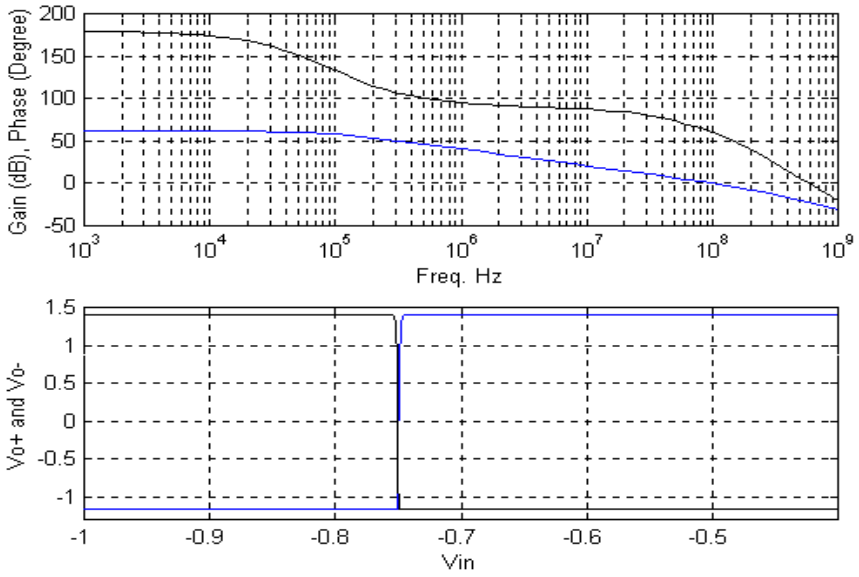


Fig. 4.8. The frequency and DC responses of the balanced op-amp.

4.3.2 FULLY BALANCED SI SAMPLE-HOLD CIRCUIT ARCHITECTURE

A fully balanced switched-current block has been designed using the same thoughtway of the methodology in [21]. The proposed fully balanced (FB) sample-hold is shown in Fig. 4.9. In this circuit, the currents (I and -I) are processed in two steps:

- Track mode: the input currents are fed to the cell when both switches are closed. The currents are memorized as voltages across the holding capacitors. It should be emphasized that linear capacitors are not needed to store the data.
- Hold mode: when the switches open, the voltages are held on the capacitors. These voltages maintain the output currents equal in magnitude and opposite to the input currents as long as M_1 and M_2 have the same aspect ratios.

In the SI structure shown in Fig. 4.9, all the switches operate at a constant DC voltage, equal to V_{CM}, thus causing both the charge injection and settling time [50] to be signal-independent. Moreover, if a proper biasing circuit as the one shown in [21] is used to generate V_{CM}, the gap of the switches [8, 10] is avoided.

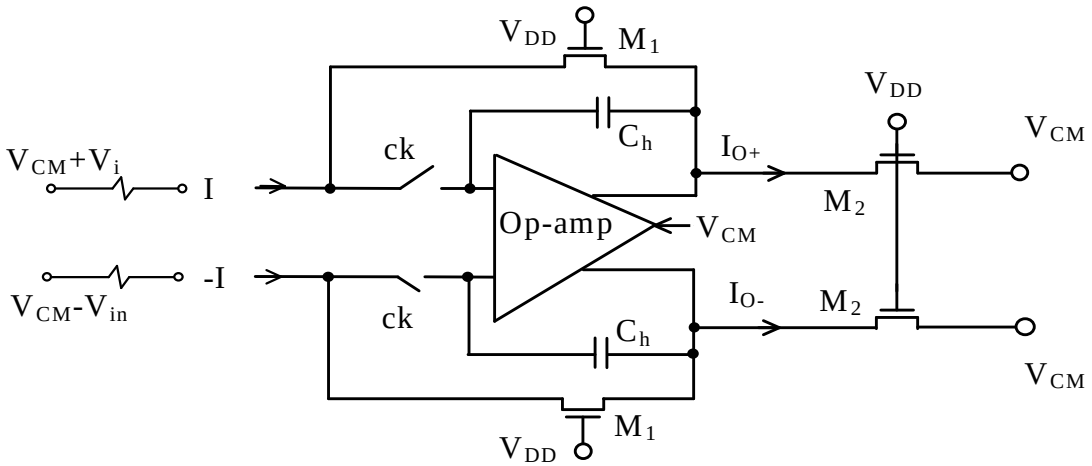


Fig. 4.9. Fully balanced sample-hold circuit.

The circuit shown in Fig.4.9 has been simulated for 3µm/0.8µm nMOS switches, aspect ratios of M_1 and M_2 equal to 6µm/5µm and 0.5pF holding capacitors. Linear resistors are used to convert the input voltages to currents. The responses of the fully balanced SI sample-hold circuit to both sinusoidal and step inputs are shown in Fig.4.10. The simulation shows that the circuit has 1% settling time around 24nsec.

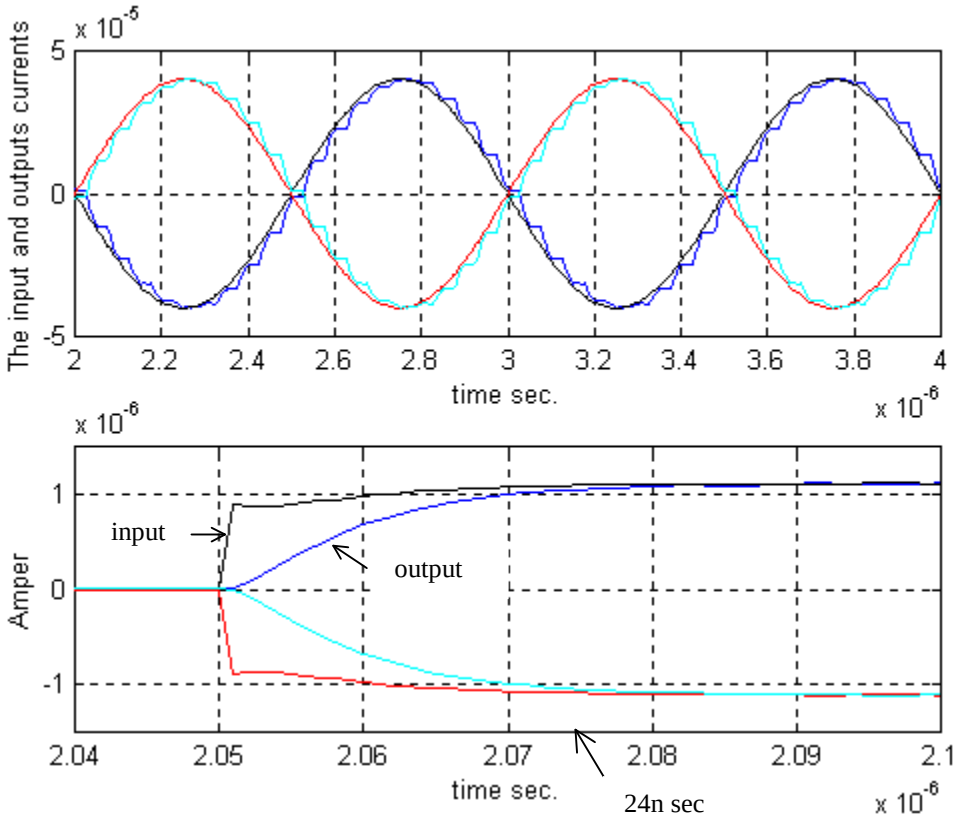


Fig. 4.10. The sinusoidal and step responses of the sample-hold in Fig. 4.9.

4.3.3 SIGN-BIT REALIZATION

The sign-bit realization in [51] is achieved by adding an extra transistor to the MOCD input as shown in Fig. 4.11. This method is based on connecting the MOCD input either to +I or –I, thus changing the direction of the output current to obtain the plus or minus sign. Consequently, all internal potentials of the MOCD change at each

sign-bit variation. Thus, the settling time of the MOCD can affect the maximum allowable clock frequency.

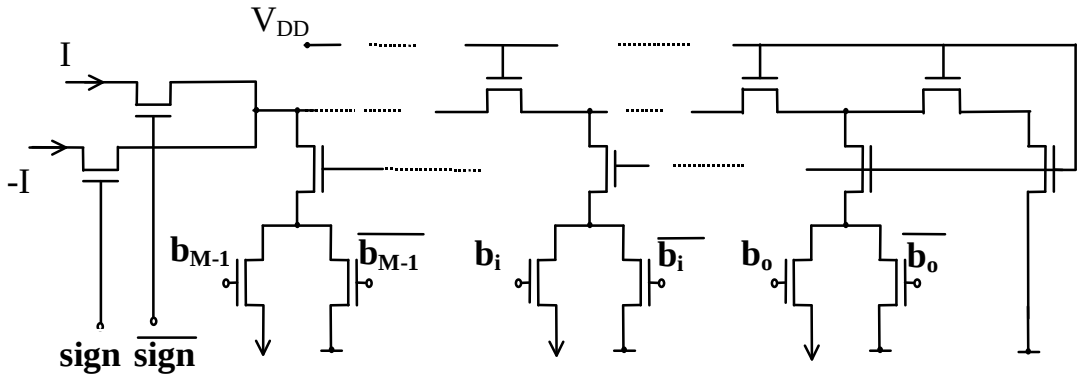


Fig. 4.11. The sign-bit implementation using two MOCD inputs [51].

Here, we propose a new method for the sign-bit realization. This method is suitable for fully balanced circuit where the positive and negative signals are available. The new method uses the two output currents of the MOCD by adding the SUM current of one MOCD to the DUMP current of the other one, as shown in Fig. 4.12. The positive output current I_{o+} is

$$I_{o+} = (2a-1)I = \beta I \tag{4.8}$$

The attenuation factor (a) changes from zero to one when the digital word (<bi>) is changed from 00 to FF (8-bit MOCD). The variation of the coefficient (β) against the control digital word can be represented as in Fig. 4.12. This method avoids the switching method in [51] and no additional circuitry is needed. Moreover, the internal voltages are kept constant when the sign-bit changes. Thus the proposed method is faster than the method that has been used in [51].

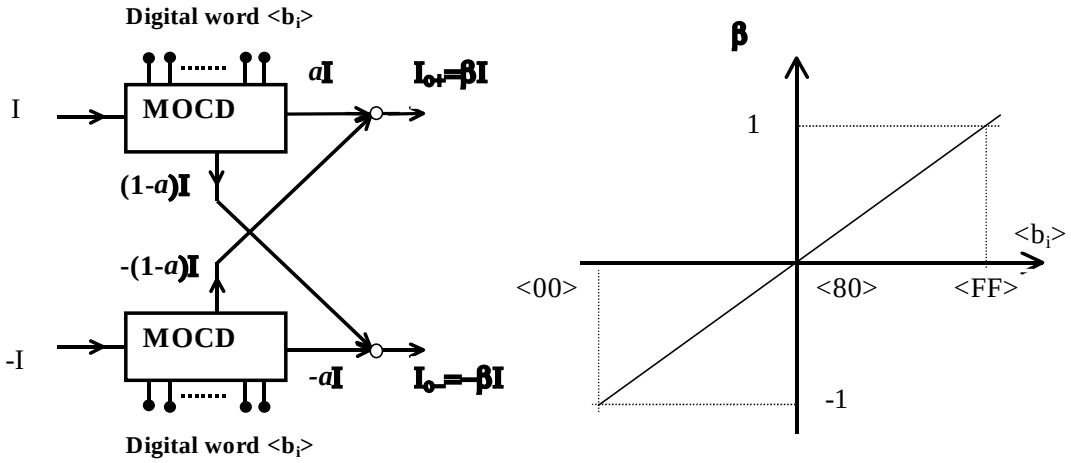


Fig. 4.12. Proposed method for sign-bit realization.

4.3.4 PROGRAMMABLE FULLY BALANCED SAMPLE-HOLD

Using the circuits proposed in sections 4.3.2 and 4.3.3, a fully programmable balanced SI S/H circuit has been implemented. 8-bit MOCDs have been used. The complete circuit has been simulated with 3μm/0.8μm nMOS switches, the aspect ratio of the transistors equal to 6μm/5μm, 0.5pF holding capacitors and 6μm/2.5μm unit transistor of the MOCD. The strategy for the realization of sign-bit has been tested as shown in Fig. 4.13. The top figure of (4.13) shows the sign-bit while the other MOCD bits are 1000000 (<40>). Thus the attenuation factor is ±0.5 as shown in the two bottom curves. Fig. 4.13 displays the expected behavior.

4.4 INTERFACE BLOCKS

The general block diagram of a current-mode signal processing is depicted in Fig. 4.14. The input and output blocks are interfaces between the core section (current-mode) and the surrounding voltage-mode circuit. Moreover, single-to-balanced and balanced-to-single-ended sections are necessary to interface a balanced circuit to a single-ended one.

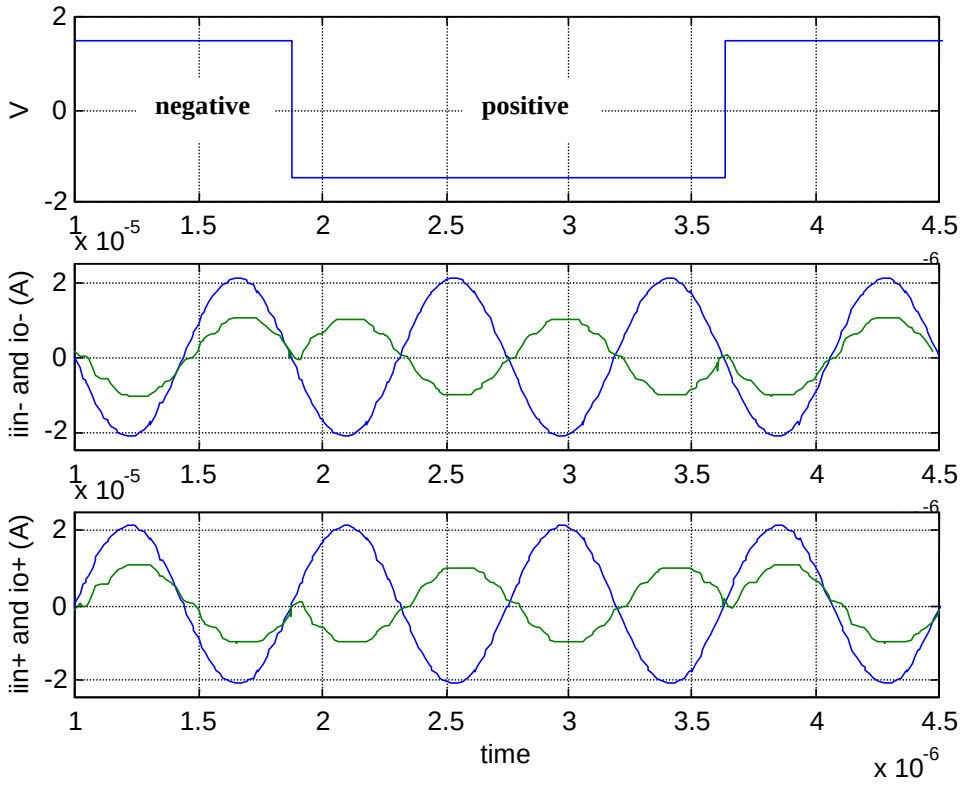


Fig. 4.13. The time response of the programmable SI sample-hold circuit.

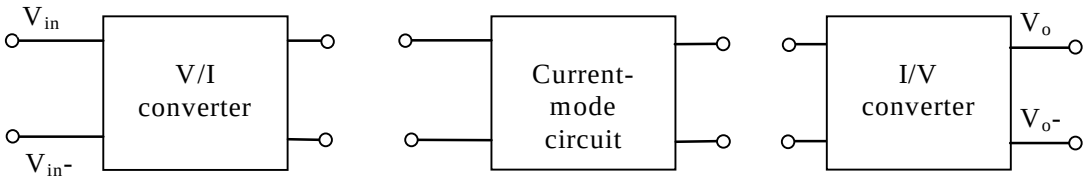


Fig. 4.14. Block diagram for current-mode signal processing.

Fully balanced switched-current circuits often need other auxiliary blocks to interface the current-mode and the voltage-mode circuits. Generally, in fully balanced circuit, the first block is a single-ended input to balanced output block. After that, this voltage signal must be converted to current.

4.4.1 SINGLE-ENDED INPUT TO BALANCED-OUTPUT CONVERTER

In the technical literature, there are some circuits [52, 53] for single-ended to balanced conversion. In this work, the circuit shown in Fig. 4.15 is used to implement

the single-ended to balanced converter [52]. Table 4.5 presents the dimension of the MOS transistors in Fig. 4.15. Fig. 4.16 shows the frequency and DC responses. The 3 dB cutoff frequency is around 10 MHz.

Table 4.5. Channel widths (L=3μm).

$M_1, M_2, M_7, M_8, M_9, M_{11}, M_{12}, M_{13}, M_{b2}$	*4*μm
M_3, M_4, M_{b3}	*8*μm
M_6, M_5, M_{10}, M_{b1}	*20*μm
Total current	*72μA*

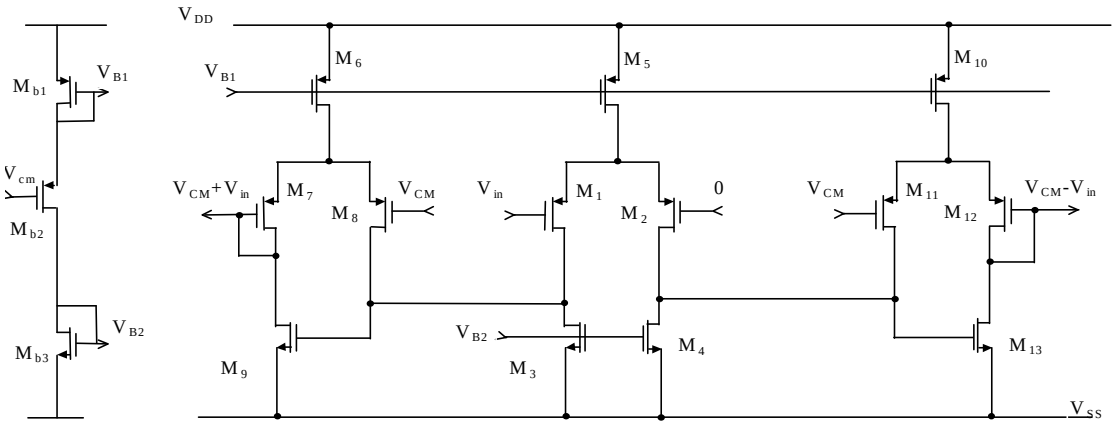


Fig. 4.15. Differential-input to balanced-output converter [52].

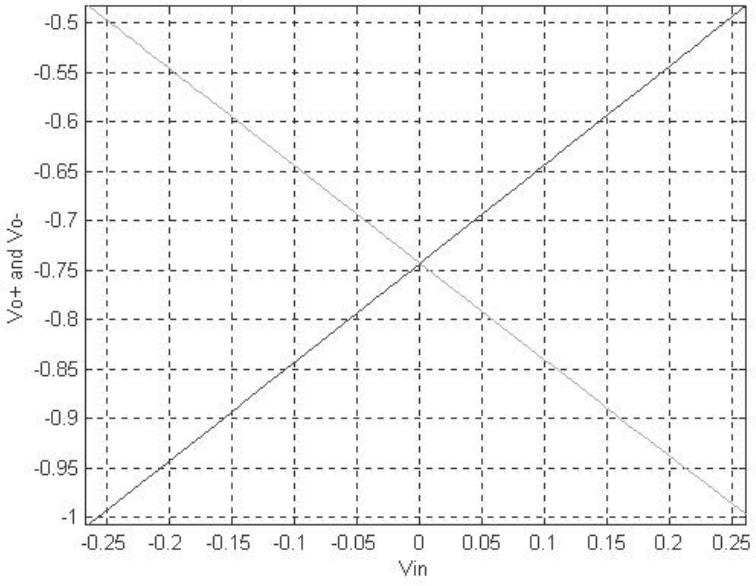


Fig. 4.16.(a). The DC response of the circuit shown in Fig. 4.15.

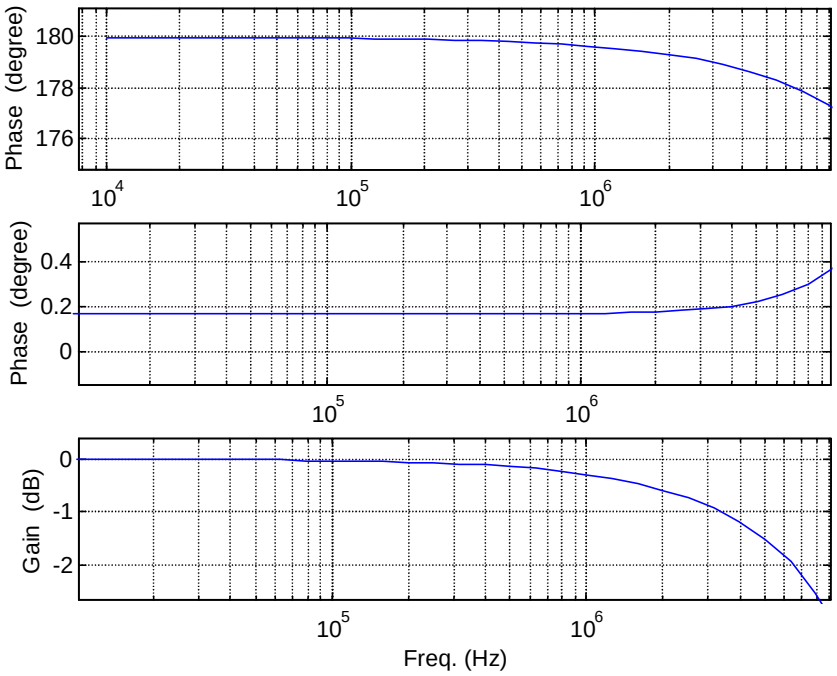


Fig. 4.16.(b). The frequency response of the circuit shown in Fig. 4.15.

4.4.2 VOLTAGE-TO-CURRENT AND CURRENT-TO-VOLTAGE CONVERTERS

In this work, polysilicon resistors (R) are used to perform the linear voltage to current and current to voltage converters, as shown in Fig. 4.17

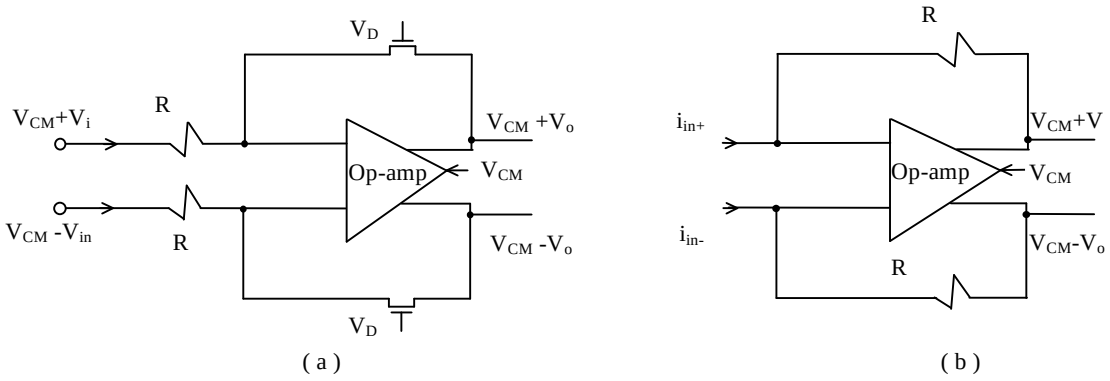


Fig. 4.17. (a) V/I converter. (b) I/V converter.