CHAPTER 1

LOW-VOLTAGE ANALOG DESIGN

1.1 INTRODUCTION

Recently, the power supply voltage for many commercial very large scale integrated (VLSI) circuits has been decreased to 3V and will continue to decrease to further lower levels. This trend [1, 2] is driven by three main factors :

- The scaling of VLSI technologies (deep-submicron).
- Power management in large VLSI chips.
- Increased market demands for mobile or portable battery-operated products.

These factors are technology, design and market-driven respectively, and as such seem independent of one another. However, they are to a large extent interrelated.

Obviously, minimum feature sizes are scaled down in three dimensions. At the present time, VLSI technologies are characterized by channel lengths in the range from 0.5μm to 0.25μm. By convention the channel length of the MOS transistors is used as the reference length. Scaling is one effective method of reducing the cost of IC products, i.e. more components are integrated on a single chip with roughly the same effort and cost. In addition, smaller geometry, in general, lowers the parasitic capacitances and increases transconductance in MOS devices, yielding higher-speed circuits. However, scaling inevitably results in thinner MOS gate oxide. Hence, scaled down devices are subject to breakdown at relatively low voltages because of the increase in electric field. Therefore, the reduction of the supply voltage is necessary.

With the reduction of the supply voltage, analog designers are faced with new problems in circuit design. Key design issues in low supply voltage must be addressed to maintain the same system performance achieved with relatively high supply voltage. Actually, in analog circuit design, supply voltage reduction is a primary factor of circuit modifications.

The design at low supply voltages is particularly harder in mixed mode VLSI signal processing systems [3, 4], in which analog and digital circuits are integrated on a single chip. The electrical parameters of transistors are optimized for digital circuits due to the fact that they usually account for the majority of the total chip area. For instance, as the technological process scales down, the MOSFET threshold voltage remains about the same. The reduction of the threshold voltage that would be necessary for analog circuits usually produces two negative effects on digital circuits, the reduction of noise margin and high leakage currents. Of course it might be possible to use multi-threshold voltage process technology in which a high threshold voltage can be used for digital circuits and a low threshold voltage can be used for analog circuits (continuous-time and sampled-data circuits) [5]. This solution, however, increases the cost of IC products.

Digital circuits do not suffer significantly under low voltage conditions and can perform well with slight modifications, while new analog techniques for low voltage circuits must be developed. Furthermore, in digital design lowering the supply voltage implies in lower power consumption whereas in analog design a lower supply is not a necessary neither sufficient condition for low power. In fact, lowering the supply may or may not reduce power consumption depending on whether certain design changes are made to maintain or restore the analog performance at acceptable levels. In analog circuit, the power consumption per pole is in a crude approximation proportional to the dynamic range (DR) [6, 7, 8]:

$$P = \eta kTf_o(DR) \tag{1.1}$$

where DR is defined as the ratio of the mean square value of the signal to the mean square value of the noise, f_o is the filter pole frequency, η is a dimensionless factor depending on the implementation of the filter and kT is the thermal energy. Equation (1.1) is derived neglecting the bias currents of the amplifiers, assuming a pure capacitive load C and that the only contribution to noise is thermal noise. Here, we consider the mean square voltage noise at the load to be equal to kT/C. Consequently, to keep the same DR, the load capacitor should be scaled up with the square of the supply voltage scaling factor. In this idealized situation, for a given dynamic range, the power consumption is independent of the supply voltage. In practice, however, power dissipation is generally dominated by the static dissipation of the amplifier. As shown in [9], to keep the same circuit performance (signal-to-noise ratio and bandwidth), the static power consumption is increased for lower supply voltages.

In this chapter, we will review some key limitations in analog circuit design at low-voltage power supply. Some solutions based on both integrated circuit technologies and circuit design strategies are mentioned.

1.2 LIMITATIONS OF LOW-VOLTAGE OPERATION

The operational amplifier is a widely used building block in analog circuits. The power supply voltage must be higher than a minimum value to allow for correct operation of the amplifier. Fig.1.1 shows the most simple input and output stages of operational amplifiers. For the input, the maximum bias voltage V_B is around V_{DD}-(V_{Top}+V_{DSsat}). Another boundary is set by the output stage; the minimum supply voltage [10] is approximated as

$$V_{DD,\,min} \cong V_{DSsat,n} + V_{swing} + V_{DSsat,p} \tag{1.2}$$

Consequently, low supply voltage causes directly shrinking of both the voltage swing and the dynamic range.

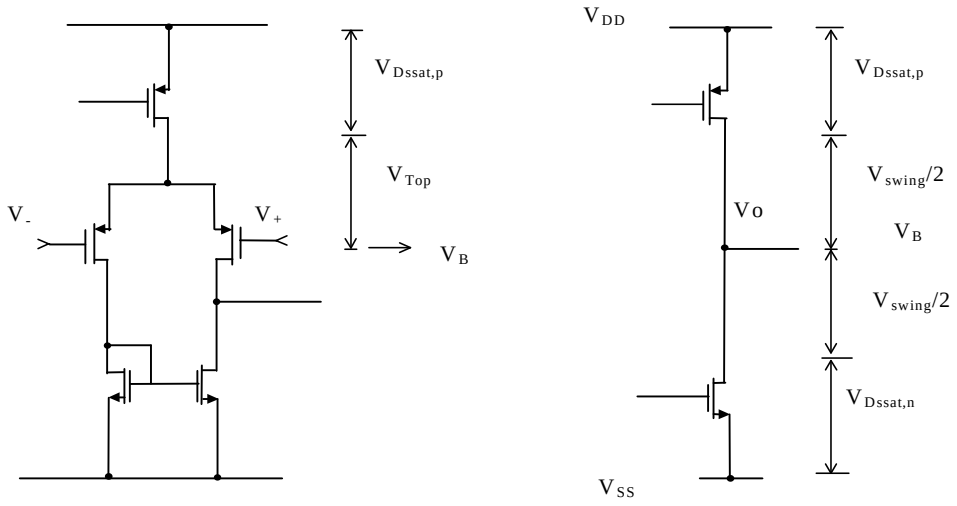


Fig. 1.1. The common-mode input range and output range of an op-amp.

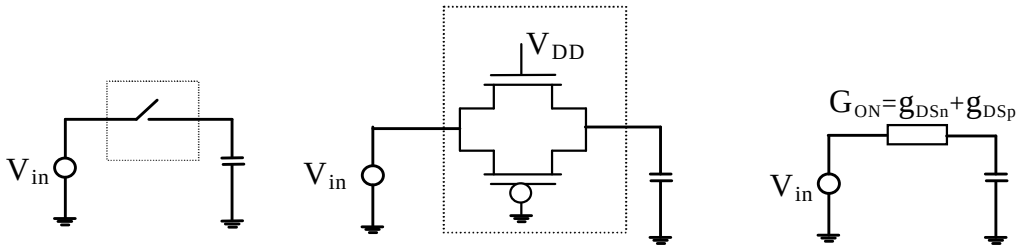
Another problem that must be faced at low-voltage is related to the switch. The complementary MOS switch has been largely employed in sampled-data (switched-capacitor (SC) and switched-current) circuits. Fig. 1.2 shows an S/H circuit. Around $V_S=V_D=V_{in,}$ in strong inversion (see Appendix A),

$$g_{DSn} = \mu_n C_{ox}^{'} \frac{W}{L}(V_{DD} - V_{Ton} - nV_{in}) \tag{1.3}$$

The expression for the conductance g_{DSp} of the p-channel transistor is similar to (1.3).

The switch conductance is dependent of both the supply voltage and the input signal. Fig. 1.3 illustrates the rail-to-rail operation of the CMOS switch. Note the dependence of the total switch conductance ($G_{on}=g_{DSn}+g_{DSp}$) on the input signal. Reducing the supply voltage reduces the overdrive voltage of the MOS switches. Consequently, the overlapping conduction range of the nMOS and the pMOS devices is reduced. When

the supply voltage reaches $(V_{Ton}+|V_{Top}|)/(2-n)$, the on-resistance becomes very large and the rail-to-rail operation is not practical any more. In conclusion, the conduction gap is one of the most significant obstacles for low-voltage operation in sampled-data circuits.



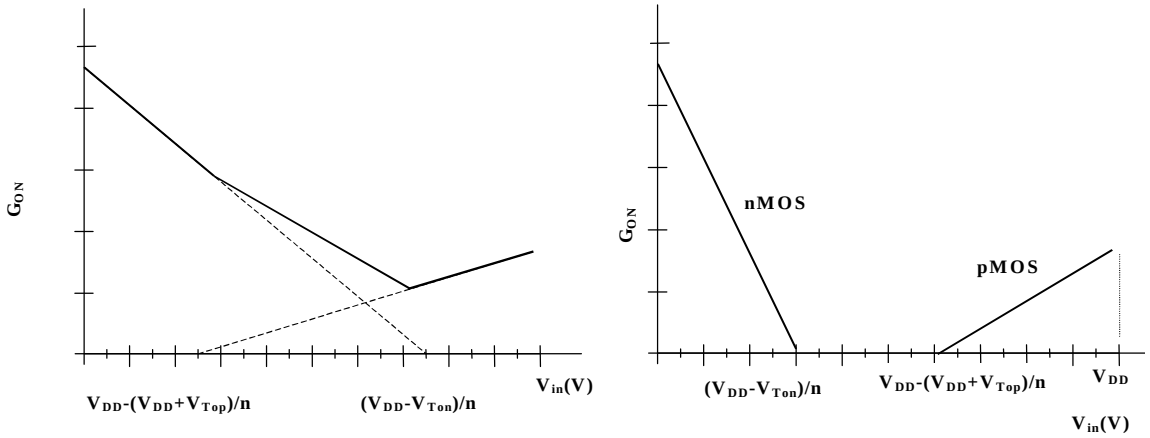
(a) **(b)** **(c)**

Fig.1.2. The sample-hold circuit.

(a) Basic sample-hold scheme.

(b) Basic sample-hold and the CMOS switch.

(c) Basic sample-hold and the on-conductance of the CMOS switch.



V_{DD} =5V V_{DD}=1.5 V

Fig.1.3. On-conductance of a CMOS switch for V_{DD}=5V and 1.5V.

1.3 LOW-VOLTAGE CIRCUIT DESIGN TECHNIQUES

In this section, we describe two existing solutions that allow for low-voltage operation of CMOS switches. The first is based on a special multi-threshold process, and the second is based on circuit design techniques.

1.3.1 TECHNOLOGY CONSIDERATIONS FOR LOW-VOLTAGE ANALOG CIRCUITS

As mentioned above, low supply voltage has generated design problems such as reduction of the dynamic range and the difficulty of turning on the CMOS/MOS switches over the entire voltage swing. From the technology side, special techniques to overcome these problems exist. One is enlarging V_{swing} by using a dedicated process, which has a special low V_T nMOS transistor [11, 12]. In [11] an extra nMOS transistor with V_{Ton} =0.2V is used as a switch, which allows a 1V voltage swing from 1.4V power supply.

A less expensive alternative is to use a technology that provides unimplanted devices. In this technology, a low threshold nMOS is realized by a shielding technique [8]. The resulting nMOS device has a typical threshold of 300mV with a relatively small body effect. Other possible solution is the use of bipolar devices of BiCMOS technology [13, 14].

Technology solutions to solve problems of low-voltage circuits are expensive. Thus, circuit designers have developed solutions based on the circuit art that will be reviewed in the next section.

1.3.2 DESIGN STRATEGY FOR LOW-VOLTAGE CIRCUITS

Analog circuit designers have introduced circuit cells appropriate for low-voltage operation [10, 15] to avoid the expensive multi-threshold technique. A general guideline for the design of high gain amplifiers at low-voltage is the use of multistage cascade structures instead of stacked transistors. Moreover, for large voltage swing, the output stage must achieve rail-to-rail swing. Details about low-voltage op-amp design can be found in [8, 16].

This work concentrates on circuit techniques that circumvent the problem of the conduction gap of the switches. One manner to overcome the switch gap problem is the clock multiplication technique [17]. In this method, a higher voltage for driving the critical switches (switches connected to non-constant voltage) is generated on-chip from the low power supply. This technique generates problems such as the possibility to create latch-up. Furthermore, the use of higher voltages is not allowed anymore in advanced sub-micron CMOS technologies due to reliability considerations [10].

Another approach to allow for proper operation of switches in low-voltage SC circuits is the switched-opamp technique [10, 18]. In this technique, the critical switch is eliminated, and its function is realized by turning on and off the operational amplifier attached to this switch. Fig.1.4 shows the conventional SC circuit and the switched op-amp equivalent circuit. This technique is based on the switched op-amp output to be in a high impedance state during the low state of the clock, as shown in Fig. 1.4 (c).

In the switched-opamp technique, the maximum sampling frequency is limited by the time necessary to turn on and off the op-amp which is limited to a few hundred kHz [8]. The seminal switched op-amp technique described in [10] has been slightly modified in [18] to allow rail-to-rail output swing.

From the discussion above, the ideal solution to the conduction gap is that all switches operate at a constant voltage level that is out of the conduction gap.

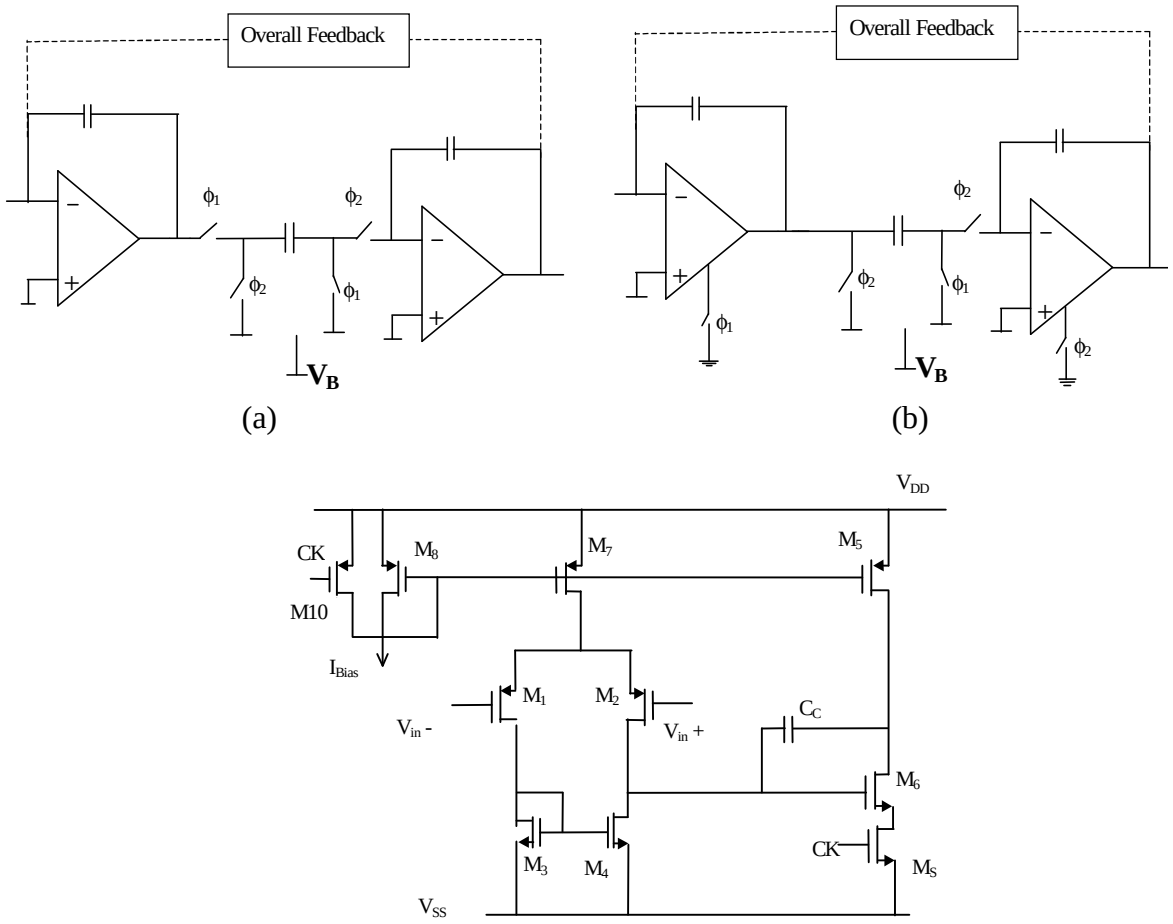


Fig.1.4. Switched-opamp technique [10].

(a) Conventional SC integrator.

(b) Switched-opamp equivalent SC circuit.

(c) Switched-opamp.