Inverter-Based Switched Current Circuit for Very Low-Voltage and Low-Power Applications

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Abstract -- **In this paper, a new sample-and-hold (S/H) circuit for low-voltage and low-power CMOS analog design is proposed. The circuit is based on the conventional CMOS inverter operating as a transconductor. The proposed circuit does not require linear capacitors and employs switches that operate at fixed channel voltage. Owing to the use of inverters, the proposed structure presents class-AB operation. A S/H circuit has been designed in a standard 0.35-μm CMOS technology at 0.6V supply. The S/H cell operating at a clock frequency of 10 kHz consumes 30 nW and presents a dynamic range of approximately 60 dB.**

I. Introduction

Despite an increasing number of very low voltage/power applications [1], a few number of real low-voltage and low-power analog circuits has been demonstrated [2,3]. Current-mode signal processing circuits have been used for low supply voltage operation, because the voltage range is compressed through either square root or logarithm functions of the input signal. Therefore, the switched-current (SI) technique [4], has been considered as an analog sample-data circuit implementation for low voltage supply. However, in sampled-data circuits (switched-capacitor or switched-current), the conduction gap [5] of the switches presents a major significant obstacle at low power supply. In the conventional SI technique [4] shown in Fig. 1(a), the switch voltage is signal dependent. Thus, similarly to the conventional switched-capacitor (SC) technique, conventional SI circuits suffer from the conduction gap of the switches. The switched-opamp technique [5] has been developed to overcome this problem in the SC technique. This technique, however, limits the speed of the circuit dramatically due to turning on/off of the operational amplifiers. A new SC technique recently published [6] for low-voltage and high speed has no signal-dependent switches; however, as in the conventional SC techniques, it requires op-amps and linear capacitors. Another sampled-data technique is known as Switched- MOSFET (SM) [7,8]. As shown in the basic sample-and-hold (S/H) of the SM technique of Fig.1 (b), the channel of the switch operates at a fixed voltage V_B while the operational amplifier drives transistors operating in the linear region. The need for operational amplifiers precludes the use of SM circuits for very low-power applications.

This paper presents a new topology of sampled data circuits for low-voltage and low-power applications. To reduce supply voltage requirement and power consumption, a minimalist design style based on inverters and switches is proposed. In the new circuit, the switches operate at fixed channel voltage, which improves the accuracy of the proposed cell. Moreover, the core cell consumes low power due to class-AB operation. The paper is organized as follows. Section II describes the SI and SM techniques. The new S/H circuit is described in Section III. The simulation results are shown in Section IV. Concluding remarks are drawn in Section V.

II. SI and SM techniques

Both S/H circuits shown in Fig. 1 operate as current mirrors when the switches are closed. In Fig. 1 (b), assuming the op-amp to be ideal, transistors M_1 and M_2 are both biased with the same set of voltages. Therefore, neglecting transistor mismatch, the output current I_0 is an inverted replica of the input current I_{in}.

In the track mode of both circuits, the input current is fed to the cell. The current is memorized as a voltage across the holding capacitor. In the hold mode, the switch opens and the voltage is held on the capacitor. The output current is equal to its value on the previous clock phase.

The proper operation of the current mirror in Fig. 1(a) requires the transistors to operate in saturation while the transistors in Fig. 1(b) have to operate in the triode region.

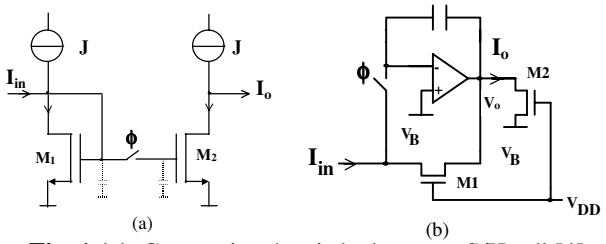

Fig. 1 (a). Conventional switched-current S/H cell [4].
(b). Switched-MOSFET S/H circuit [7,8].

III. The Switched-Inverter (S-Inv) Circuit

The S/H circuit consists of 4 identical CMOS inverters, a holding capacitor, and a switch as shown in Fig.2. A CMOS inverter is the simplest possible implementation of a transconductor. The dotted inverters provide non-inverted or inverted replicas of the input current. The holding capacitor is not required to be linear.

1. Switched Inverter Basic Cell.

The S/H circuit operates as follows.

- Sample mode - After the switch has been closed, the input of Inv-4 is charged to a voltage v_{g2} such that the difference between the currents flowing through the n-channel and p-channel transistors in Inv-4 equals the input current. The intermediate inverters (Inv-2 and Inv-3) compose an inverting unity gain amplifier, as shown in Fig. 3. In effect, because the current "I" flowing out of transconductor (inv-2) is flowing into transconductor (inv-3), v_{g2}=-v_{g1} must follow. The input current is memorized as a voltage across the holding capacitor C_h. The high transconductance of the complete cell, given by -$g_{m4}A_{V1}$ (g_{m4} is the transconductance of Inv-4 while A_{V1} is the voltage gain of Inv-1), ensures an almost constant input voltage for the S/H cell, which is equal to the threshold voltage (V_B) of the inverter.
- Hold mode – When the switch opens, the voltage held on the capacitor keeps v_{g1} and v_{g2} constant. The inputs of the dotted inverters are v_{g1} and v_{g2}; therefore, as long as the outputs of the dotted inverters ensure saturation of the transistors, the output currents I_{o1} and I_{o2} are non-inverted and inverted copies of I_{in}.

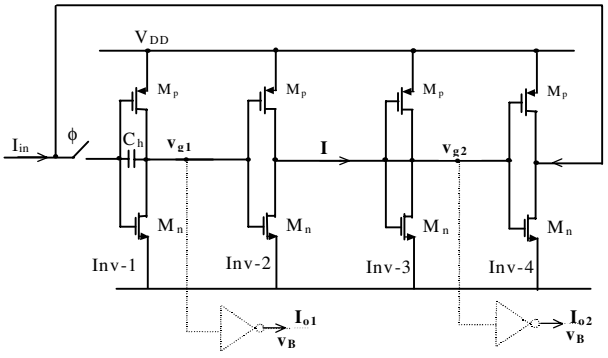

Fig. 2. Sample and hold circuit of S-Inv technique.

Since the channel voltage of the switch is fixed to V_B, both charge injection and settling time are signal-independent, which reduces the sampling error. The dimensions of the inverters can be mask-programmed to allow for programmability of the S-Inv cells.

The ac analysis of the circuit in Fig. 2 leads to the transfer function of the cell, which can be approximated to a single-pole transfer function as:

$$\frac{I_{o2}(s)}{I_{in}(s)} \cong -\frac{1}{1+\frac{s}{A_V p_1}} \qquad (1)$$

with $p_1 = g_{04}/A_{V1}C_h$,and $A_V = \frac{g_{m1}g_{m4}}{g_{o1}g_{o4}}$. The 1% settling time of the S/H cell is equal to $4.6*C_h/g_{m4}$.

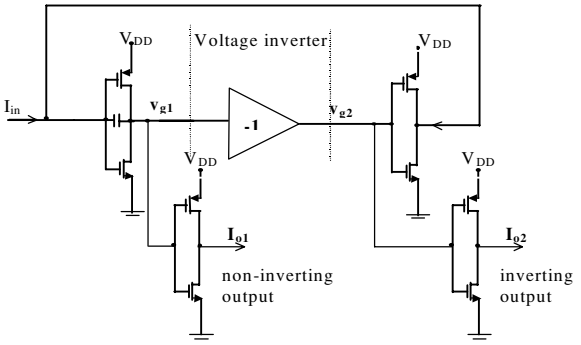

Fig. 3. The S-Inv at sampling mode.

2. First Generation Integrator

The S-Inv integrator is realized using two cascaded S/H circuits. as shown in Fig. 4. The z-domain transfer function at ϕ_1 is:

$$H_1(z) = \frac{I_{o1}}{I_{in}} = \frac{1}{1-\beta Z^{-1}} \qquad (2)$$

while at ϕ_2 is :

$$H_2(z) = \frac{I_{o2}}{I_{in}} = -\frac{Z^{-1/2}}{1-\beta Z^{-1}} \qquad (3)$$

β represents the width of the inverter labeled β normalized to the width of the remaining inverters (β<1).

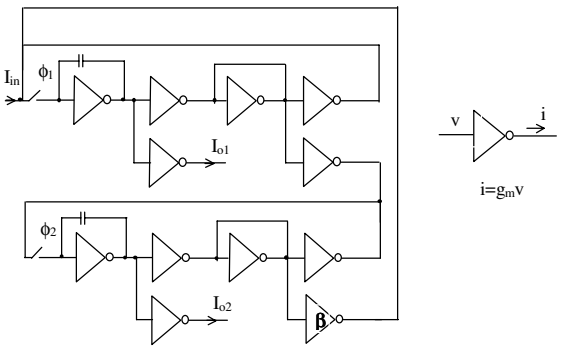

Fig. 4. The S-inv lossy integrator.

IV. Circuit Design and Simulation

The proposed S/H circuit has been designed with MOSFET parameters of the TSMC 0.35-μm CMOS technology. The transistors operate in weak inversion due to very low supply voltage (V_{DD}≅V_{THn}=0.6V, V_{THp}=-0.77V). A threshold voltage mismatch factor $A_{VTn(p)}$=8.2 (14.9) mV.

µm and a current mismatch factor $A_{\beta n(p)}$=0.2% (0.4%) µm have been considered for circuit design. The mismatch model [9] has been used to determine the minimum transistor area. The dimensions 48µm/1.75µm for the n-MOS transistors and 144µm/1.75µm for the p-MOS transistors result in a 0.1% standard deviation for the inverter current. The dimensions of the CMOS switch are 0.7µm/0.35µm and 2µm/0.35µm for the n and p-channel transistors, respectively. The holding capacitor is 0.5pF. The clock frequency is 10 kHz and the amplitude is 0.9V, slightly higher than the power supply to provide an adequate switch conductance. The threshold voltage of the inverter is V_B =224mV. Fig. 5 shows the non-inverted and inverted outputs of the S/H cell for a 400nA (peak value), 0.5kHz input current. The biasing current for each inverter is around 6.5nA. The signal-to-noise-and-distortion ratio (SNDR) is shown in Fig. 6. The input for the simulation is a 156Hz current. The dynamic range is around 60dB for the inverting output, a value about 3dB better than SNDR at the non-inverting output. In a fully differential implementation, one can use the inverting output only, thus obtaining a better performance. The noise analysis of the S/H cell is presented in the Appendix.

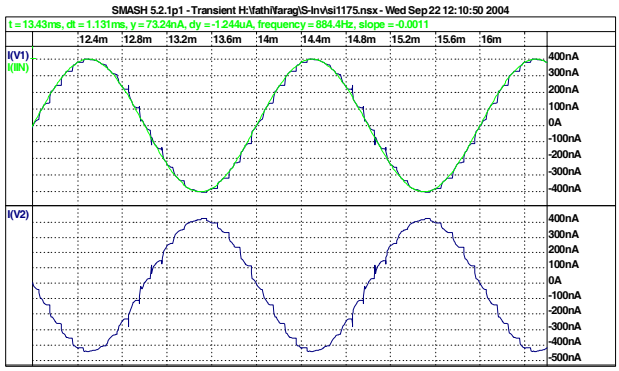

Fig. 5. Non-inverted and inverted outputs of the S/H cell.

The lossy integrator shown in Fig. 4 has been simulated for β=0.95. The theoretical unity gain frequency and low frequency gain are 1.7kHz and 26dB. The simulated frequency response of the integrator shown in Fig. 7 fits very well the theoretical calculations. The simulations have been run with SMASH.

V. Summary

A new topology for sampled data circuit named switched inverter has been introduced. The S-Inv technique has been tested for very low voltage and ultra-low power consumption. In the S-Inv technique, the switches operate at constant channel voltage, which alleviates the distortion errors due to voltage-dependent charge injection and switch conductance. The circuit has been designed and simulated by using a TSMC 0.35-µm technology with 0.6V supply voltage. The overall power consumption of the proposed S/H circuit is 30nW. The initial stage of this research has shown very encouraging results for the application of the S-Inv circuit to low-power low-voltage analog circuits.

ACKNOWLEDGMENTS

The authors wish to thank CNPq, the Brazilian Agency of Science and Technology, for the partial financial support of this work and Dolphin Integration for providing the SMASH simulator.

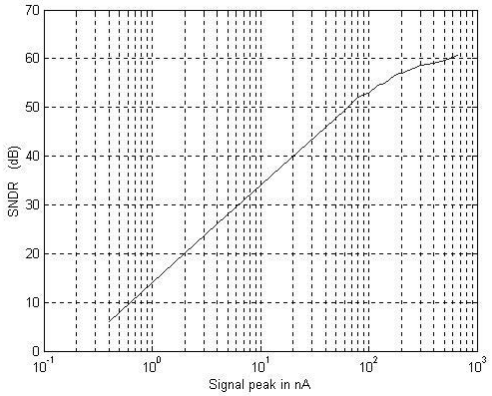

Fig.6. Simulated result of the SNDR.

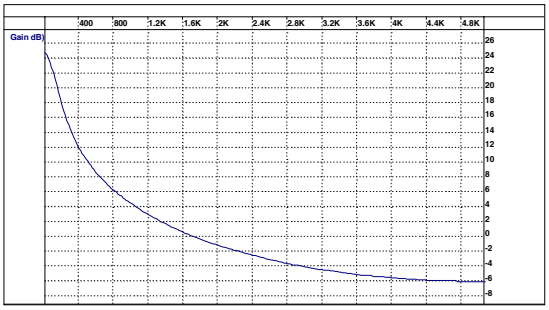

Fig. 7. Frequency response of the S-Inv integrator.

VI. References

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Appendix-A: Noise Analysis of the Sample-and-Hold Circuit

1. The CMOS Inverter

The effect of the flicker noise is much lower than the effect of the wide-band thermal noise due to aliasing. The power spectral density (PSD) of the thermal noise in an MOS transistor operating in weak inversion and saturation, can be expressed [10] as

$$S = 2qI_D \tag{A.1}$$

Fig. A.1.(b) shows the equivalent noise circuit of the CMOS inverter, where $S_{inv}=S_n+S_p$.

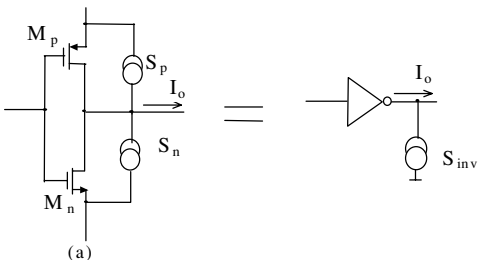

Fig.A.1. CMOS inverter and noise equivalent circuit.

The thermal PSD of a CMOS inverter in weak inversion and saturation can be written as

$$S_{inv}^{th} = 2q(I_{DN}+I_{DP}) = \begin{cases} 4qI_D & \text{for } I_o=0 \\ 2q|I_{omax}| & \text{for } I_o=\pm I_{omax} \end{cases} \tag{A.2}$$

2. Switched Inverter Circuit in Sampling Time

Fig. A.2 shows the S-Inv sample-and-hold circuit with noise sources.

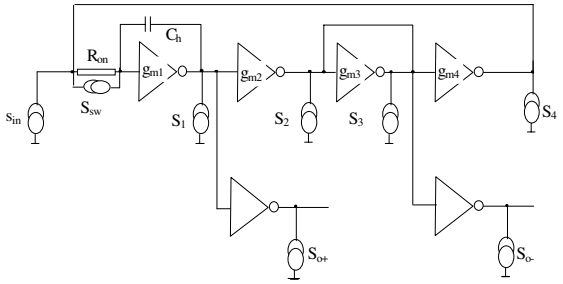

Fig. A.2. Noise equivalent circuit of the S-inv at sampling time.

The direct power spectral density of the output noise can be expressed during sampling time as

$$S_{oi}^{d}(f) = mS_{oi}(f) \tag{A3}$$

where m is related to the phase number (m=0.5 for two phases), and S_{oi} is the output PSD due to the noise source S_i. Moreover, The effect of the switch on noise is negligible due to its relatively large conductance compared to the transconductance of the input inverter. The direct PSD at the inverting output is

$$S_{o2}^{d} = m\left(S_{in}+S_4+\frac{S_1}{A_{v1}^2}+\frac{S_2+S_3}{A_{v1}^4}\right)+S_{o-} \tag{A-4}$$

3. Switched Inverter S/H at Hold Mode

At holding mode with 0.1% settling time ($mT_c \geq 7T_{on}=7C_h/g_m$), the held power spectrum density of the noise can be related to the direct term, as in [11], and the total power spectral density is

$$S_{oi}^{T} = (1+r)S_{oi}^{d} \tag{A-5}$$

where r is ratio between PSD of sampled hold to the direct PSD, which is equal to $3.5/(m-1)^2$.

Therefore, the mean square value of the output noise current can be approximated as

$$\overline{i_{o2n}^2} = (1+r)A_{v1}(S_{in}+S_4)g_o/4C_h + \overline{i_{o-n}^2} \tag{A-6}$$

Equation (A-6) gives 14dB signal to noise ratio at 1nA input current, which is very close to the simulation results.