Design-oriented model for short-channel MOS transistors based on inversion charge

Dayana A. Pino-Monroy
STMicroelectronics
38920 Crolles, France
dayana.pino.monroy@gmail.com

Patrick Scheer
STMicroelectronics
38920 Crolles, France

Mohamed K. Bouchoucha
STMicroelectronics
38920 Crolles, France

Carlos Galup-Montoro
Universidade Federal de Santa Catarina
88040-900 Florianopolis, Brazil

Manuel J. Barragan
Univ. Grenoble Alpes, CNRS,
Grenoble INP, TIMA
F-38000 Grenoble, France

Jean-Michel Fournier
Univ. Grenoble Alpes, CNRS,
Grenoble INP, TIMA
F-38000 Grenoble, France

Jean-Michel Fournier
Univ. Grenoble Alpes, CNRS,
Grenoble INP, TIMA
F-38000 Grenoble, France

Andreia Cathelin
STMicroelectronics
38920 Crolles, France

Sylvain Bourdel
Univ. Grenoble Alpes, CNRS,
Grenoble INP, TIMA
F-38000 Grenoble, France

2023 IEEE 14th Latin America Symposium on Circuits and Systems (LASCAS) | 978-1-6654-5705-7/23/$31.00 ©2023 IEEE | DOI: 10.1109/LASCAS56464.2023.10108277

***Abstract*— This paper presents a design-oriented MOS transistor model that uses only 7 parameters for analytically describing the MOSFET behavior. Based on the inversion charge, it accounts for the most relevant short-channel effects in advanced technologies. The model provides analytical relations for the transconductances, output conductance, and nonlinearities of the transistor for simple analytical circuit design. The model is validated using the 28nm FD-SOI technology from STMicroelectronics and is compared to a state-of-the-art 4-parameter model to demonstrate the advantages of the proposed model for RF/analog design purposes.**

Keywords—Analytical MOSFET modeling, charge-based MOSFET model, inversion coefficient, nonlinear distortion, short-channel effects, 28nm FD-SOI

I. INTRODUCTION

Design methodologies based on g_m/I_D and inversion coefficient (IC) are well suited to analog and RF purposes since the need for energy consumption optimization becomes more and more important in integrated circuit applications. This approach provides the designer with the information of the power efficiency to select the best operation regimes of the MOS transistor depending on the application. In advanced technology nodes such as the 28nm FD-SOI, the weak and moderate inversion regimes are the most interesting regimes if we consider the trade-off between low-power consumption and other performances as gain, noise figure or linearity [1]. For this reason, an accurate and simple model describing all operation regions (from linear to saturation) and regimes (from weak to strong inversion) is required to lead the designer to a first analytical circuit sizing before jumping into intensive simulation process for performances optimization.

ACM [2] and EKV [3] models are the basis of these IC-based or g_m/I_D-based design methodologies as they rely on the inversion charge of the MOS transistor. In addition, simplified versions of these models offers simple and suitable equations for circuit pre-conception [1], [4]–[7]. The simplest implementation of these models employs three parameters [8], [9]: the subthreshold slope factor, n, the specific current, I_{S0}, and, the threshold voltage, V_T. To comply with advanced nanometric technologies, more complex versions of these models have been developed to consider short-channel effects. Thus, an additional parameter was considered for modeling the drain-induced barrier lowering effect, introducing the σ parameter to improve V_D dependency in ACM models for weak to moderate inversion regimes [6].

In the same way, another parameter named ζ for ACM [10], or λ_C for EKV [11] was introduced to describe carrier velocity saturation. These models can be accurate enough especially for saturation and strong inversion regimes, allow for a better modeling of the saturation region and enable nonlinearity analysis [4]. However, these models fail to describe accurately the transition from the linear to the saturation region.

A 7-parameter analytical model is proposed in this paper. This model takes into account MOSFET short-channel effects allowing a calculation of the current as a function of V_D from the linear to the saturated region of the transistor and for all inversion regimes. Section II describes the considered short-channel effects, while in section III we explain how they have been included in our model. Furthermore, the derivatives of the current are inferred from the presented model in section IV and model consistency with respect to DC measurements is demonstrated in section V. Section VI summarizes our main contributions.

II. SHORT-CHANNEL EFFECTS

Our model considers the main short-channel effects affecting the behavior of MOS transistors in advanced technology nodes. In this regard, we have focused on the most relevant parameters to describe the drain current and its dependency with the MOS transistor terminal voltages, including the drain voltage.

A. Carrier mobility reduction and series resistances effects

The effective mobility of the carriers in the inversion layer of the MOS transistor depends on several scattering mechanisms causing a dependence of the mobility on the transversal and the longitudinal components of the electric field [2]. The first one will be treated in this subsection, and the second one is related to the carrier velocity saturation that will be explained in II.B.

When a high vertical electric field is applied in the transistor channel, the mobility in the inversion layer near the semiconductor-oxide interface is reduced. This

978-1-6654-5705-7/23/$31.00 ©2023 IEEE

reduction of the effective carrier mobility is mainly due to three mechanisms: Coulomb scattering, photon scattering, and surface roughness scattering [2]. The carrier mobility reduction will cause a decrease of the drain current, especially in strong inversion regime, and clearly visible in linear region.

On the other hand, the source and drain series resistances cannot be overlooked in short-channel devices. For short-channel transistors, the voltage drop in the source and drain regions becomes important in strong inversion and especially in linear region, as the channel resistance is minimal. In practice, the presence of source and drain series resistances can be described as a further reduction of the apparent carrier mobility [2].

B. Carrier velocity saturation effect

When the longitudinal electric field is low enough as in long-channel transistors, the carrier velocity is proportional to it. Nevertheless, for short-channel devices, when the longitudinal electric field increases, the carrier velocity reaches a limit and saturates. This effect is known as carrier velocity saturation [2] and introduces a new dependency of the drain current on the drain voltage, V_D.

C. Drain induced barrier lowering (DIBL) effect

The formation of the conduction channel in long-channel transistors depends mainly on the gate voltage which controls the electric field between the gate and the substrate terminals. However, as the channel length decreases, a drop of the potential barrier at the source side occurs when the drain voltage increases. This allows the creation of a conduction channel at a lower gate voltage, interpreted as a reduction of the threshold voltage, V_T. Adding the DIBL effect to the model will introduce direct dependency of the drain current on the drain voltage, V_D.

D. Channel length modulation (CLM) effect

The CLM effect occurs when the drain voltage increases after the pinch-off occurrence, creating a depletion region at the drain side and a reduction of the effective length of the channel, which increases the current as V_D increases [2]. Considering this phenomenon will add a third effect directly linked to the dependency of the drain current on V_D.

III. Analytical Model

The proposed analytical model is based on the 3-parameter ACM model presented in [5], [7], [12] in which we include the most significant short-channel effects previously described, leading to a 7-parameter model. The main equations of this model are presented below.

The model is based on the normalized inversion charges at the source and drain terminals of the transistor, q_S and q_D.

$$q_S = \frac{Q'_{IS}}{Q'_{IP}}, \tag{1}$$

$$q_D = \frac{Q'_{ID}}{Q'_{IP}}, \tag{2}$$

where, Q'_{IS} and Q'_{ID} are the inversion charges at source and drain, respectively. $Q'_{IP} = -nC'_{ox}U_T$, is the inversion charge density at pinch-off, and C'_{ox} is the oxide capacitance per unit area.

The relationship between the normalized inversion charges, q_S and q_D, and the source, drain, and gate voltages referred to the substrate, V_S, V_D, and V_G respectively, is given through the pinch-off voltage as following

$$V_P \approx \frac{V_G - V_{T0} + \sigma(V_D + V_S)}{n}, \tag{3}$$

$$V_P - V_S = U_T\big(q_S - 1 + ln(q_S)\big), \tag{4}$$

$$V_P - V_D = U_T\big(q_D - 1 + ln(q_D)\big), \tag{5}$$

where V_{T0} is the equilibrium threshold voltage, and the DIBL has been introduced with parameter σ [6]. Notice that the introduction of σ makes V_T dependent on the terminal voltages V_D and V_S.

Equations (4) and (5) can be used to directly relate q_S and q_D with the drain-to-source voltage,

$$V_{DS} = U_T\left(q_S - q_D + ln\left(\frac{q_S}{q_D}\right)\right). \tag{6}$$

The drain current is modeled as

$$I_D = I_{S0}\frac{(q_S - q_D)(q_S + q_D + 2)}{1 + \theta\left(\frac{q_S + q_D}{2}\right)}. \tag{7}$$

$$I_{S0} = \mu_n C'_{ox} n \frac{U_T^2}{2}\frac{W}{L}, \tag{8}$$

where, W is the width of the transistor, I_{S0} is the specific current given by (8), and parameter θ has been introduced to model the carrier mobility reduction. This results in an effective reduction of the drain current, especially in the linear region.

Then, the carrier velocity saturation effect, that has been widely considered in the literature [4], [10], [11], [13], is represented by ζ and defined as

$$\zeta = \frac{\mu_n U_T}{L v_{sat}}, \tag{9}$$

where, μ_n is the electron mobility, $U_T = kT/q$ is the thermal voltage, L is the transistor length, and v_{sat} is the saturation velocity of the carriers.

To be more accurate, μ_n in (9) should be replaced by the effective mobility that includes the effects of the vertical electric field and series resistances presented just before. Keeping here μ_n for simplicity purpose will lead to an effective value of ζ. When the transistor reaches the carrier velocity saturation,

$$i_{dsat} = \frac{I_{Dsat}}{I_{S0}} = \frac{2}{\zeta} q_{Dsat}. \tag{10}$$

and equation (7) becomes

$$I_{Dsat} = I_{S0}\frac{(q_S - q_{Dsat})(q_S + q_{Dsat} + 2)}{1 + \theta\left(\frac{q_S + q_{Dsat}}{2}\right)}. \tag{11}$$

By equating (10) and (11), the relation between q_S and q_{Dsat} is obtained given by (12) at the bottom of next page.

Going further, the saturation drain-to-source voltage is given by

$$\frac{V_{DSsat}}{U_T} = q_S - q_{Dsat} + ln\left(\frac{q_S}{q_{Dsat}}\right). \tag{13}$$

To ensure continuity of the model between the linear and saturation regions, the following term is introduced

$$V'_{DS} = \frac{V_{DS}}{\sqrt[4]{1+\left(\frac{V_{DS}}{V_{DSsat}}\right)^4}}. \quad (14)$$

Accordingly, a V'_D term has to be considered,

$$V'_D = V'_{DS} + V_S\,, \quad (15)$$

and therefore, also a q'_D,

$$V_P - V'_D = U_T\left(q'_D - 1 + ln(q'_D)\right). \quad (16)$$

Finally, related to the CLM effect, V_E, is integrated to the model in the main equation of the drain current as (17).

CLM is essential for modeling long and short-channel transistors in strong inversion regime in saturation region.

IV. Derivatives of the Drain Current

The presented model gives the DC characteristics of the transistor, but it also allows to model the AC behavior by estimating the current derivatives. Such characteristics are fundamental for a design-oriented model since it gives to the designer the means to analytically calculate gain, noise figure or IIP3 as a function of g_m, g_d or g_{m3}.

For illustration purposes, and due to space limitations, this paper shows the expression of the normalized derivatives, considering only the effects of the DIBL and carrier mobility reduction but neglecting the carrier velocity saturation. Interested readers are referred to [14] for further details.

The normalized value of the transconductance g_m, is the derivative of $i_d = I_D/I_{S0}$ with respect to the normalized gate voltage, $v_g = V_G/U_T$,

$$g_m = \frac{\partial i_d}{\partial v_g} = \frac{2}{nB}\left[q_S - q_D - i_d\frac{\theta}{4}\left(\frac{q_S}{1+q_S} + \frac{q_D}{1+q_D}\right)\right], \quad (18)$$

with,

$$B = 1 + \frac{\theta}{2}(q_S + q_D)\,. \quad (19)$$

The second and third derivatives of the drain current with respect to the gate are given by (20) and (21), respectively.

Thanks to the integration in the model of a direct dependence of the current on the drain voltage, it is possible to estimate the drain conductance, g_d, resulting in (22), where $v_d = V_D/U_T$ is the normalized drain voltage.

V. Consistency of the Model

The 7-parameter model was validated for several lengths of n-MOS transistors in the 28nm FD-SOI technology from STMicroelectronics. For the sake of simplicity, only the results obtained for the 1 µm wide and 30 nm long transistor will be presented here. The model parameter values are presented in Table I and were extracted following the procedure described in [14].

TABLE I. Technological Parameters for a n-MOS Transitor in 28nm FD-SOI Technology

Parameter	n	I_{S0} (µA)	V_{T0} (mV)	σ	θ	ζ	V_E (V)
4-Parameter Model	1.38	4.9	384.9	0.093	N/A	N/A	N/A
7-Parameter Model	1.38	5.9	384.9	0.093	0.115	0.035	5

Fig. 1 presents the main characteristics of interest and compares the proposed 7-parameters (red solid lines) with the 4-parameter model presented in [6] (purple dashed lines) and with the transistor measurements (green squares) for the 30nm n-MOS transistor.

For each characteristic of the 7-parameter model, the relative error has been estimated following (23), and plotted on the right axis of each figure (blue dots in Fig. 1).

$$\text{RE (\%)} = \frac{Model - Measure}{Measure} * 100\%\,, \quad (23)$$

It can be observed on $I_D(V_G)$ characteristics (Fig. 1(a) and (b)) that both models (4 and 7-parameter based) have a good accuracy in weak to moderate inversion regimes for different values of V_D. However, only the 7-parameter model is precise in strong inversion regime, thanks to the modeling of the carrier mobility reduction and the carrier velocity saturation effects.

On the other hand, Fig. 1(c) presents the $I_D(V_D)$ characteristic proving the importance of integrating the model parameters related to the direct dependency of the current on V_D, which is also reflected in (d), for the derivative, g_d. The 4-parameter model highly overestimate the values of both characteristics.

$$q_S = \frac{\theta}{2\zeta}q_{Dsat} - 1 + \sqrt{1 + q_{Dsat}\left(2 + \frac{2}{\zeta} - \frac{\theta}{\zeta}\right) + q_{Dsat}^2\left(1 + \frac{\theta}{\zeta} + \frac{\theta^2}{4\zeta^2}\right)} \quad (12)$$

$$I_D = I_{S0}\left(1 + \frac{V_{DS} - V'_{DS}}{V_E}\right)\frac{(q_S + q'_D + 2)(q_S - q'_D)}{1 + \frac{\theta}{2}(q_S + q'_D)} \quad (17)$$

$$g_{m2} = \frac{\partial^2 i_d}{\partial v_g^2} = \frac{2}{n^2 B}\left[\frac{q_S}{1+q_S} - \frac{q_D}{1+q_D} - \frac{\theta}{4}\left[2ng_m\left(\frac{q_S}{1+q_S} + \frac{q_D}{1+q_D}\right) + i_d\left(\frac{q_S}{(1+q_S)^3} + \frac{q_D}{(1+q_D)^3}\right)\right]\right] \quad (20)$$

$$g_{m3} = \frac{\partial^3 i_d}{\partial v_g^3} = \frac{2}{n^3 B}\left[-\frac{\theta}{4}\left[3n^2 g_{m2}\left(\frac{q_S}{1+q_S} + \frac{q_D}{1+q_D}\right) + 3ng_m\left(\frac{q_S}{(1+q_S)^3} + \frac{q_D}{(1+q_D)^3}\right) + i_d\left(\frac{q_S(1-2q_S)}{(1+q_S)^5} + \frac{q_D(1-2q_D)}{(1+q_D)^5}\right)\right] + \frac{q_S}{(1+q_S)^3} - \frac{q_D}{(1+q_D)^3}\right] \quad (21)$$

$$g_d = \frac{\partial i_d}{\partial v_d} = \frac{1}{B}\left[2q_S\frac{\sigma}{n} - 2q_D\left(\frac{\sigma}{n} - 1\right) - i_d\frac{\theta}{2}\left(\frac{\sigma}{n}\frac{q_S}{1+q_S} + \left(\frac{\sigma}{n} - 1\right)\frac{q_D}{1+q_D}\right)\right] \quad (22)$$

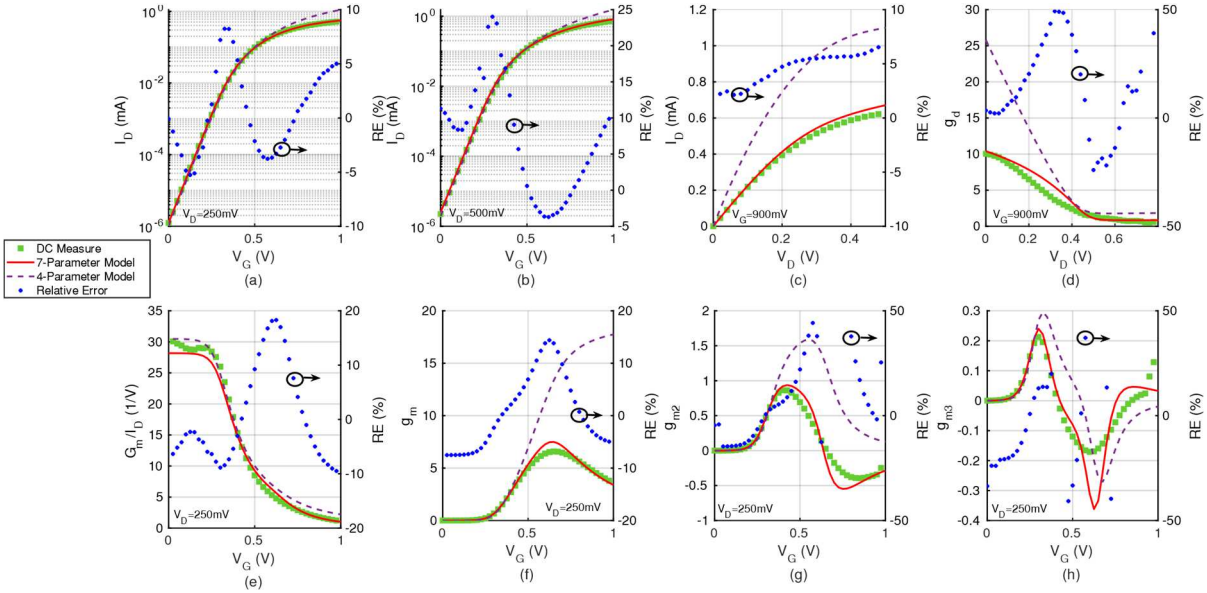

Fig. 1. L=30 nm and W=1µm n-MOS transistor characteristics, comparison between DC measurements (green squares), 7-parameter model (red solid line), 4-parameter model (purple dashed line) and relative error for the 7-parameter model (blue dots in right axis) for: (a) $I_D(V_G)$ for V_D=250 mV, (b) $I_D(V_G)$ for V_D=500 mV in linear scale, (c) $I_D(V_D)$ for V_G=900 mV, (d) $g_d(V_D)$ for V_G=900 mV, (e) $G_m/I_D(V_G)$ for V_D=250 mV where $G_m = g_m I_{s0}/(nU_T)$, (f) $g_m(V_G)$ for V_D=250 mV, (g) $g_{m2}(V_G)$ for V_D=250 mV, and (h) $g_{m3}(V_G)$ for V_D=250 mV.

Fig. 1(e) depicts the G_m/I_D ratio, an essential and interesting characteristic for analog design, specially to estimate the power efficiency of a circuit. In this case, the estimation of the 4-parameter model presents a similar result to that illustrated above, overestimating the values with respect to the measurements in strong inversion regime.

Finally, Fig. 1(f), (g), and (h) show the first three normalized derivatives with respect to V_G, g_m, g_{m2} and g_{m3}, respectively. Here, the 4-parameter model has a good accuracy for V_G values up to the threshold voltage while the 7-parameter model proves a closer estimation of those nonlinearity quantities.

Note that the relative error in the DC characteristics (Fig. 1(a)-(c)) has a maximum value of 25% with respect to the measurements, justifying the interest of a 7-parameter model.

VI. Conclusion

An analytical 7-parameter design-oriented model has been presented based on the inversion-charge of the MOS transistor for the 28nm FD-SOI technology. The model takes into account the main short-channel effects thanks to the introduction of technology-related parameters, achieving a good accuracy for the DC characteristics, with 10% maximum of relative error with respect to the measurements.

For the AC behavior, an estimation of the main derivatives of the current has been done based on a simplification of the proposed model, allowing to illustrate the g_m nonlinearities, the G_m/I_D ratio and the g_d, that are relevant parameters for analog and low-power designs. Finally, we can state that the 7-parameter model brings a significant accuracy improvement compared to any other analytical model while being compatible with circuit hand calculations.

References

[1] G. Guitton, M. de Souza, A. Mariano, and T. Taris, "Design Methodology Based on the Inversion Coefficient and its Application to Inductorless LNA Implementations," *IEEE Transactions on Circuits and Systems*, vol. 66, no. 10, pp. 3653–3663, 2019.

[2] C. Galup-Montoro and M. C. Schneider, *MOSFET modeling for circuit analysis and design*. New Jersey: World Scientific, 2007.

[3] C. Enz and E. A. Vittoz, *Charge-based MOS transistor modeling: the EKV model for low-power and RF IC design*. Chichester, England; Hoboken, NJ: John Wiley, 2006.

[4] F. Chicco and C. C. Enz, "Charge-Based Distortion Analysis of Nanoscale MOSFETs," *IEEE Transactions on Circuits and Systems*, vol. 66, no. 2, pp. 453–462, 2019.

[5] M. Siniscalchi, N. Gammarano, S. Bourdel, C. Galup-Montoro, and F. Silveira, "Modeling a nanometer FD-SOI transistor with a basic all-region MOSFET model," *IEEE Latin America Electron Devices Conference (LAEDC)*, pp. 1–4, 2020.

[6] C. M. Adornes, D. G. A. Neto, M. C. Schneider, and C. Galup-Montoro, "Bridging the gap between design and simulation of low voltage CMOS circuits," *IEEE Nordic Circuits and Systems Conference (NorCAS)*, p. 5, 2021.

[7] S. Bourdel, S. Subias, M. K. Bouchoucha, M. J. Barragan, A. Cathelin, and C. Galup, "A gm/ID Design Methodology for 28 nm FD-SOI CMOS Resistive Feedback LNAs," *IEEE International Conference on Electronics, Circuits, and Systems (ICECS)*, p. 4, 2021.

[8] M. C. Schneider, C. Galup-Montoro, S. M. Acosta, and A. I. A. Cunha, "Distortion analysis of MOSFETS for application in MOSFET-C circuits," *ISCAS '98. Proceedings of the 1998 IEEE International Symposium on Circuits and Systems*, pp. 33–36, 1998.

[9] P. G. A. Jespers and B. Murmann, "Calculation of MOSFET Distortion Using the Transconductance-to-Current Ratio (gm/ID)," *IEEE International Symposium on Circuits and Systems (ISCAS) 2015*, pp. 529–532, 2015.

[10] P. D. da Silva, C. Galup-Montoro, M. C. Schneider, and F. R. de Sousa, "Design-oriented model for nonlinearities in MOSFETs," *Circuits and Systems and TAISA Conference 2008*, pp. 153–156, 2008.

[11] C. Enz, F. Chicco, and A. Pezzotta, "Nanoscale MOSFET Modeling Part 1: The Simplified EKV Model for the Design of Low-Power Analog Circuits," *IEEE Solid-State Circuits Magazine*, vol. 9, no. 3, pp. 26–35, 2017.

[12] A. I. A. Cunha, M. C. Schneider, and C. Galup-Montoro, "An MOS transistor model for analog circuit design," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 10, pp. 1510–1519, 1998.

[13] W. Sansen, "Biasing for Zero Distortion: Using the EKV\/BSIM6 Expressions," *IEEE Solid-State Circuits Magazine*, vol. 10, pp. 48–53, 2018.

[14] D. A. Pino-Monroy *et al.*, "Design-Oriented All-Regime All-Region 7-Parameter Short-Channel MOSFET Model Based on Inversion Charge," *IEEE Access*, vol. 10, p. 16, 2022.