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RESEARCH ARTICLE

Design-Oriented Single-Piece 5-DC-Parameter MOSFET Model

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ABSTRACT This paper presents a novel charge-based MOSFET model, denoted ACM2, including velocity saturation and drain-induced barrier lowering. Employing the proposed model, all the DC characteristics (currents and charges) and the small-signal equations can be expressed as single-piece expressions valid in all inversion (weak, moderate, and strong) regions. When applied to bulk technology, ACM2 has 5 DC parameters, and an extra parameter is included for SOI technologies to account for back gate bias. Straightforward procedures are provided for extracting the short-channel parameters associated with velocity saturation and back gate bias. Experimental results demonstrate that the DC and small-signal characteristics of the ACM2 model match the silicon measurements in bulk and SOI technologies, with typical errors of less than 20 % in the DC currents and 30 % in the transconductances. The validity of the model is further verified with two design examples. Firstly, simulations of a CMOS inverter in a 130 nm bulk technology show similar results using the PSP or ACM2 models. Then, an RF design example is provided. The ACM2 model is employed to design a 2.4 GHz low-noise-amplifier in a 28 nm FD-SOI CMOS technology. Obtained results in terms of S_{11}, S_{21}, NF, and IIP3 are consistent with simulations using the complete UTSOI2 model provided in the technology design kit.

INDEX TERMS ACM model, design-oriented model, FD-SOI, MOSFET, MOSFET model, open-source PDK, inverter, RF LNA.

I. INTRODUCTION

Textbooks for integrated circuits (IC) design [1], [2], [3], [4] present oversimplified MOSFET models valid only in specific regions of operation. On the other hand, the accurate BSIM models [5], available with most of the process design kits (PDKs), are extremely complex and need hundreds of parameters. Recent studies [6], [7], [8], [9], [10] aim to bridge the gap between the oversimplified design models and the extremely complex simulation ones. In effect, a design-oriented transistor model, valid in all the operating regions of the device, with a few, but meaningful electrical parameters, is of great help for properly sizing transistors in the pre-simulation phase of a design flow.

Furthermore, jointly with the open-source PDKs and tools [11], simple and accurate compact models in

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open-source simulators will also help the entrance of new engineers in the integrated circuit design domain.

In [6], the inclusion of the drain-induced barrier lowering (DIBL) coefficient σ to the long-channel model rendered a 4-parameter model (4PM) consisting of single-piece equations that has successfully simulated MOS circuits operating at low voltages. The 7-DC-parameter model in [7] is strongly based on physics, but still uses the mathematical interpolation function presented in [12] and [13] to obtain the continuity between the triode and saturation regions. Finally, the work of [8] introduced a compact model, valid in all operating regions, that avoids, for the first time, the use of interpolation functions employed in previous models.

This work develops the minimalist 5-parameter model (5PM) of [8], which consists of single-piece functions and is not restricted to the low-voltage domain. The 5 parameters are the threshold voltage V_{T0}, the specific current I_S, the slope factor n, the drain-induced barrier lowering (DIBL) coefficient σ and the parameter ζ associated to velocity saturation. Also, a sixth parameter, dedicated to FD-SOI technologies, is included to model the effect of the back gate voltage, giving rise to a 6-parameter model (6PM).

The paper is organized as follows. Section II introduces the main equations of the ACM2 model. Section III presents the methods to extract the 5(6) electrical parameters. Section IV validates the proposed ACM2 for a 130-nm bulk CMOS and 28 nm FD-SOI CMOS technologies against the PSP [14] and UTSOI2 [15], [16] models, respectively. In Section V, the low-frequency small-signal model is developed and validated. Finally, in Section VI, a CMOS inverter and a low noise amplifier (LNA) exemplify the application of the model in circuit simulations.

II. THE MAIN MODEL EQUATIONS

The ACM2 model is based on the charge-controlled model of the drain current proposed by Maher and Mead in 1987 [17], which takes into account both the drift and diffusion components of the current as well as the saturation velocity phenomenon, yielding (1).

$$I_D = I_S \frac{(q_s + q_d + 2)}{1 + \zeta |q_s - q_d|} (q_s - q_d). \tag{1}$$

For an n-channel transistor, the normalized inversion charge densities at source (q_s) and drain (q_d) are defined as the inversion charge densities $Q_{S(D)}$ normalized to the thermal charge density $-nC_{ox}\phi_t$ as given in (2).

$$q_{s(d)} = \frac{Q_{S(D)}}{-nC_{ox}\phi_t}. \tag{2}$$

where C_{ox} is the oxide capacitance per unit area, n is the slope factor and ϕ_t is the thermal voltage. The specific current I_S, given in (3), is related to the gate width W and length L, and to technology parameters. μ is the carrier mobility.

$$I_S = \mu n C_{ox} \frac{\phi_t^2}{2} \frac{W}{L}. \tag{3}$$

Parameter ζ is a short-channel parameter associated with the velocity saturation phenomenon. It is defined by (4) as the ratio of a diffusion-related velocity to v_{sat}, the saturation velocity.

$$\zeta = \frac{\frac{\mu\phi_t}{L}}{v_{sat}}. \tag{4}$$

For sufficiently long L, we can ignore the velocity saturation effect; thus, (1) reduces to,

$$I_D = I_S \left[q_s^2 - q_d^2 + 2(q_s - q_d) \right], \tag{5}$$

where the quadratic terms arise from drift, while the linear terms arise from diffusion [17], [18], [19]. Comparing (1) and (5) we observe an important consequence of velocity saturation in the drain current expression. For long-channel transistors, $\zeta \to 0$ and (5) holds; thus, an increase in the drain-to-source voltage reduces the normalized drain charge; consequently, the drain current increases. In contrast, for short-channel devices, (1) holds and the drain current can attain a maximum, as shown in Fig. 1.

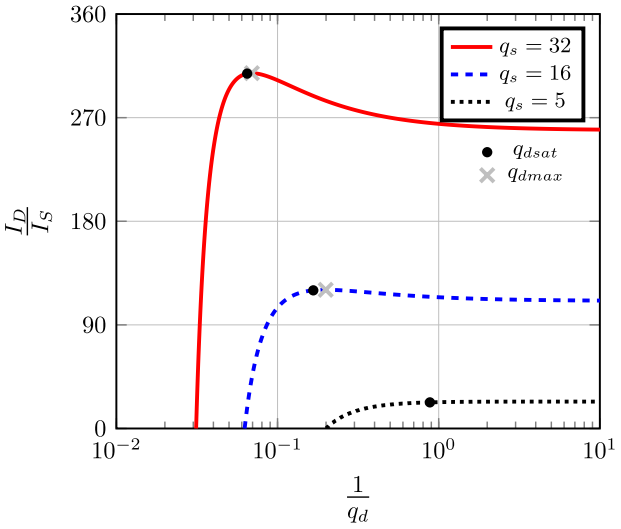

FIGURE 1. Characteristic of the drain current, eqn. (1), for a velocity saturation parameter $\zeta = 0.1$. The $1/q_d$ horizontal axis is chosen in order to plot saturation as usual in the right direction of the output characteristics.

The extremum condition for (1),

$$I_D = \left. \frac{dI_D}{dq_d} \right|_{q_{dmax}} = 0, \tag{6}$$

gives,

$$q_{dmax} = q_s + \frac{1}{\zeta} - \frac{1}{\zeta}\sqrt{1 + 2\zeta(q_s + 1)}. \tag{7}$$

Multiplying and dividing (7) by the algebraic conjugate we obtain,

$$\frac{q_{dmax}}{q_s} = \frac{\zeta q_s - \frac{2}{q_s}}{1 + \zeta q_s + \sqrt{1 + 2\zeta(q_s + 1)}}. \tag{8}$$

Thus, we have a maximum in the I_D vs. q_D curve for

$$q_s > \sqrt{\frac{2}{\zeta}}. \tag{9}$$

The bump in the output characteristics has no physical meaning, but even when the output characteristics increase monotonically (*e.g.* in weak inversion), the saturation for q_d going to zero has no physical meaning, either. In effect, due to the velocity saturation of the carriers,the absolute value of Q_{Dsat}, the carrier charge at the drain end, has a minimum, given [18], [19] by,

$$I_{Dsat} = -Wv_{sat}Q_{Dsat}. \tag{10}$$

Or, using normalized variables,

$$i_{dsat} = \frac{I_{Dsat}}{I_S} = \frac{2}{\zeta}q_{dsat}. \tag{11}$$

From (1) and (11), the saturation charge density normalized to the thermal charge density is given by,

$$q_{dsat} = q_s + 1 + \frac{1}{\zeta} - \sqrt{\left(1+\frac{1}{\zeta}\right)^2 + \frac{2q_s}{\zeta}}. \tag{12}$$

Comparing (7) and (12) it is easy to verify that,

$$q_{dsat} > q_{dmax}. \tag{13}$$

Thus, physical saturation occurs always in the triode region (before the bump) of the output characteristics. It is interesting to observe that for the strong inversion model, $q_{Dmax} = q_{Dsat}$, as shown in page 248 of [20]. Thus, in the strong inversion model, saturation velocity occurs at the maximum of the output curve.

The unified charge-control model (UCCM) [18], [19] expresses the relationship between the terminal voltages and the normalized charge densities for all inversion levels of a long-channel transistor. In the UCCM, the source and drain normalized charge densities q_S and q_D are calculated using (14):

$$\frac{V_P - V_{S(D)B}}{\phi_t} = q_{s(d)} - 1 + \ln q_{s(d)}. \tag{14}$$

The pinch-off voltage V_P is linearly approximated [21] by (15), where V_T is the threshold voltage.

$$V_P = \frac{V_{GB} - V_T}{n}. \tag{15}$$

Applying (14) to the source and drain we obtain the symmetrical expression (16), that links q_s and q_d with the potential drop V_{DS} along the channel.

$$\frac{V_{DS}}{\phi_t} = q_s - q_d + \ln\left(\frac{q_s}{q_d}\right). \tag{16}$$

For a long channel transistor, it is clear from (16), that $q_D \to 0$ when $V_{DS} \to \infty$. The classical way to deal with velocity saturation using (16) is to calculate the drain-to-source saturation voltage substituting q_d by its saturation value. In the present model we avoid the definition of a saturation voltage substituting $q_{s(d)}$ by $q_{s(d)} - q_{dsat}$ in (16), getting (17)

$$\frac{V_{DS}}{\phi_t} = q_s - q_d + \ln\left(\frac{q_s - q_{dsat}}{q_d - q_{dsat}}\right). \tag{17}$$

Equation (17) has the necessary properties to model the effect of the velocity saturation of the carriers using single-piece equations. In effect, $V_{DS} = 0$ for $q_s = q_d$, $q_d \to q_{dsat}$ when $V_{DS} \to \infty$. If we interchange q_s and q_d, V_{DS} changes sign.

As shown in Fig. 2, the use of the modified UCCM (17) avoids the bump in the output characteristic without the need of an interpolation function. The commonly used interpolation functions between the triode and saturation regions not only complicate the code of the model but also produce glitches in the derivatives at $V_{DS} = 0$, besides not passing the so-called Gummel symmetry test [22].

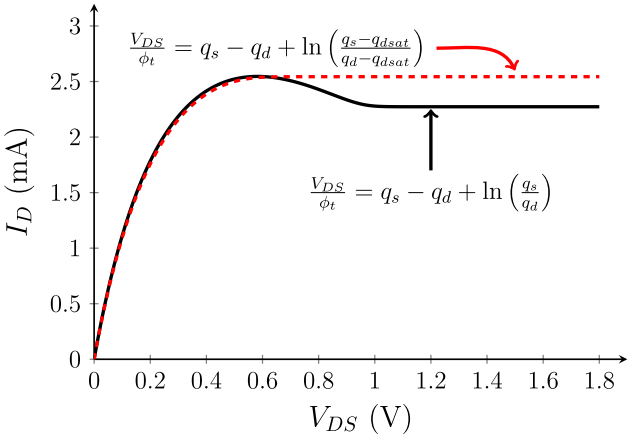

FIGURE 2. Effect of the maximum of $I_D(q_d)$ on the output characteristic $I_D(V_D)$.

MOS transistors are symmetrical devices; therefore, their models must also be symmetrical, *i.e.* the drain and source terminals can be chosen arbitrarily, but the transistor characteristics must remain the same regardless of the choice that has been taken. Furthermore, the transition between forward ($V_{DS} > 0$) and reverse ($V_{DS} < 0$) operations must be continuous.

The term in the denominator of (1) causes a discontinuity in the derivative of the current, with respect to V_{DS}, at $V_{DS} = 0$. To avoid this problem, we approximate the absolute value function as,

$$1 + \zeta\,|q_s - q_d| \cong 1 + \sqrt{\zeta^2\,(q_s - q_d)^2 + \epsilon^2}. \tag{18}$$

where ϵ has been chosen equal to 0.1.

In the Gummel symmetry test, the transistor is symmetrically biased with a differential voltage $V_{DS} = 2V_X$ and a common mode voltage V_{CM}, as shown in Fig. 3. By changing the voltage V_X from positive to negative values, the transistor characteristics proceed symmetrically from the forward region to the reverse region. To pass the Gummel test,

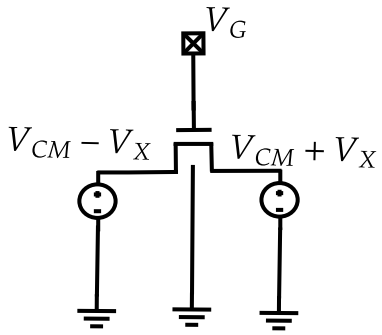

FIGURE 3. Circuit for the Gummel symmetry test.

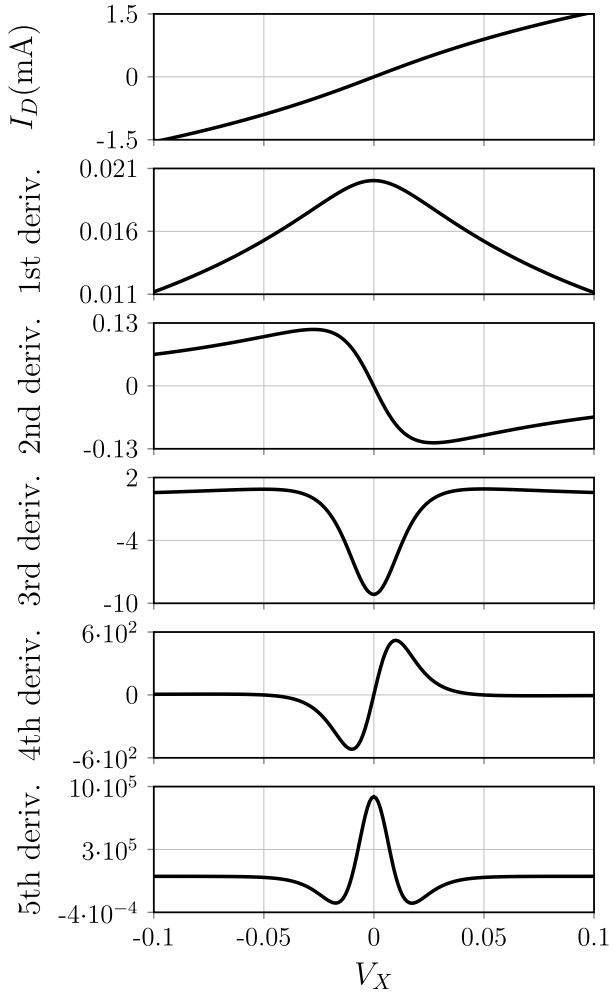

FIGURE 4. Drain current and its first to fifth order derivatives with respect to V_X.

the model must provide a continuous transition of the drain current and its derivatives with respect to V_X.

Fig. 4 shows that the ACM2 model generates symmetrical continuous curves for the drain current and its derivatives, with smooth transitions for all derivatives around $V_X = 0$.

Finally, the drain-induced barrier lowering (DIBL) coefficient σ is introduced to account for the effect of both the drain and source voltages on the threshold voltage, as shown in eqn. (19), which keeps the device symmetry [18], [19].

$$V_T = V_{T0} - \sigma(V_S + V_D). \tag{19}$$

Here, V_{T0} is the equilibrium threshold voltage.

Summarizing, the ACM2 calculates V_T from (19), V_P from (15), q_S from (14), q_{Dsat} from (12), q_D from (17) and I_D from (1).

Fig. 5 summarizes the differences between the 3-parameter long-channel MOSFET model and the proposed 5-parameter model for the bulk technology. As regards the value of the drain current, in weak inversion, the effect of velocity saturation is irrelevant, but DIBL is strong; deep in strong inversion, it is the opposite, and in between, both DIBL and velocity saturation are relevant. The n-channel MOSFET used in Figs. 2, 4 and 5 has the following parameters: $V_{T0} =$ 528 mV, $I_S = 5.52\ \mu$A, $n = 1.37$, $\sigma = 0.026$ and $\zeta = 0.056$.

Transistors of SOI-based technologies have a fourth terminal, the back gate, that can be used as a tuning knob to control the channel [23]. The back gate is coupled to the channel with an insulator thicker than that between the main gate and the channel. The back gate acts as a secondary gate that allows a fine-tuning of the device characteristics, especially through the modulation of the threshold voltage. The transistor model of SOI-technologies is completed, then, through the introduction of parameter δ, which encapsulates the threshold voltage variation with the body bias voltage V_{BB}. For an SOI N-type transistor in which $V_{BB} = 0$ V, the model coincides with that of the bulk technology. Hence, the additional 6th parameter δ characterizes exclusively the FD-SOI features and allows the model of the bulk technologies to be adapted to SOI technologies and be denoted 6PM ACM2. This extended (6PM) version of the 5PM ACM2 model shares the same aforementioned equations; however, the terminal charge densities are solved for the modified expression of the threshold voltage, given by,

$$V_T = V_{T0} - \sigma(V_S + V_D) - \delta V_{BB}. \tag{20}$$

The sign of δ can easily address the forward and reverse modes for both channel types. For the 28 nm FD-SOI CMOS technology, the variation of the threshold voltage V_T as a function of the body bias voltage is explicitly explained in [23] and reported in Fig. 6. Note that, for 4 transistor types, the linear approximation in (20) of the threshold voltage with the body bias voltage fits very well the experimental results.

The PMOS model can be easily expressed using the generic formalism defined for the NMOS transistor with minor changes. It maintains the same charge densities and current definitions as well as the effect of the short-channel parameters. The terminal voltages, since they are referred to as a higher potential (V_{DD}), can be defined with a negative sign to be implemented using the same charge-voltage equations (14), (15), (17), and (20).

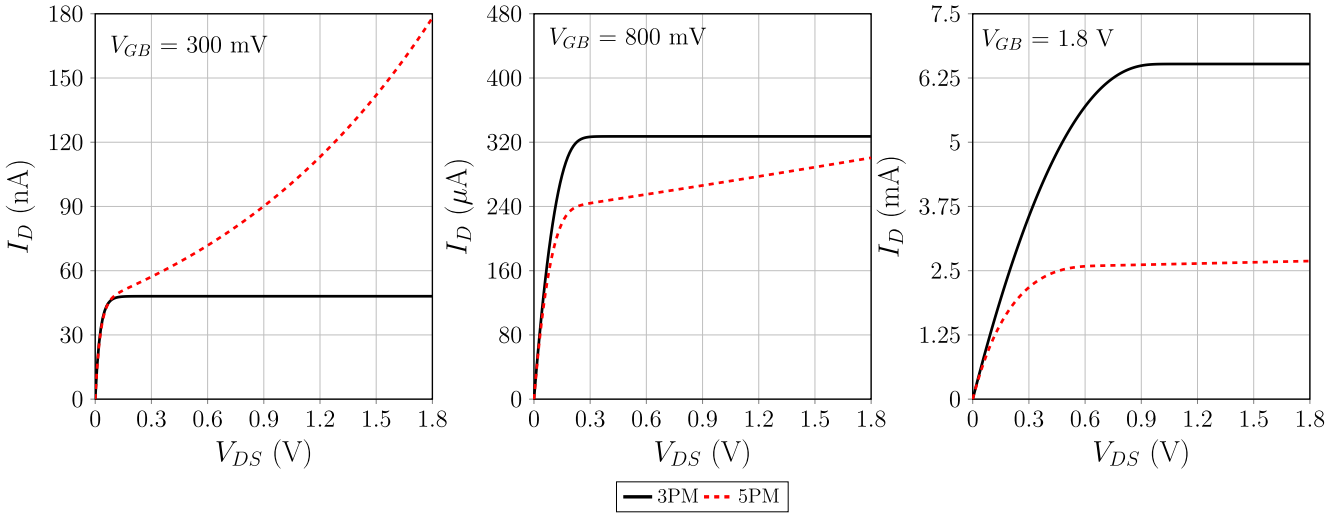

FIGURE 5. Output characteristics for an NMOS transistor including DIBL and v_{sat}.

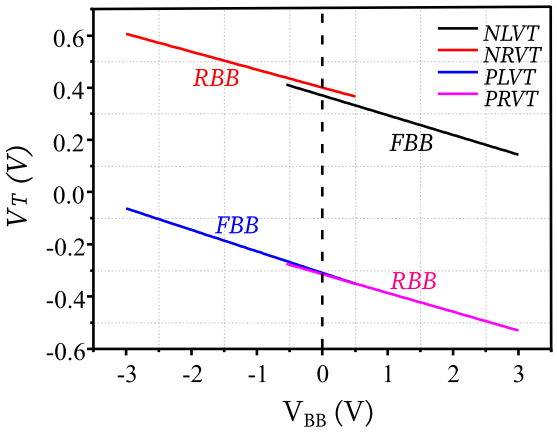

FIGURE 6. Threshold voltage variation as function of the body bias voltage for NMOS (N) and PMOS (P) transistors using the regular threshold voltage flavor (RVT) and the low threshold voltage flavor (LVT) from the 28 nm FD-SOI CMOS tehnology [23].

III. PARAMETER EXTRACTION

No matter the quality of a model, its accuracy hinges upon the appropriate values of the parameters employed. The enormous advantage of having only five physics-based parameters is that we were able to develop a direct method for the extraction of each of them, minimizing the interference of spurious effects in each extraction. Parameters V_{T0} and I_S are extracted simultaneously for very low V_{DS}, in the transition from weak to moderate inversion, using the g_m/I_D methodology reported in [6], for which the secondary effects of series resistances, mobility reduction, drain-induced barrier lowering, Early effect, and velocity saturation are negligible. The slope factor n is determined at low V_{DS} in weak inversion, as in [6] and [7].

The DIBL parameter σ is simply the inverse of the intrinsic common source gain in the saturation region, either in weak or moderate inversion, as explained in [6]. In this paper we adopted a constant value of sigma, representative of moderate inversion.

The velocity saturation parameter ζ [19] that completes the ACM2 DC parameters for bulk transistors can be easily extracted from the combination of (11) with the inverse of (12). The inverse function of (12) is,

$$q_s = \sqrt{1 + \frac{2}{\zeta} q_{dsat}} - 1 + q_{dsat}, \tag{21}$$

which gives,

$$\zeta = \frac{2\left(q_s + 1 - \sqrt{1 + i_{dsat}}\right)}{i_{dsat}}. \tag{22}$$

The normalized source charge q_s can be computed from parameters (V_{T0}, n, σ), along with equation (14). The i_{dsat} value corresponds to the drain current, normalized to the specific I_S. This drain current can be obtained through either measurement or simulation for a given operating point (V_G, V_D, V_S, V_B) within the saturation region. For the extraction of ζ in the NMOS transistor, the operating point was configured as $V_G = V_D = V_{DDmax}$ and $V_S = V_B = 0$ V. V_{DDmax} is the maximum V_{DD} allowed for the technology.

For the extraction of parameter δ, a plot of the threshold voltage versus the body bias voltage, such as Fig. 6, can be employed. The line slope corresponds to δ.

The extraction methodologies outlined herein are equally applicable to PMOS devices.

Table 1 presents the extracted parameters of the low threshold voltage (LVT) NMOS and PMOS transistors of the 130-nm CMOS and 28 nm FD-SOI CMOS technologies. Finally, to summarize, the conceptual structure of the model, including its main parameters, is represented in Fig. 7.

IV. MODEL IMPLEMENTATION AND VALIDATION

Using a MATLAB® and/or a Verilog-A algorithm, the proposed set of equations is implemented and solved

TABLE 1. Extracted parameters of transistors of the 130 nm bulk and 28 nm FD-SOI CMOS technologies.

Technology	130 nm		28 nm	
Transistor	NMOS	PMOS	NMOS	PMOS
W/L (μm/μm)	10/0.12	10/0.12	1/0.06	1/0.06
V_{TO} (mV)	490	- 478	389	- 404
I_S (μA)	11.78	9.39	3.15	0.76
n	1.41	1.46	1.15	1.01
σ	0.053	0.048	0.018	0.029
ζ	0.007	0.031	0.039	0.024
δ	-	-	0.079	-0.076

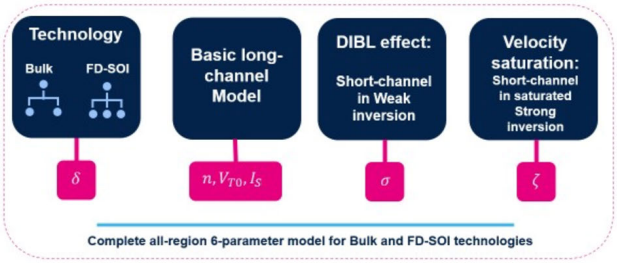

FIGURE 7. Conceptual structure of the ACM2 MODEL.

to derive the main characteristics relationships using the 443 Algorithm [24] for the UCCM equation.

The Verilog-A code facilitates the inclusion of the 5PM ACM2 model [25] into both commercial and open-source circuit simulators. In the case of open-source tools, the utilization of *openvaf* [26], a Verilog-A compiler designed for ngspice, is essential to incorporate the model into circuit simulations.

The ACM2 is an all-region single-piece model in contrast with [7], which uses the interpolation function introduced in [13] to obtain the continuity between the triode and saturation regions.

A. DC CHARACTERISTICS: BULK CMOS TRANSISTORS

An open-source PDK was used to compare the results of the DC characteristics I_D vs V_{GB} and I_D vs V_{DS} for the bulk technology, either using the PSP model or the ACM2 model. The design kit from the Institute for High-Performance Microelectronics (IHP) [27] was chosen due to available silicon measurements.

The IHP SiGe 130 nm BiCMOS technology uses the PSP MOSFET model [14] for SPICE simulations. The PSP model is also implemented in Verilog-A to simulate the model in the open-source framework. The Verilog-A was also compiled by the *openvaf* software.

Figures 8- 9 show the DC characteristics of a minimum-length low-voltage threshold (LVT) NMOS transistor of the IHP technology. The relative error refers to the difference between the IHP measurements and the 5 PM, normalized to the IHP measurements.

Fig. 8 shows good matching between the IHP measurements and both the PSP and ACM2 models for the I_D vs V_{GB} characteristic. In saturation ($V_{DS} = 0.6, 1.2$ V) and strong inversion ($V_{GB} > 1$ V) the relative error is negligible, which shows a remarkable result for a 5-DC constant-parameter design-oriented model.

Fig. 9 shows the good matching between the IHP measurements and both PSP/ACM2 models for the I_D vs V_{DS} characteristic. The ACM2 model has a good fitting over all the inversion levels. It is interesting to observe that in weak inversion, ACM2 better represents the high DIBL effect than PSP.

B. DC CHARACTERISTICS: FD-SOI

The obtained results are compared to the UTSOI2 compact model implemented in the design KIT and measured results for different bias conditions and transistor sizes. For sake of simplicity, the comparison is done for a low threshold voltage RF "$LVTNFET_{RF}$" of the 28 nm FD-SOI CMOS technology of STMicroelectronics with length $L = 60$ nm and width $W = 1\mu m$, for which the corresponding parameters were extracted.

As a main characteristic, the drain current to gate voltage (I_D *vs* V_G) relationships are evaluated for different drain voltages. In Fig.10, the model UTSOI2-based simulations and measurements data are reported for drain voltages $V_D =$ 50, 100, 250, 500, 750, and 1000 mV for $V_{BB} = V_{BN} = 0$ V and $V_D = 500$ mV with $V_{BB} = V_{BN} = 1$ V. In a secondary axis, the relative error of the 6PM ACM2 model with respect to the measurements is shown. The x-axis represents the different inversion regions of the device since it covers the allowed range of V_G.

The first case shows the current characteristic in linear region. For $V_{GS} < 0.7$ V, which covers weak, moderate, and early strong inversion regions, the relative error with respect to the measurements is less than 20%, and the model captures well the behavior of the current with a small deviation for high V_{GS}. For higher V_{DS} values, the transistor enters the saturation region, and the relative error is small. Since the model is design-oriented and is used as a simple tool to predict the transistor behavior analytically, the most interesting regions for which a good fitting is required are mostly the weak to moderate inversion regions in saturation. In fact, these regions are required for low-power design, and the saturation region is important for some circuits to control the DC biasing. Using the introduced 5PM version, the obtained ($I_D vs V_G$) curves are very close to the transistor characteristic implemented with the PDK model and measurements. Hence, the simple model is well adapted to short-channel transistors as well as a large drain-to-source voltage that were not captured in most models in the technical literature. The complementary parameter, δ, is introduced to compare the transistor description with measured results in the presence of body voltage $V_{BN} = 1$ V as an illustrative example. As shown in Fig.10, the measured results of the drain current to gate voltage characteristic are compared to the model for a body bias voltage V_{BB}. This verification is followed for different V_{DS} values to cover all operation regions. The model is in good agreement with the measured

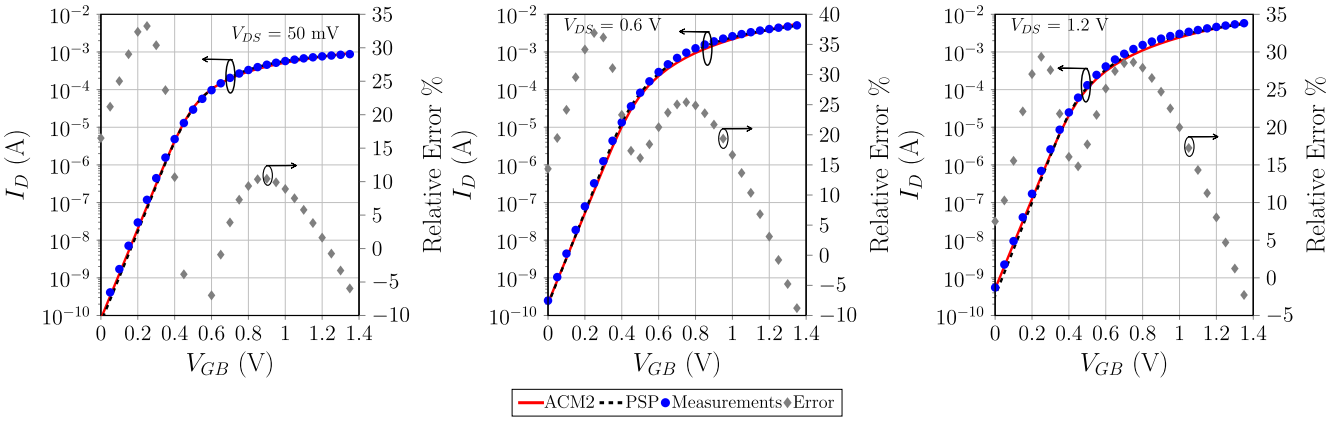

FIGURE 8. $I_D - V_G$ Characteristics for an LVT NMOS bulk transistor with $W/L = 10\ \mu$m/ 120 nm.

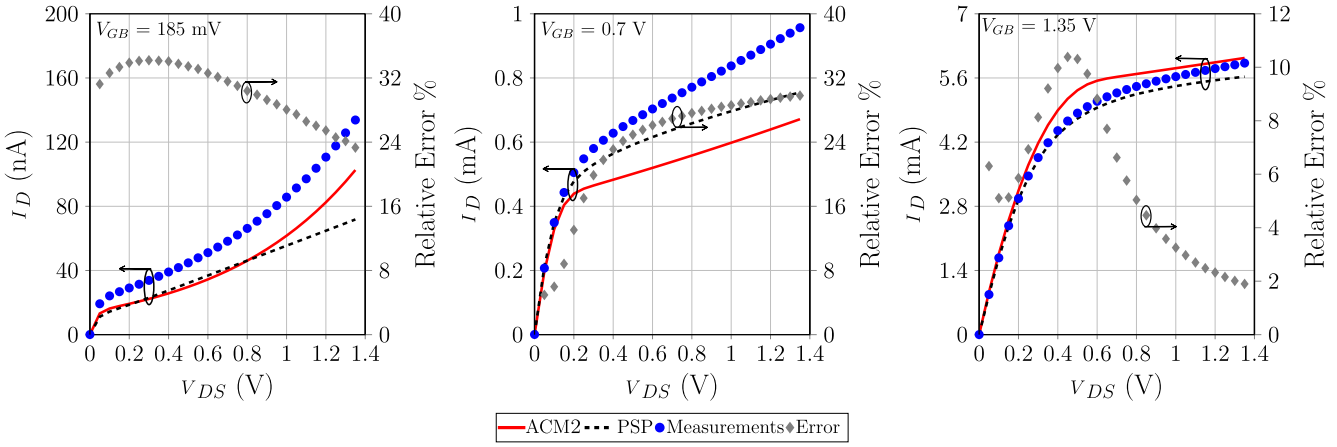

FIGURE 9. $I_D - V_D$ Characteristics for an LVT NMOS bulk transistor with $W/L = 10\ \mu$m/ 120 nm.

values in all regions. Hence, the accuracy of the 6PM ACM2 model is validated through measurements and in comparison with the PDK compact model. Besides, the inclusion of the body bias voltage in the model effectively reshapes the characteristic curve of the transistor as predicted by lowering the threshold voltage and follows accurately the measured current.

The drain current to drain voltage ($I_D vs V_D$) curves are plotted in different inversion regions at $V_G = 100$ mV, 400 mV, 700 mV for the 5PM version and $V_G = 0.4$ V and $V_{BN} = 1$ V, as an illustrative example for the 6PM version. In Fig. 11, a comparison between the 6PM ACM2 model, the UTSOI2 model, and measurement is presented. From the transistor output characteristics, we can drive the same conclusion as for the ($I_D vs V_G$). The model accurately reproduces the measurement data in the saturation region with a relative error of less than 10% over the different inversion regions. In the linear region, the model captures well the transistor behavior for low V_{GS}. Then, as V_{GS} increases, the relative error get higher while the shape of the curve is well captured and the absolute difference is low. The complementary parameter is implemented to compare the transistor description with measured results in the presence of a body voltage $V_{BN} = 1$ V. As shown in Fig. 11, the model captures well the effect of the body in reducing the threshold voltage.

Although the curve shape is well captured by the 6PM ACM2 representation, in linear region for low values of V_D the approximation deviates a little from the measured current due to some short channel effects that are not taken into account here for the simplicity of the model. In fact, the carrier mobility reduction dominates the SCEs for transistors operating in linear regime [19].

V. SMALL-SIGNAL MODEL

A. DESIGN-ORIENTED MODEL

The small-signal transconductances expressions complete the 5-6 parameter model and bridges the gap between transistor level description and system level allowing systematic design methodologies for integrated circuits. Fig.12 details the equivalent low-frequency small-signal circuit to describe the MOSFET transistor and shows the transconductances

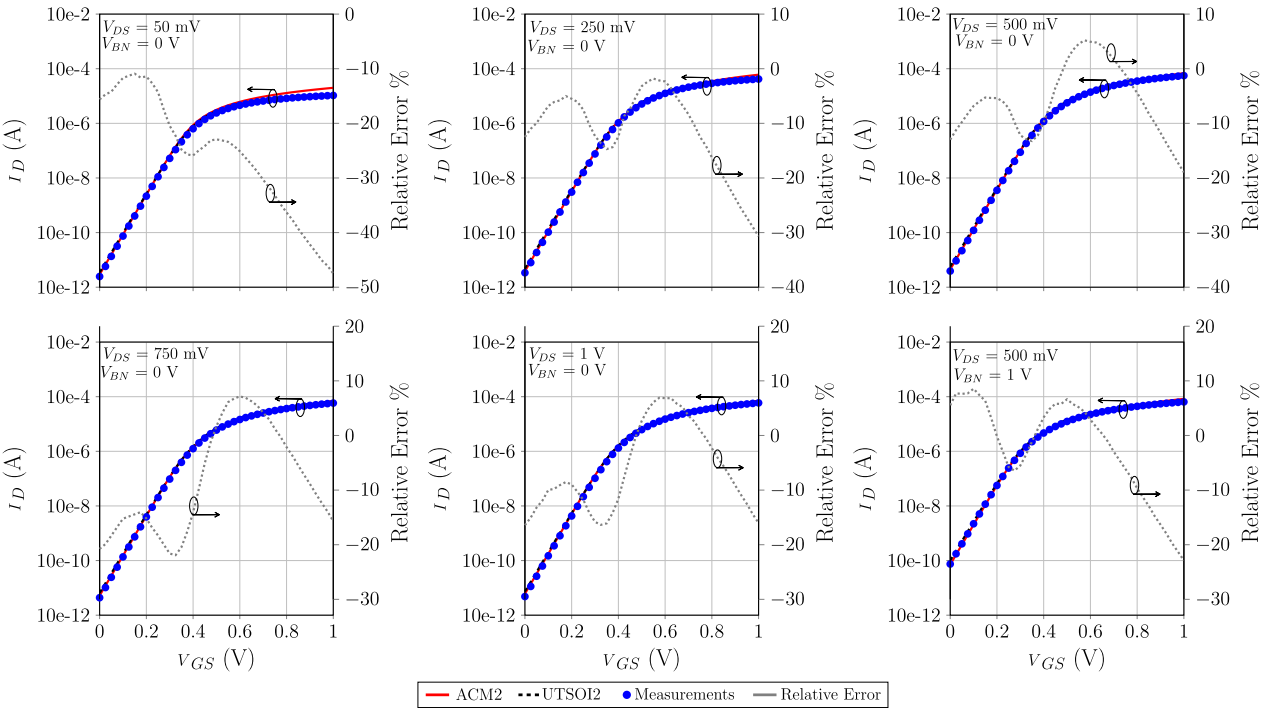

FIGURE 10. $I_D - V_G$ Characteristics for a NMOS LVT transistor from the 28 nm FD-SOI CMOS technology with W/L = 1 μm/ 60 nm for different V_{DS} and V_{BN}.

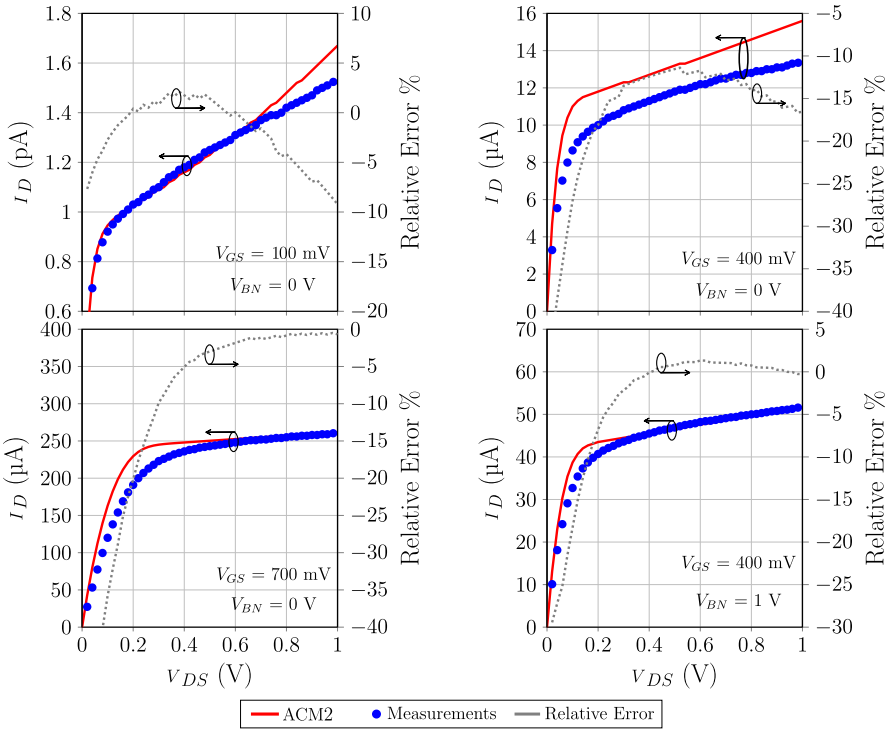

FIGURE 11. $I_D - V_D$ Characteristics for a NMOS LVT transistor from the 28 nm FD-SOI CMOS technology with W/L = 1 μm/ 60 nm for different V_{GS} and V_{BN}.

associated with different nodes, which are related to the drain current I_D as,

$$I_D = g_m v_G - g_{ms} v_S + g_{ds} v_D + g_{mb} v_B, \tag{23}$$

where g_m, g_{ms}, g_{ds} and g_{mb} are respectively, the gate, source, drain and bulk transconductances and v_G, v_S, v_D and v_B represent small variations in the gate, source, drain and bulk voltages, respectively, given by (24), (25), (26)

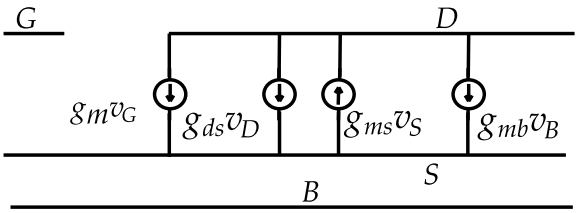

FIGURE 12. Small-signal equivalent circuit of a MOS transistor.

and (27),

$$g_m = \frac{\partial I_D}{\partial V_G}, \tag{24}$$

$$g_{ms} = -\frac{\partial I_D}{\partial V_S}, \tag{25}$$

$$g_{ds} = \frac{\partial I_D}{\partial V_D}, \tag{26}$$

$$g_{mb} = \frac{\partial I_D}{\partial V_B}. \tag{27}$$

The gate transconductance, g_m, is one of the main characteristics of the transistor on which designers put a lot of attention to describe their circuits and ensure their functionality since it is related to the main performances including voltage and current transfer functions, gain, noise expressions, filtering, and impedances.

In addition, an accurate model of the second and third derivative of I_D with respect to the gate voltage, for instance, g_{m2} and g_{m3}, is important when it comes to linearity studies that take part at an early stage of circuit design. In fact, g_{m2} and g_{m3} are directly related to the linearity performance, from the harmonic distortion to the compression point and the intermodulation products. As a design-oriented model, the proposed model with its two versions, bulk and FD-SOI, introduces simple expressions of the transconductances and their derivatives to provide designers with a complete analytical kit that is simple to handle and to run simple and fast calculations or build systematic design algorithms.

For X standing for one of the transistor terminals, and v_X for the corresponding potential normalized to the thermal voltage ϕ_t, a generic expression of the first derivative of the normalized current i_d can be expressed as (28), as shown at the bottom of the next page.

Considering the gate transconductance, $X = G$, and denormalizing the current and voltage, the g_m expression, valid in all regions, has been derived to yield (32), as shown at the bottom of the next page.

In the same way, considering the drain node, $(X = D)$, the output conductance can be expressed as (33), shown at the bottom of the next page.

The current efficiency g_m/I_D of the transistor, associated with the operation region of the device, can be derived as a function of the charge densities (34), as shown at the bottom of the next page.

Similarly, the generic expression of the second derivative can be easily derived, yielding (35), as shown at the bottom of the next page. Hence, by referring to the gate node, the current second derivative g_{m2} can be identified (37), as shown at the bottom of the next page.

To conclude, the third-order derivative gives (38), as shown at the bottom of the next page.

B. SMALL-SIGNAL MODEL VALIDATION

The model has been tested for $V_{DS} = 250$, 500, and 1000 mV to capture the saturation region, targeting simple and fast sizing of circuits such as amplifiers. It is important for this kind of circuit to have a first approximation of $g_{m1}, g_{m2}, and g_{m3}$. This allows the designers to tune specifically a parameter to improve the performance in a comprehensive way thanks to the detailed analytical derivation and the accurate device description. Fig. 13 displays the comparison results for the transistor with $L = 60$ nm. The 5PM/6PM relative error with respect to the measurements is shown in the right axis. The current derivatives are plotted with respect to the inversion coefficient i_d. As shown in Fig. 13, the shape of all the quantities is well captured by the model for different bias conditions. For the transconductance g_m, a maximum relative error of 15% is noticed with respect to the measurements, with very small deviations in the weak and moderate inversion regions ($i_d < 10$). Also, the g_{m2} and g_{m3} are well estimated in the different inversion regions; especially, the linearity sweet spot for which $g_{m3} = 0$ is well approximated by the model.

VI. CIRCUIT EXAMPLES AND SIMULATION RESULTS

A. INVERTER

Fig. 14 shows the schematic of the inverter, which, herein, comprises LVT transistors of the IHP PDK with the geometry and extracted parameters presented in Table 1.

Fig. 15 shows the simulated voltage transfer characteristic (VTC) and the short-circuit current I_{SC} for three values of the supply voltage. The DC characteristics of the inverter using ACM2 present results very similar to PSP's.

An important characteristic of a CMOS inverter is the high-to-low transition time, which requires knowledge of the transistor capacitances for its evaluation. To properly compare the ACM2 and PSP models, 100 fF was included as a load capacitance of the inverter. A voltage step was applied to the inverter input to determine the high-to-low transition at $V_{DD} = 1.5$ V. Fig. 16 shows both the output and the pull-down current for the PSP and ACM2 models. Note the remarkable agreement between the simulation results obtained from the PSP and ACM2 models.

B. RF CIRUITS: LNA DESIGN

In order to validate the proposed design-oriented model and its small-signal set of equations, a RF LNA circuit is designed in the 28 nm FD-SOI CMOS technology based on analytical equations followed by a comparison with the UTSOI2 PDK model. As it will be shown, the simplicity of the proposed design-oriented model allow us to analytically

explore the LNA design space to find an optimum solution. Common-source-based LNA topologies have been used as demonstrators for other versions of the model [28], [29], [30], in this work the LNA shown in Fig. 17, consists in a single-stage common gate (CG) single-ended amplifier. The CG transistor transconductance g_{m1} is set to match the real part of the input impedance, $R_S = 50\,\Omega$, that can be expressed as,

$$Zin = \frac{1}{g_{m1} + \frac{1+L_s(C_s+C_{gs1})s^2}{L_S s}}, \tag{39}$$

On the other hand, a degenerative LC network is inserted at the source node to cancel out the impedance imaginary part together with the effect of C_{gs1} at the desired frequency f_0. The s-parameter S_{11} measures the quality of the input matching. It can be expressed as,

$$S_{11} = \frac{|Zin - Rs|}{|Zin + Rs|}, \tag{40}$$

where the input impedance Z_{in} is given by (39). Usually, S_{11} is designed for acceptable signal transmission, and the matching bandwidth is defined as the frequency range where S_{11} is below $-10\,\text{dB}$. Assuming a perfect input matching ($g_m = 1/Rs$) at f_0, the corner frequencies where the $-10\,\text{dB}$ S_{11} limit is achieved can be computed as,

$$f_{S_{11}=-10dB} = \frac{f_0}{3}\sqrt{9 + 2Zr^2\left(1 \pm \sqrt{1 + \frac{9}{Zr^2}}\right)}, \tag{41}$$

where Zr is the ratio of the relative characteristic impedance of the LC source resonator to the source resistance Rs, given by,

$$Zr = \frac{Z_{LC}}{Rs}. \tag{42}$$

The matching BW (BW_{S11}) is the difference between the two solutions of the equation ($f_{S11=-10\,dB}$). It is worth noting that the degeneration inductor finite quality factor $QLs > 5$ is

$$g_X = \frac{\partial i_d}{\partial v_X} = \frac{2\,(1+q_s)\,\frac{\partial q_s}{\partial v_X} - 2\,(1+q_d)\,\frac{\partial q_d}{\partial v_X} - i_d\,\zeta\left(\frac{\partial q_s}{\partial v_X} - \frac{\partial q_d}{\partial v_X}\right)}{1+\zeta\,(q_s - q_d)} \tag{28}$$

With $\partial q_s/\partial v_X$ and $\partial q_d/\partial v_X$ are the charge density derivatives expressed as,

$$\frac{\partial q_{s(d)}}{\partial v_G} = \frac{1}{n}\frac{q_{s(d)}}{1+q_{s(d)}} \tag{29}$$

$$\frac{\partial q_{s(d)}}{\partial v_{D(S)}} = \frac{\sigma}{n}\frac{q_{s(d)}}{1+q_{s(d)}} \tag{30}$$

$$\frac{\partial q_{d(s)}}{\partial v_{D(S)}} = \left(\frac{\sigma}{n} - 1\right)\frac{q_{d(s)}}{1+q_{d(s)}} \tag{31}$$

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{I_S}{\phi_t} g_G = \frac{I_S}{n\phi_t}\frac{2(q_s - q_d) - i_d\,\zeta\left(\frac{q_s}{1+q_s} - \frac{q_d}{1+q_d}\right)}{1+\zeta\,(q_s - q_d)} \tag{32}$$

$$g_{ds} = \frac{I_S}{\phi_t} g_D = \frac{I_S}{n\phi_t}\frac{2(q_s\sigma - q_d(\sigma - n)) - i_d\zeta\left(\sigma\frac{q_s}{1+q_s} - (\sigma - n)\frac{q_d}{1+q_d}\right)}{1+\zeta(q_s - q_d)} \tag{33}$$

$$\frac{g_m}{I_D} = \frac{1}{n\phi_t}\left(\frac{2}{2+q_s+q_d} - \frac{q_s - q_d}{(1+\zeta(q_s - q_d))(1+q_s)(1+q_d)}\right) \tag{34}$$

$$g_{X2} = \frac{\partial^2 i_d}{\partial {v_X}^2} = \frac{2\left(\frac{\partial q_s}{\partial v_X}\right)^2 + 2\,(1+q_s)\,\frac{\partial^2 q_s}{\partial {v_X}^2} - 2\left(\frac{\partial q_d}{\partial v_X}\right)^2 - 2\,(1+q_d)\,\frac{\partial^2 q_d}{\partial {v_X}^2} - \zeta\left[g_X\left(\frac{\partial q_s}{\partial v_X} - \frac{\partial q_d}{\partial v_X}\right) + i_d\left(\frac{\partial^2 q_s}{\partial {v_X}^2} - \frac{\partial^2 q_d}{\partial {v_X}^2}\right)\right]}{1+\zeta\,(q_s - q_d)} \tag{35}$$

With,

$$\frac{\partial^2 q_{s(d)}}{\partial {v_G}^2} = \frac{1}{n^2 q_{s(d)}(1+q_{s(d)})^3} \tag{36}$$

$$g_{m2} = \frac{I_S}{(n\phi_t)^2}\frac{2q_s^2 + q_s(1+q_s)^2 - 2q_d^2 + q_d(1+q_d)^2 - \zeta n g_G(q_s - q_d) - i_d(q_S^3 - q_d^3 + 3q_s^2 - 3q_d^2)}{(1+\zeta(q_s - q_d))^2} \tag{37}$$

$$g_{m3} = \frac{I_S}{(n\phi_t)^3}\left\{\frac{\frac{2q_s}{(1+q_s)^3} - \frac{2q_d}{(1+q_d)^3} - \zeta n^2 g_{G2}\left(\frac{q_s}{1+q_s} - \frac{q_d}{1+q_d}\right) - \zeta\left[2n g_G\left(\frac{q_s}{(1+q_s)^3} - \frac{q_d}{(1+q_d)^3}\right) + i_d\left(\frac{q_d(1-2q_d)}{(1+q_d)^5} - \frac{q_d(1-2q_d)}{(1+q_d)^5}\right)\right]}{1+\zeta\,(q_s - q_d)}\right\} \tag{38}$$

where $g_{Gn} = \frac{\partial^n i_d}{\partial {v_G}^n}$.

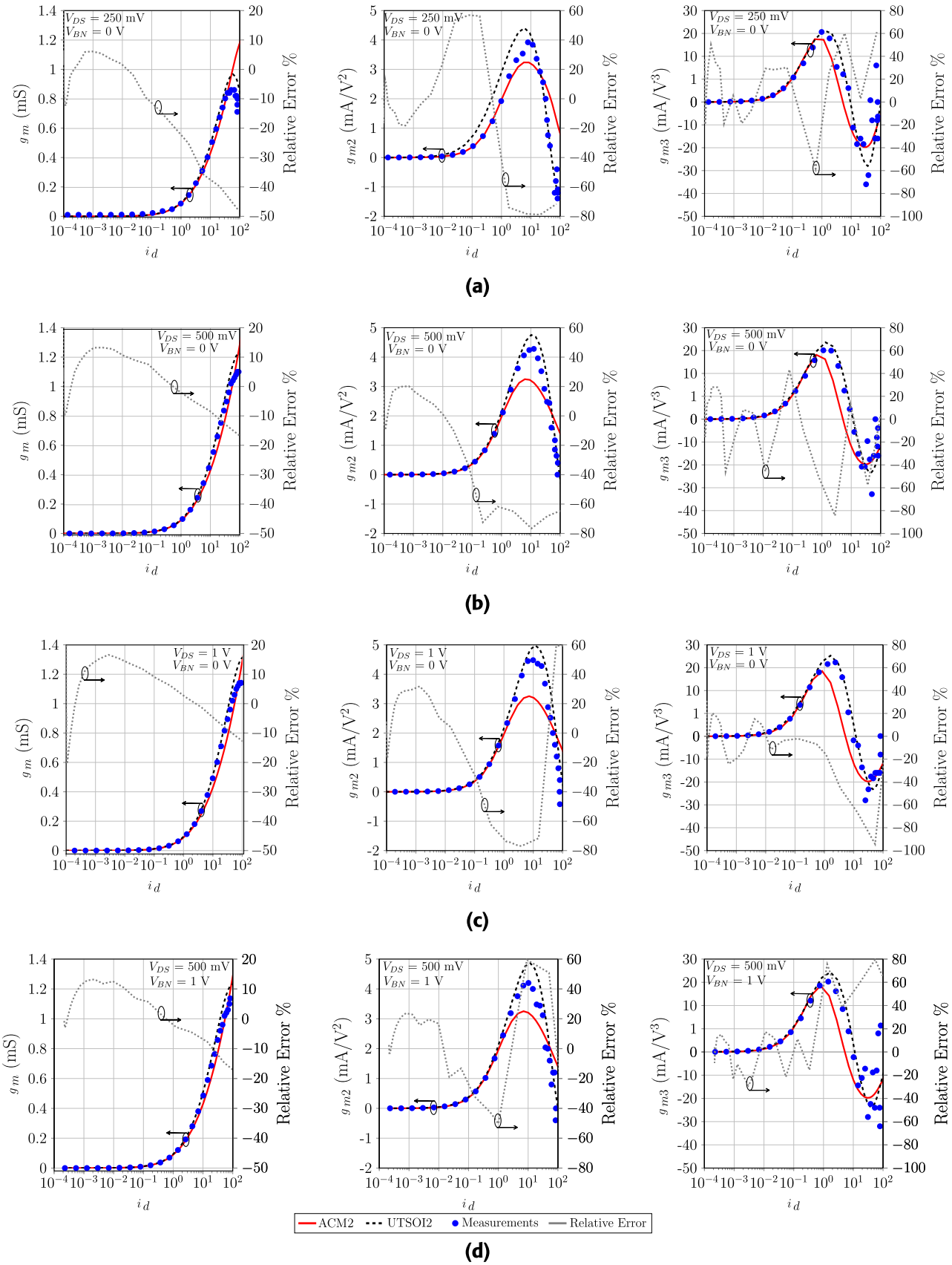

FIGURE 13. g_m, g_{m2} and $g_{m3} - i_d$ for a NMOS LVT FD-SOI transistor with $W/L = 1\ \mu$m/ 60 nm for different V_{DS} and body bias voltages *VBN* over the different inversion regions: (a) V_{DS} = 250mV, V_{BN} = 0V. (b)V_{DS} = 500mV, V_{BN} = 0V. (c) V_{DS} = 1V, V_{BN} = 0V. (d)V_{DS} = 500mV, V_{BN} = 1V.

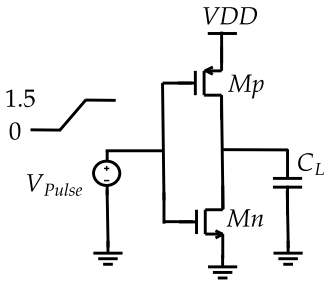

FIGURE 14. Schematic of the inverter.

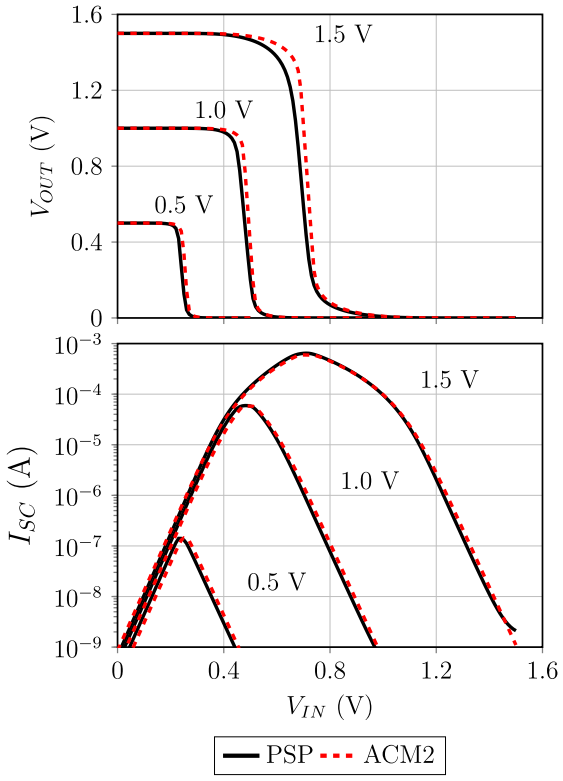

FIGURE 15. VTC and short-circuit current of a CMOS inverter for the PSP and ACM2 models.

sufficient not to cause significant error in the BW. BW_{S11} can be expressed as,

$$BW_{S11} = \frac{2}{3} f_0 \, Zr. \tag{43}$$

Finally, a load resistance sets the voltage gain, expressed as,

$$Av = R_L \frac{g_{m1}}{1 + R_L g_{ds1}}, \tag{44}$$

while maintaining enough headroom for the CG transistor and less impact on the noise figure NF. The gain bandwidth is defined as the 3 dB bandwidth around the maximum gain value. The CG gain achieves its maximum value at the matching frequency f_0. However, the degeneration inductor contributes to a gain reduction. The 3 dB corner frequencies

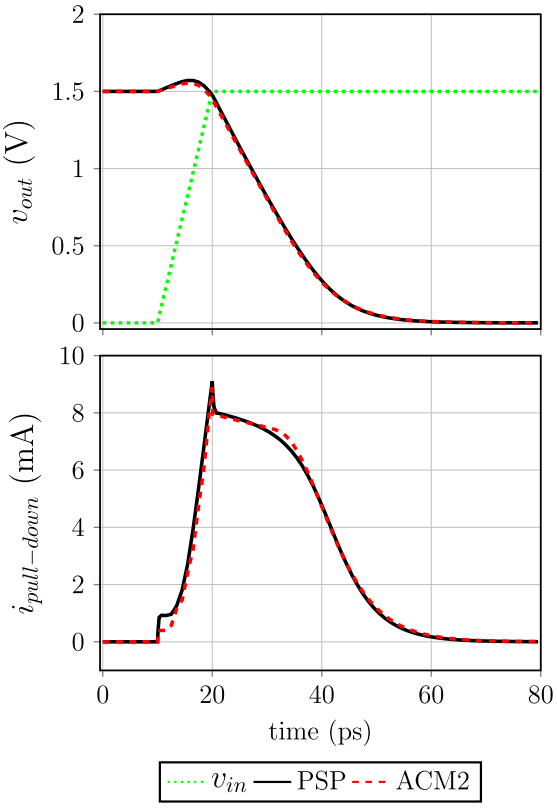

FIGURE 16. Output voltage (top) and pull-down current (bottom) in response to a step from 0 to 1.5 V, rise time of 10 ps, applied to the inverter for the PSP and ACM2 models.

for the gain can be expressed as,

$$f_{3dB} = f_0 \left(\sqrt{1 + Zr^2} \pm Zr \right). \tag{45}$$

Hence the 3-dB bandwidth can be calculated as,

$$BW_{3dB} = 2 f_0 \, Zr. \tag{46}$$

The noise figure NF considering the MOS transistor and Load resistor thermal noise sources is expressed as,

$$NF = 1 + \frac{\gamma}{R_s g_{m1}} + \frac{R_S}{R_L}(1 + \frac{1}{g_{m1} R_S})^2. \tag{47}$$

The noise figure under matching condition [31] can be simplified as,

$$NF = 1 + \gamma + \frac{4R_S}{R_L}, \tag{48}$$

where γ is the excess noise factor defined in [32]. Finally, regarding the LNA linearity, the CG IIP_3 considering the non-linearity contribution from g_{m1}, that is, assuming small signal operation and hence weak non-linearity conditions, is expressed as,

$$IIP_3 = 20 \log \left(\sqrt{\left| \frac{8 g_{m1}}{g_{m3}} \right|} \right). \tag{49}$$

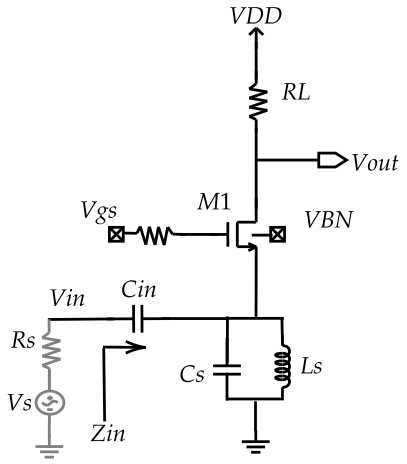

FIGURE 17. Simplified schematic of the CG LNA.

As can be seen in equations (39)-(49), the small signal performance of the CG LNA in Fig. 17 can be analytically expressed as a function of the transistor transconductance, g_{m1}, output conductance g_{ds1}, transconductance third-order non-linearity coefficient, g_{m3}, the transistor parasitic capacitances, and the value of the passive elements (resistors, capacitors and inductor) in the circuit. Using the proposed design-oriented model to bridge the gap between small-signal parameters and the transistor's dimensions and bias conditions, we can analytically evaluate equations (39)-(49) to find a solution to a given design target.

The M_1 transistor is designed in order to have a maximal g_{m1} slightly above 20 mS (up to 25 mS) to select a bias point as close as possible to the linearity sweet spot. In fact, in close proximity to the maximum g_{m1}, an inflexion point appears in the g_{m3} characteristic (Fig. 13) and it crosses 0 (the sweet spot), first in weak inversion, then in moderate to strong inversion regime. In this work, we take advantage of the accurate small-signal description of the transistor together with the 28 nm FD-SOI CMOS features (the body bias voltage) to finely tune the inversion coefficient in order to flatten the design space around the input matching points and target the highest linearity through the selection of minimal g_{m3} while consuming a limited power budget.

The circuit is designed at 2.4 GHz based on the small-signal characteristics from the model as well as the dynamic behavior description in Appendix A. The transistor inversion coefficient i_d is selected as the design variable. Based on the design considerations and the analytical description in (44)−(49), the circuit sizes are obtained and reported in Table 2. $L = 2Lmin = 60$ nm, for which the model was validated, is selected for high f_T and less variability and area trade-off.

The design space can be analytically explored thanks to the inversion coefficient i_d which is directly related to the overdrive voltage ($V_G - nV_S - V_T$). In this work, the model accuracy to track the transistor performance variation as a function of the four terminals including the

TABLE 2. LNA component sizes for $V_{DD} = 1$ V and $f_0 = 2.4$ GHz.

component	M1	RL	Cs	Ls	Cin
size	$75\mu m/60nm$	500Ω	2.8 pF	1.5 nH	10 pF

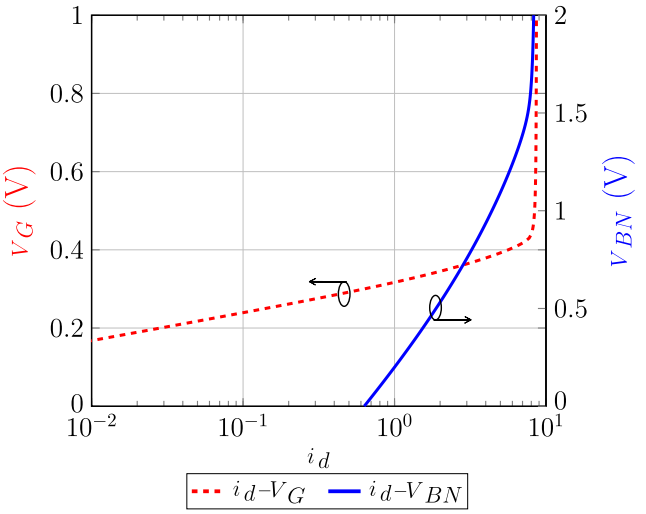

FIGURE 18. $V_G - i_d$ ($V_{BN} = 0$ V) and $V_{BN} - i_d$ ($V_G = 0.3$ V) for $V_{DS} = V_{DD} - R_L I_D$.

SOI-based technology is demonstrated. Applied to the LNA, two methods are shown to explore the bias voltage range and select the optimal working point for the best linearity, power, noise and gain performance while controlling the input matching. In Fig.18, the direct relationship between i_d and V_G and V_{BN} is shown. First, the transistor is biased for $V_{BN} = 0$ V. The LNA performance variations at $f_0 = 2.4$ GHz are shown in Fig. 19 from simulations using the UTSOI2 PDK and our ACM2 model based on equations (39)-(49). Setting $S_{11} < -10$ dB as matching condition, the design space is limited to 200 mV of gate voltage control (350 mV −550 mV). As expected, within this operation range, two perfect matching points can be selected ($g_{m1} = 20$ mS) and also two local linearity sweet spots can be addressed. However, the power consumption varies through a very sharp slope. Moreover, a fast alteration between the maximum and minimum IIP3 points occurs within a few V_G mVolts for which 4 dB of gain and NF variations are noticed. The weak performance controlability together with the ACM2 model accuracy are validated when comparing the analytical results to the simulated results using the PDK UTSOI2 model as shown in Fig. 19. The second alternative consists in exploring the same design space through the fine-control of the body bias voltage to tune the threshold voltage as in (20). Hence, the gate voltage is maintained constant at 300 mV for which the amplification operation starts. The LNA performance variations at $f_0 = 2.4$ GHz are shown in Fig. 20. For the same matching criteria, the targeted design space is obtained through more than $1V$ tuning range. This

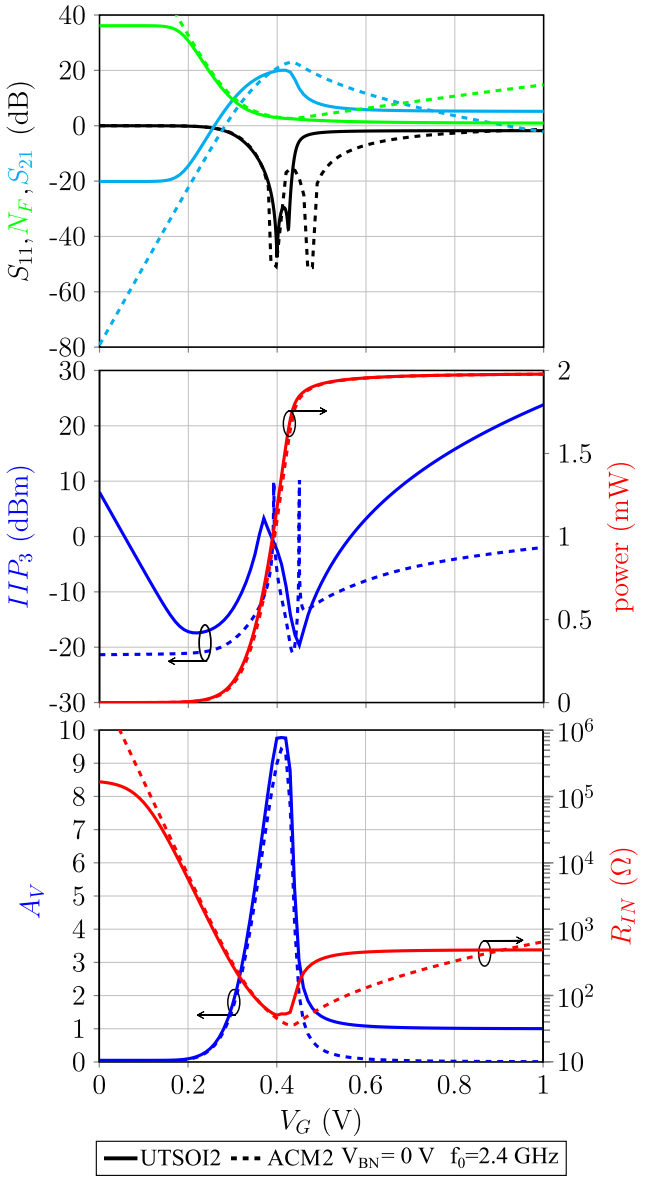

FIGURE 19. Performance variations at $f_0 = 2.4$ GHz and $V_{BN} = 0$ V as function of V_G from ACM2 and UTSOI2 PDK models.

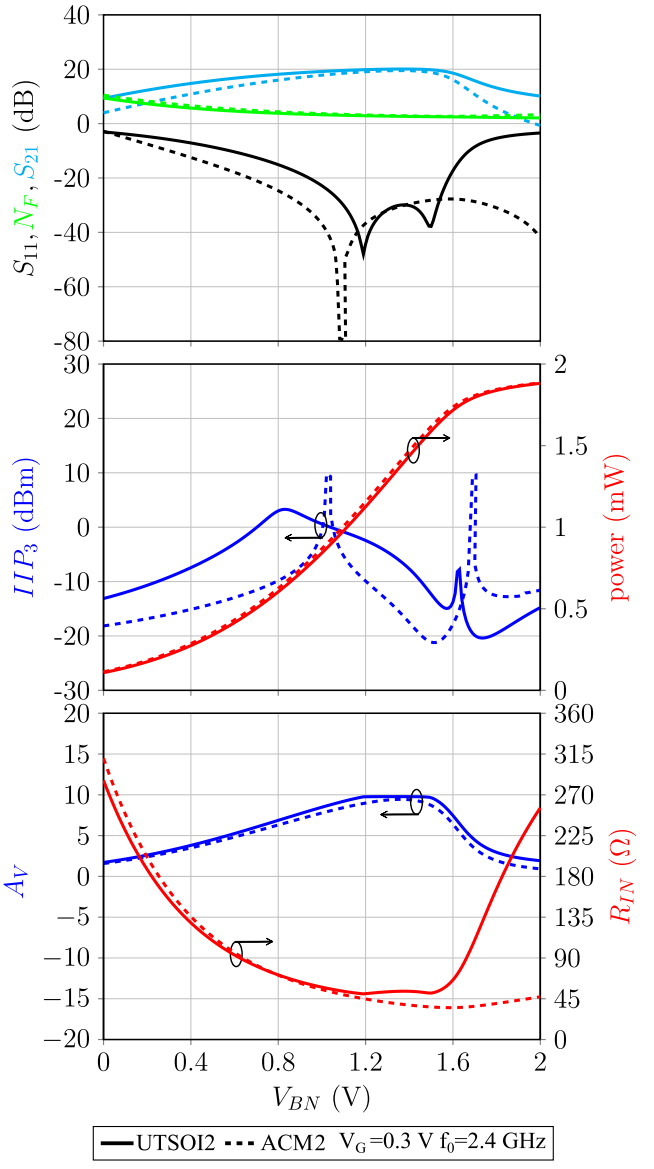

FIGURE 20. Performance variations at $f_0 = 2.4$ GHz and $V_G = 0.3$ V as function of V_{BN} from ACM2 and UTSOI2 PDK models.

allows to finely select the bias point for the maximum IIP3 while maintaining good noise and gain results. In addition, different trade-offs can be easily addressed for a given power budget. As it is shown in Fig. 19 and 20, the proposed model, based on a simple set of DC parameters, accurately tracks the LNA RF performance variations over wide tuning ranges for both bulk ($V_{BN} = 0$ V) and SOI cases using an advanced technology such as the 28 nm CMOS FD-SOI CMOS. Asymptotic behavior of the IIP_3 sweet spots and S_{11} perfect matching are obtained with the analytical results since they are based on ideal calculations. In the real case, these values do not tend to infinite and achieve defined extrema as shown using the PDK simulations. The results obtained with the ACM2 model are in good agreement with the UTSOI2 results despite local discrepancies outside the amplification range of V_G. This is mainly due to the validity of the simple analytical description of the circuit.

In order to verify the frequency performance, a particular working point is selected at $V_G = 300$ mV and $V_{BN} = 0.9$ V. As shown in Fig.21, the $S_{11} = -18.35$ dB at $f0 = 2.4$ GHz while the $S_{21} = 18.7$ dB and the $NF = 3.5$ dB. In this case, for $S_{11} = -18.35$ dB, $Zr = 0.43$ (41)-(42), and then, BW_{S11} is estimated to be 1 GHz. As shown in Fig. 21.a, 800 MHz of matching bandwidth is obtained through simulation, in good agreement with the analytical estimation (43). Moreover, the 3 dB gain bandwidth is $BW_{3dB} = 2.06$ GHz is in good agreement with the simulated 2 GHz bandwidth [1.5, 3.44] GHz as shown in Fig. 21.a.

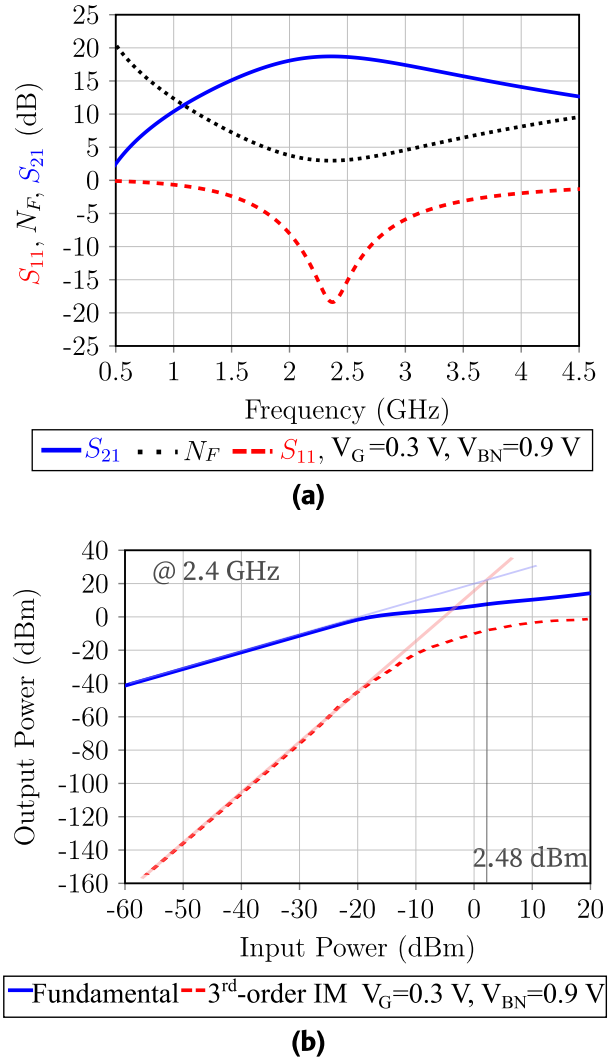

FIGURE 21. LNA S-parameters variation with the frequency (a) and IIP3 (b) at 2.4 GHz, $V_G = 0.3$ V, $V_{BN} = 0.9$ V and $V_{DD} = 1$ V.

As indicated in Fig.21, the *IIP*3 is as high as 2.48 dBm and the power consumption is 716 μW only. It is noticed that a different trade-off can be addressed based on the analytical analysis targeting 2.4 dB of NF with more than 20 dB of gain while relaxing the linearity and power requirements.

VII. CONCLUSION

In this paper, the effect of saturation velocity is included in the charge control equation through the saturation carrier charge, in order to avoid the definition of a saturation voltage and the use of interpolation functions to link the triode and saturation regions. Consequently, the new model consists of single-piece equations, derived from physics. The new 5PM for bulk and 6PM for FD-SOI are validated against experimental results and circuit simulations for a logic inverter in bulk technology and an LNA in FD-SOI. The simplicity of the model equations and the reduced number of parameters make the new model attractive for newcomers in the design area, as well as for the experienced ones in the pre-simulation phase of a design flow.

To summarize the pros and cons of the proposed ACM2 design-oriented model, Table 3 shows a comparison of the model main features with the PDK compact models, 4-parameter EKV/ACM models and 7-parameter-based ACM model. The comparison is conceptually illustrated using "+" and "−" signs, representing the inclusion or not of the feature, respectively.

APPENDIX A
CHANNEL CHARGE AND ASSOCIATED CAPACITANCES

In ACM model the inversion charge density Q_I is linearly dependent on the surface potential ϕ_s for a constant gate-to-bulk voltage [17], [19].

$$dQ_I = nC_{ox}d\phi_s. \tag{50}$$

The drain current is calculated using the expression below: [19]

$$I_D = \mu W\left(-Q_I\frac{d\phi_s}{dy} + \phi_t\frac{dQ_I}{dy}\right), \tag{51}$$

where y is the coordinate along the channel length.

The carrier velocity saturation effect is included in the mobility model as in [17], [18],

$$\mu = \frac{\mu_s}{1+\frac{\mu_s}{v_{sat}}\frac{d\phi_s}{dy}}. \tag{52}$$

Combining (50), (51) and (52) we obtain,

$$dy = -\frac{\mu_s W}{nC_{ox}I_D}\left(Q_I - nC_{ox}\phi_t + \frac{I_D}{Wv_{sat}}\right)dQ_I. \tag{53}$$

We define a virtual charge density as,

$$Q_V = Q_I - nC_{ox}\phi_t + \frac{I_D}{Wv_{sat}}. \tag{54}$$

Since n and I_D are constant along the channel $dQ_V = dQ_I$, consequently (53) can be rewritten as,

$$dy = -\frac{\mu_s W}{nC_{ox}I_D}Q_V dQ_v. \tag{55}$$

Integrating (55) we obtain the drain current in terms of the virtual charges at the source and drain as,

$$I_D = \frac{\mu_s W}{C_{ox}L}\frac{Q_{VS}^2 - Q_{VD}^2}{2n}. \tag{56}$$

The total charge stored in the channel Q_{ch} is easily calculated in terms of the virtual charges at source and drain using (54), (55) and (56).

$$\begin{aligned} Q_{ch} &= W\int_0^L Q_I dy \\ &= WL\left(\frac{2}{3}\frac{Q_{VS}^2 + Q_{VS}Q_{VD} + Q_{VD}^2}{Q_{VS}+Q_{VD}}\right. \\ &\quad \left. + nC_{ox}\phi_t - \frac{I_D}{Wv_{sat}}\right). \end{aligned} \tag{57}$$

TABLE 3. Comparison of MOSFET models.

Features	PSP (Bulk) model	UTSOI2 (FD-SOI) model	4PM EKV model (saturation region)	4PM-ACM model (low-voltage)	7PM-ACM model	This work
One-piece model: Transition triode to saturation regions and weak to strong inversions	-	-	-	+	-	+
Analytical small-signal model	-	-	+	+	+	+
Analytical quasi-static dynamic model	-	-	+	+	-	+
Number of DC parameters	tens of	tens of	4	4	7	5/6
Body bias	+	+	-	-	-	+
Explicit VD dependency	+	+	-	+	+	+
I_D error [%] (*)	8.13	6.86	-	32.73	4.46	16.83 - Bulk 12.81 - FD-SOI
Main short-channel effects						
Velocity saturation	+	+	+	-	+	+
DIBL	+	+	-	+	+	+
Mobility reduction	+	+	-	-	+	-
Channel length modulation	+	+	-	-	+	-

(*) The mean drain current error was calculated from a I_D vs V_G characteristic in the saturation region, using the formula $\frac{1}{N}\sum_1^N \left|\frac{I_{D,model}-I_{D,meas}}{I_{D,meas}}\right|$, N is the number of data points.

In the limit case of velocity saturation along the whole channel,

$$Q_{VS} \approx Q_{VDsat} \approx -nC_{ox}\phi_t. \tag{58}$$

since $I_{Dsat} = -Wv_{sat}Q_{Dsat}$ [18], [19]

Consequently, (57) reduces to,

$$\begin{aligned} Q_{ch} &\approx WL\left(Q_{VDsat} + nC_{ox}\phi_t\right) - \frac{LI_D}{v_{sat}} \\ &\approx -\frac{LI_D}{v_{sat}} \end{aligned} \tag{59}$$

C_{gs} is calculated as [19]

$$C_{gs} = -\frac{\partial Q_G}{\partial V_S} = \frac{1}{n}\frac{\partial Q_{ch}}{\partial V_S} \tag{60}$$

Applying the chain rule to (57),

$$\frac{\partial Q_{ch}}{\partial V_S} = \frac{\partial Q_{ch}}{\partial Q_{VS}}\frac{\partial Q_{VS}}{\partial V_S} + \frac{\partial Q_{ch}}{\partial Q_{VD}}\frac{\partial Q_{VD}}{\partial V_S} + \frac{\partial Q_{ch}}{\partial I_D}\frac{\partial I_D}{\partial V_S}, \tag{61}$$

$$\frac{\partial Q_{ch}}{\partial Q_{VS}} = \frac{2}{3}WL\frac{Q_{VS}^2 + 2Q_{VS}Q_{VD}}{(Q_{VS}+Q_{VD})^2} = \frac{2}{3}WL\frac{1+2\alpha}{(1+\alpha)^2}, \tag{62}$$

where,

$$\alpha = \frac{Q_{VD}}{Q_{VS}}. \tag{63}$$

From (54) and (57),

$$\frac{\partial Q_{VS}}{\partial V_S} = \frac{\partial Q_S}{\partial V_S} - \frac{g_{ms}}{Wv_{sat}} \tag{64a}$$

$$\frac{\partial Q_{VD}}{\partial V_S} = -\frac{g_{ms}}{Wv_{sat}}. \tag{64b}$$

Finally, from (14),

$$\frac{\partial Q_S}{\partial V_S} = nC_{ox}\frac{Q_S}{Q_S - nC_{ox}\phi_t}. \tag{65}$$

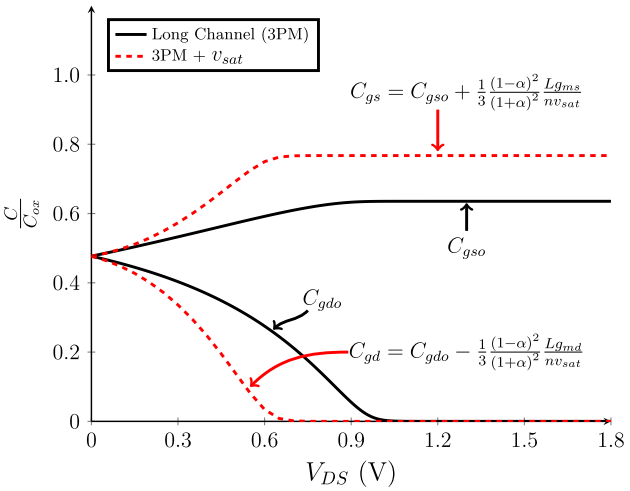

FIGURE 22. Intrinsic capacitances including velocity saturation.

Combining (60),(61), (62), (64), (65),

$$C_{gs} = C_{gso} + \frac{1}{3}\frac{(1-\alpha)^2}{(1+\alpha)^2}\frac{Lg_{ms}}{nv_{sat}}, \tag{66}$$

where,

$$C_{gso} = \frac{2}{3}WLC_{ox}\frac{1+2\alpha}{(1+\alpha)^2}\frac{q_s}{q_s+1}. \tag{67}$$

In strong inversion $q_s \gg 1$ and saturation $\alpha = 0$, thus $C_{gso} = \frac{2}{3}WLC_{ox}$.

For velocity saturation along the whole channel, we can estimate C_{gs} from (59) as,

$$C_{gs} = -\frac{1}{n}\frac{L}{v_{sat}}\frac{dI_D}{dV_S} = \frac{1}{n}\frac{Lg_{ms}}{v_{sat}}. \tag{68}$$

Since for a uniform channel $C_{gs} \approx WLC_{ox}$, we can estimate the second term in (66) as $\frac{1}{3}WLC_{ox}$.

In a similar way, we can calculate C_{gd} as,

$$C_{gd} = C_{gdo} - \frac{1}{3}\frac{(1-\alpha)^2}{(1+\alpha)^2}\frac{Lg_{md}}{nv_{sat}}, \tag{69}$$

where,

$$C_{gdo} = \frac{2}{3}WLC_{ox}\frac{\alpha^2+2\alpha}{(1+\alpha)^2}\frac{q_d - q_{dsat}}{q_d - q_{dsat}+1}. \tag{70}$$

Fig. 22 shows the effect of velocity saturation on C_{gs} and C_{gd}. The complete set of capacitive coefficients is available at [25].

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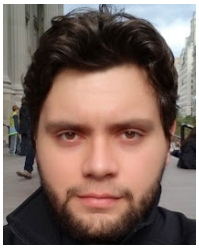

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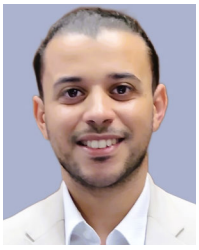

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