Design and Testing of a 32-kHz Frequency Divider Chain Operating at VDD = 76 mV

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***Abstract*—In this paper, we describe the design of a minimalist standard cell library (inverter, NAND and D flip-flop) in a conventional 130 nm CMOS technology optimized for operation at VDD = 90 mV, in order to transcend the past limits of low voltage standard cells libraries. The classical six-transistor CMOS Schmitt trigger was used as the basic cell of the logic family. Experimental results for a 15-stage frequency divider chain demonstrate operation at 32 kHz with a supply voltage of only 76 mV.**

***Index Terms*—standard cells, schmitt trigger, CMOS, ultra-low voltage, subthreshold**

I. Introduction

WIRELESS sensor nodes as well as wearable and implantable devices require very low power budgets to operate from either a small battery or some energy harvesting mechanism, or both [1]. In many cases, thermal or electrochemical harvesting devices provide very low voltages of the order of 100 mV or even lower [2]- [3]. Recent papers have shown that CMOS electronics can operate at such low supply voltages [4]- [6]. In this paper, we build on these recent findings with the design of an optimized minimalist ultra-low-voltage CMOS standard cell library and report experimental results obtained with the first fabricated prototypes. In Section II, the optimum design of an ultra-low-voltage (ULV) inverter is proposed and a minimalist ULV standard cell library is presented in Section III. The chip design is summarized in Section IV and experimental results are reviewed in Section V. Conclusions are drawn in Section VI.

II. Optimum Design of an Ultra-Low-Voltage Inverter

Fig. 1 shows the voltage transfer characteristic (VTC) of a CMOS Schmitt trigger (ST) with balanced PMOS and NMOS subcircuits under ULV operation [7]. The VTC shows hysteresis for VDD = 100 mV but not for VDD = 70 mV and VDD = 50 mV. As demonstrated in [8], the ST of Fig. 1 cannot theoretically present hysteresis for supply voltages below 75 mV, due to the lack of voltage gain. In practice, due to the non-perfect balance between the NMOS and PMOS networks and slope factors larger than unity, hysteresis can only appear for over 100 mV of supply.

For ULV operation, both nMOS and pMOS operate in weak inversion (WI). The MOS transistor drain current in WI is given by [7]. Where $n_{N(P)}$ is the slope factor and φ_t is the thermal voltage. G, S, D and B are the gate, source, drain and bulk nodes, respectively. The transistor current scaling factor, $I_{N(P)}$, in (1), which represents the transistor strength, is dependent on both the technology parameters and dimensions. For a balanced (symmetrical) ST, $I_{N0} = I_{P0} = I_0$, $I_{N1} = I_{P1} = I_1$, $I_{N2} = I_{P2} = I_2$ and $n_N = n_P = n$.

$$I_{DN(P)} = I_{N(P)} e^{\frac{V_{GB(BG)}}{n_{N(P)}\phi_t}} \left(e^{\frac{-V_{SB(BS)}}{\phi_t}} - e^{\frac{-V_{DB(BD)}}{\phi_t}} \right) \quad (1)$$

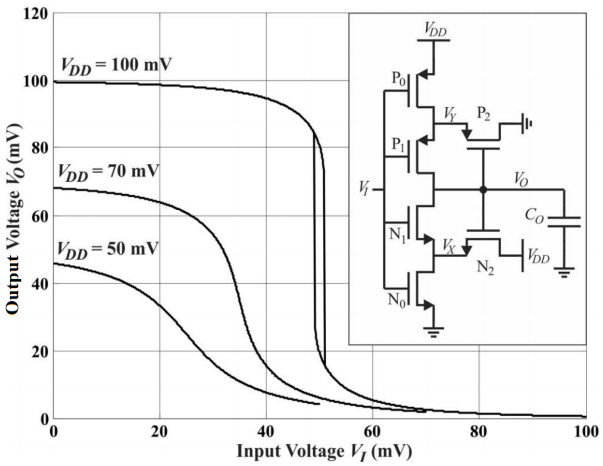

Figure 1. Voltage transfer characteristics of the symmetrical Schmitt trigger.

The voltage gain of the ST circuit around VDD/2, given by (2) [8], is a function of the supply voltage VDD and ratios I_1/I_0 and I_2/I_0. Fig. 2 shows the gain calculated using (2) for VDD = 60 mV. This extremely low voltage was selected in order to explore the limits of the design space. The value of $I_1/I_0 = I_2/I_0 = 0.5$ was chosen for layout convenience and because the voltage gain of -1.73 for these ratios is close to the optimum gain of -1.93.

$$\frac{v_o}{v_i} = \frac{\left(2 + \frac{I_0}{I_2} + \frac{I_1}{I_2} - \frac{I_2}{I_0} e^{\frac{-V_{DD}}{\varphi_t}}\right)\left(1 - e^{-\frac{V_{DD}}{2\varphi_t}}\right)}{1 - \left(2 + \frac{I_0}{I_2} + \frac{I_1}{I_2} + \frac{I_2}{I_0}\right) e^{\frac{-V_{DD}}{2\varphi_t}} - \left(1 + \frac{I_1}{I_0}\right) e^{\frac{-V_{DD}}{\varphi_t}}} \quad (2)$$

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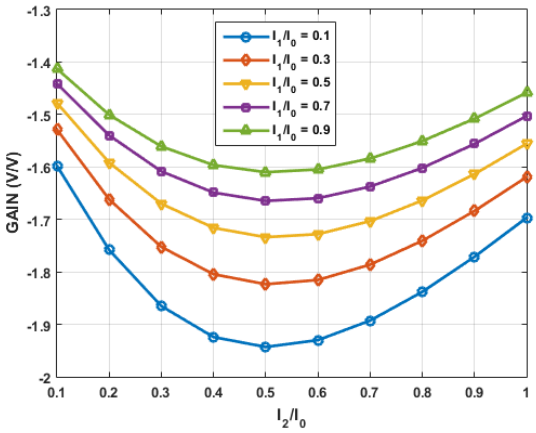


Figure 2. Voltage gain of the ST inverter as a function of I_2/I_0.

The channel length was determined from the simulation results for the operating frequency of an ST-based 11-stage ring oscillator. Due to the reverse short-channel effect, in WI the maximum operating frequency does not occur for the minimum channel length [6], [9]. In the simulated circuits, the ratio of the widths of the corresponding p- and n-channel transistors is 5 to 1, in order to balance their current strengths for a supply voltage of 90 mV. As can be seen in Fig. 3, the maximum oscillation frequency is attained for L=420 nm, but for L=300 nm the reduction in the frequency is 22%.

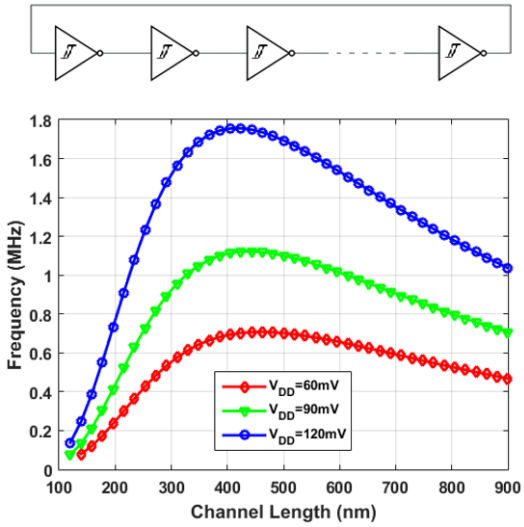
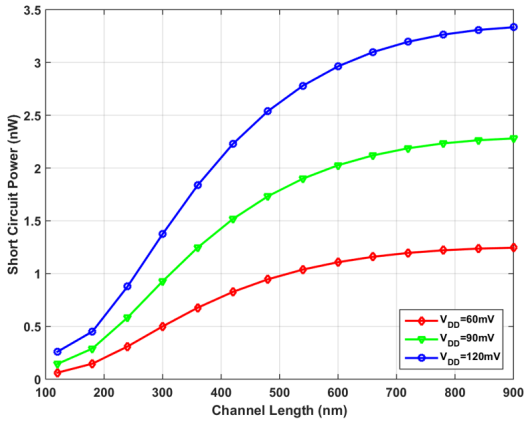


Figure 3. Oscillation frequency as a function of the channel length.

On the other hand, the short-circuit dissipation, shown in Fig. 4 is 60% larger for L=420 nm than for L=300 nm. Consequently, we chose L=300 nm for a trade-off between velocity and static power dissipation, which is of paramount importance for ULV operation. Another very important characteristic of the ST inverter is that it is less sensitive to technology parameter variations than the conventional inverter, since both the pull-up and pull-down circuits are composed of both nMOS and pMOS [7] transistors. Consequently, the yield of ST logic can be much higher than that of the conventional logic in ULV operation, as we will show in Section III.



L	t_p	P_{total}
$300nm$	$82.67ns$	$499.6pW$
$420nm$	$64.75ns$	$826.4pW$

Figure 4. Short-circuit power of an ST inverter as a function of the channel length.

Fig. 5 shows the layouts of both the conventional inverter and the ST circuit. The dimensions of the transistors of the ST inverter are given in Table I.

Table I
ST INVERTER DIMENSIONS

PMOS Network	NMOS Network
$W_{P0} = 3\mu m$ $L_{P0} = 300nm$	$W_{N0} = 600nm$ $L_{N0} = 300nm$
$W_{P1} = 1.5\mu m$ $L_{P1} = 300nm$	$W_{N1} = 300nm$ $L_{N1} = 300nm$
$W_{P2} = 1.5\mu m$ $L_{P2} = 300nm$	$W_{N2} = 300nm$ $L_{N2} = 300nm$

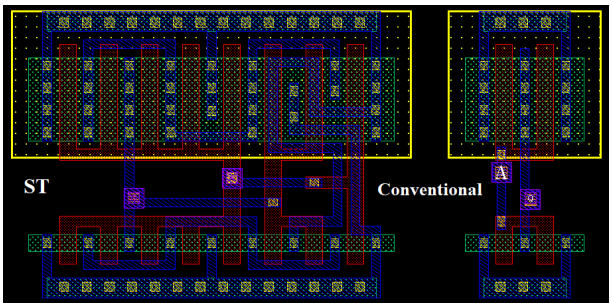


Figure 5. Layouts of both the ST inverter and conventional inverter.

III. A MINIMALIST STANDARD CELL LIBRARY

As noted in [9], the I_{on}/I_{off} ratio, where I_{on} the active current and I_{off} is the leakage current, is severely degraded for low supply voltages, with a serious risk to the correct operation of the logic gates. One main strategy to mitigate the

reduction in I_{on}/I_{off} is to avoid gates with more than three inputs [9]. Consequently, in order to improve the operation at ULV and to reduce the design effort, we designed only a small library with two input NAND and NOR gates and a D flip-flop.

The sizes of the transistors of the NAND gate are indicated in Fig. 6. The transistors were sized in order to keep the worst-case pull-up and pull-down current strengths of the NAND equals to those of the inverter.

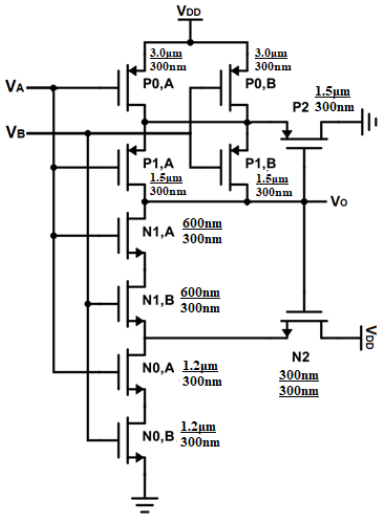


Figure 6. Schematic and dimensions of the NAND-ST.

The D flip-flop, shown in Fig. 7, is based on [10], but supplementary inverters were included to improve the operation robustness at ULV. Two divide-by-four circuits employing the D-type flip-flops of Fig. 7, connected as shown in Fig. 8, were realized. Table II compares values of delay, power and area of the classical logic and ST logic. Table III shows the results of 200 Monte Carlo simulations considering process, voltage, temperature variability and mismatch of two frequency dividers, one implemented with standard logic and the other with ST logic. As regards yield at low supply voltages, the advantage of the ST logic over conventional logic for very low voltages is crystal clear.

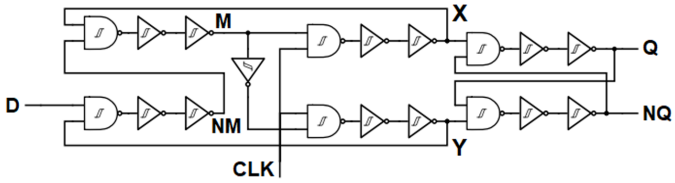


Figure 7. Schematic of the D flip-flop.

IV. TEST CHIP

A test chip to compare conventional logic with ST logic was fabricated in a 130 nm technology. The inverters, NAND2 and a frequency division chain of 15 stages were implemented with both conventional CMOS and ST logic.

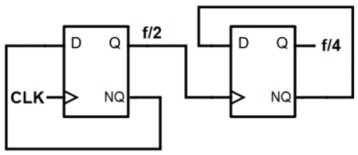


Figure 8. Schematic of the ST-based frequency divider with 2 stages.

Table II
SIMULATED COMPARISON OF DELAY, POWER AND AREA OF THE CLASSICAL AND ST LOGIC FAMILY FOR A SUPPLY VOLTAGE OF $90mV$

	Delay [ns]	**Power [nW]**	**Area [μm^2]**
Inv	6.76	0.34	14.08
Inv-ST	51.34	0.93	36.90
Nand	9.02	0.57	19.61
Nand-ST	54.01	1.57	57.61
Div	544.55	98.25	4125.14
Div-ST	6906.44	346.80	12986.31

The frequency divider chain in ST logic is shown on the top right of Fig. 9, while the conventional logic implementation is on the bottom left of the Fig. 9.

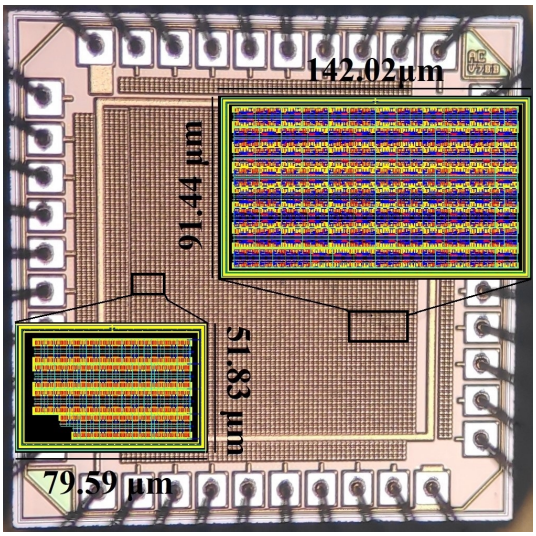


Figure 9. Micrograph of the test chip

V. EXPERIMENTAL RESULTS

The measured voltage transfer characteristics of the standard and ST inverters at very low supply voltages are shown in

Table III
YIELD OF THE FREQUENCY DIVIDERS

V_{DD}	**Yield-ST**	**Yield-Standard**
60mV	15.6%	0%
62.5mV	43.1%	0%
65mV	68.2%	0.7%
67.5mV	84.3%	4.9%
70mV	91.5%	16.4%

Fig. 10. Table IV compares the maximum voltage gains of two basic logic (inverter and NAND) gates. The superiority of the ST gates compared with the standard gates was clearly observed. Finally, the output signals of two frequency division chains at their minimum supply voltages are shown in Fig. 11 and Fig. 12.

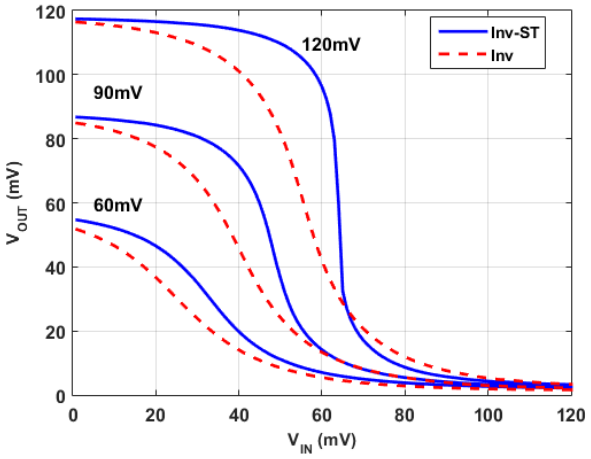


Figure 10. Measured voltage transfer functions of the classical and ST inverters.

Table IV
MEASURED GAINS OF CLASSICAL AND ST INVERTERS

Gain	Inv	Inv-ST	Nand	Nand-ST
$V_{DD} = 60mV$	-1.33	-1.64	-1.11	-1.31
$V_{DD} = 90mV$	-2.61	-5.37	-2.32	-4.18
$V_{DD} = 120mV$	-4.45	-27.32	-4.07	-17.92

The input frequency in both cases is 32.768 kHz. The ST logic operates correctly at a supply of 76 mV while the conventional logic requires 94 mV.

Figure 11. Output signals of the classical logic (upper wave) and ST logic (lower wave) frequency divider chains operating at 94mV

Figure 12. Output signals of both frequency divider chains at 76 mV of supply voltage. The classical logic (upper wave) does not operate properly, while the ST logic (lower wave) kept the signal of 1 Hz at 76 mV

VI. CONCLUSIONS

In this study, we designed a minimalist standard cell library based on the classical CMOS ST inverter, optimized for operation at a supply voltage of 90 mV. We verified the robustness of the designed ST logic family through DC and Monte Carlo simulations. The robustness of the ST library was verified through the measurement of two 2^{15} frequency divider chains, using either standard or ST logic. While the conventional logic operates from a minimum supply voltage of 94 mV, the ST logic operates from a minimum voltage of 76 mV. In the authors knowledge this is the lowest supply voltage for a sequential circuit. It can be concluded from the results obtained that, although the ST logic consumes more silicon area and increases the propagation time as compared to the standard logic, it allows the operation of standard cells from very low supply voltages, of the order of three times the thermal voltage. A future standard cell library will include three input NAND cells as well as other logic functions as in [9].

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