

Bridging the gap between design and simulation of low voltage CMOS circuits

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Abstract—This work proposes a simplified MOSFET model based on the Advanced Compact MOSFET (ACM) model, which contains only four parameters to assist the designer in understanding how the main MOSFET parameters affect the design. The 4-parameter model was implemented in Verilog-A to simulate different circuits designed with the ACM model. A CMOS inverter and a ring oscillator were designed and simulated, either using the 4-parameter ACM model or the BSIM model. The simulation results demonstrate that the 4-parameter model is very suitable for ultra-low-voltage (ULV) modeling. In the ultra-low-voltage domain, some of the secondary effects of the MOSFET are not relevant and thus not included in the 4-parameter model. A simplified MOSFET model for the ULV domain is of great importance to applications such as energy harvesting, sensor nodes for the Internet of Things, and always-on circuits.

Index Terms—ACM model, MOSFET modeling, circuit simulation, ultra-low-voltage

I. INTRODUCTION

Compact MOSFET models are essential for design and simulation of integrated circuits. Today's models began to be developed in the 1960s, when there were only long-channel devices. Through the scaling of semiconductor technologies, short-channel effects began to interfere with the circuit performance; thus, short-channel effects were included in the existing models in order to improve the design.

While BSIM is widely used in EDA tools to run MOS circuit simulations, its complexity, however, opens a gap between circuit simulation and the hands-on design, making it hard to understand how the main MOSFET parameters relate to the final results. Thus, it becomes interesting to provide simulators with inversion charge-based models, which are strongly founded on physics.

This work proposes a 4-parameter model based on the all-region Advanced Compact MOSFET model (ACM) model [1]-[2]. The authors in [3] explain the ACM model and how to design various analog MOS circuits based on the model.

In this work, the 4-parameter model was implemented using the Verilog-A description language to simulate circuits in the commercial Cadence® Virtuoso® simulator. Hardware description languages (HDLs), such as Verilog-A, were developed to provide various levels of behavioral modeling abstractions to designers and present the advantage of interchangeability with different simulators. Verilog-A is simple,

powerful, and targeted at analog hardware modeling due to its compact language [5].

This paper is organized as follows. Section II briefly introduces the 4-parameter ACM model. Section III shows the steps taken throughout the process of implementing the ACM model in the Verilog-A description. Section IV describes the methods to extract the model parameters. Section V shows simulation results of a CMOS inverter, a ring oscillator, and a self-biased current source (SBCS). Finally, the conclusions are drawn in Section VI.

II. THE 4-PARAMETER MODEL

The Advanced Compact MOSFET (ACM) model describes the electrical behavior of MOS transistors in all regions of operation.

The three main parameters of the ACM model are the specific current I_S , the threshold voltage V_{T0} and the slope factor n . Though these three parameters are usually enough to design a large set of circuits, a secondary effect called the drain-induced barrier lowering (DIBL) [4] completes the 4-parameter ACM. The DIBL is a very pronounced short-channel effect, but it cannot be ignored for long-channel transistors.

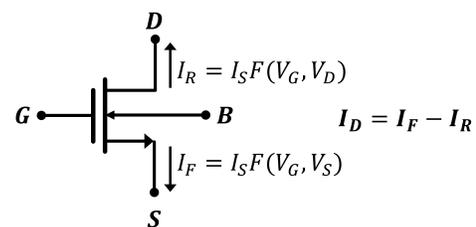


Fig. 1. Symmetric model of the NMOS transistor.

Fig. 1 presents the symbol of a n-channel MOSFET transistor and its four terminals: gate (G), source (S), drain (D) and bulk (B).

In the long-channel ACM model [3], the drain current I_D , as illustrated in Fig. 1, has two components: the forward current I_F and the reverse current I_R , both dependent on the voltage V_{GB} . I_F is also dependent on V_{SB} , while I_R is dependent on V_{DB} . This source-drain symmetry is depicted in (1).

$$I = I_F - I_R = I_S (i_f - i_r) \quad (1)$$

The specific (or normalization) current I_S is dependent on both geometry and technological parameters as given by (2), where μ is the carrier mobility, C_{ox} is the oxide capacitance per unit area, ϕ_t is the thermal voltage and n is the slope factor.

$$I_S = \mu C_{ox} n \frac{\phi_t^2 W}{2 L} \quad (2)$$

The normalized form of the unified charge-control model (UCCM), expressed in (3), establishes the relationship between the voltages at the device terminals and the normalized inversion charge density at the source (drain) $q_{IS(D)}$.

$$\frac{V_P - V_{S(D)B}}{\phi_t} = q_{IS(D)} - 1 + \ln q_{IS(D)} \quad (3)$$

$$q_{IS(D)} = \sqrt{1 + i_{f(r)}} - 1 \quad (4)$$

Using equation (4) in (3) gives the unified current-control model (UICM), expressed in (5), which establishes the relationship between the terminal voltages and the forward (reverse) inversion levels $i_{f(r)}$. As a rule of thumb [3], the transistor operates in weak inversion (WI) up to $i_f = 1$ and in strong inversion (SI) for $i_f > 100$. The intermediate values of i_f , from 1 to 100, characterize moderate inversion (MI).

The pinch-off voltage V_P can be approximated by (6), where V_{T0} is the equilibrium threshold voltage that corresponds to the gate voltage for which $V_P = 0$, σ is the magnitude of the DIBL coefficient. In the 4-parameter model the DIBL effect is modeled to respect the symmetry of the MOSFET.

$$I_{F(R)} = I_S F \left[\frac{V_P - V_{S(D)}}{\phi_t} \right] \quad (5a)$$

$$F^{-1} = \sqrt{1 + i_{f(r)}} - 2 + \ln \left(\sqrt{1 + i_{f(r)}} - 1 \right) \quad (5b)$$

$$V_P = \frac{V_{GB} - V_{T0} + \sigma V_{DB} + \sigma V_{SB}}{n} \quad (6)$$

III. IMPLEMENTING THE ACM MODEL IN CADENCE

Verilog-A is a procedural language to describe analog behavior, and all necessary interactions between the model and the simulator are handled by the Verilog-A compiler. It supports description of devices and circuits using ordinary differential algebraic equations [5].

The UICM in (5) is meant to simplify the design of various MOSFET circuits using the inversion levels; however, for a simulator, the terminal voltages are the input, and the drain current is the output. When solving (5) for the drain current, one ends up with a transcendental equation that can be solved numerically. The simulator, however, solves the equation for each point and cannot waste time and processing power in iterative calculations to find the solution of one single point. Siebel [6] tested some algorithms and ways to implement (5) in simulators and concluded that algorithm 443 [7] is the most accurate to solve (5) in one single iteration.

Algorithm 443 solves the transcendental equations in the form $x = we^w$. To resemble such form, the UCCM in (3) can be easily rewritten as (7).

$$e^{\left(\frac{V_P - V_{S(D)B}}{\phi_t} + 1 \right)} = q_{IS(D)} e^{q_{IS(D)}} \quad (7)$$

By comparing (7) to $x = we^w$, Algorithm 443 can be applied and the normalized forward and reverse charge densities are determined. Afterward, the normalized charge density in (4) is solved for the forward and reverse inversion levels i_f and i_r , which, inserted into (1), determine I_D .

IV. PARAMETER EXTRACTION

The values of the threshold voltage (V_{T0}), specific current (I_S) and slope factor (n) are extracted based on the g_m/I_D method [8] illustrated in Fig. 2. Fig. 2(a) presents the circuit configuration to obtain the g_m/I_D characteristic and Fig. 2(b) presents the values used to determine the parameters. The fourth parameter was extracted from the intrinsic gain of the common-source amplifier [9].

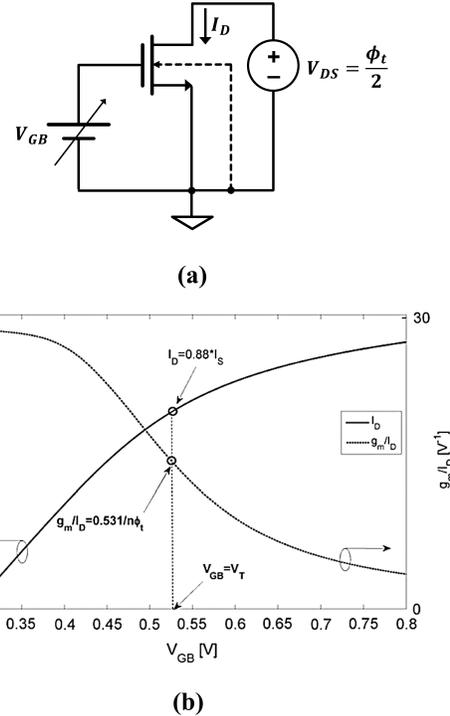


Fig. 2. (a) Circuit to measure the g_m/I_D characteristic in the linear region; (b) measurements of g_m/I_D and I_D as a function of V_{GB} ; the annotated points are used to determine V_{T0} and I_S . Source: [8].

Table I summarizes the extracted values for NMOS and PMOS transistors of $W/L = 0.6 \mu m/0.3 \mu m$ from a $0.18 \mu m$ technology.

V. CIRCUIT EXAMPLES AND SIMULATION RESULTS

Three circuits were simulated using the ACM model Verilog-A description and BSIM 4.5 [10]; the classic CMOS

TABLE I
EXTRACTED PARAMETERS EMPLOYED AS INPUT TO VERILOG-A
DESCRIPTION

Transistor	NMOS	PMOS
$\frac{W}{L}$ [$\frac{\mu m}{\mu m}$]	0.6 0.3	0.6 0.3
I_S [nA]	280	89
V_{T0} [mV]	309	- 269
n	1.19	1.17
σ [mV/V]	15	23

inverter, an 11-stage ring oscillator, and a self-biased current source (SBCS).

A. CMOS inverter

A versatile and yet simple circuit, the CMOS inverter shown in Fig. 3 is used for numerous ULV digital circuits and analog building blocks such as amplifiers and oscillators, just to name a few of their applications.

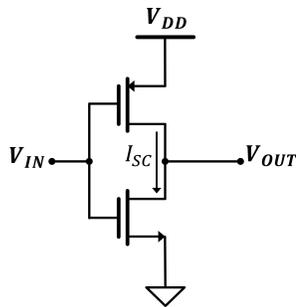


Fig. 3. CMOS inverter. I_{SC} is the short-circuit current.

The CMOS inverter of this work, was designed to have a perfect balance between the NMOS and PMOS transistors for $V_{DD} = 100$ mV. Their aspect ratios are $W_P/L_P = 600$ nm/300 nm, and $W_N/L_N = 600$ nm/300 nm, respectively. The extracted values in Table I were used as input to the Verilog-A description.

The design was validated using the all-region ACM model in Verilog-A and BSIM in the Cadence® simulator. The Voltage Transfer Characteristic (VTC), small-signal gain and short-circuit current results were obtained via DC simulation for five values of supply voltage V_{DD} . Fig. 4 shows that for the V_{DD} range shown, the 4-parameter model appropriately describes the electrical behavior of the CMOS inverter.

B. Ring oscillator

The ring oscillator, illustrated in Fig. 5, consists of N CMOS inverters in a loop. The load capacitance C_L in-between stages are crucial to set the oscillator frequency and critical for a successful start-up. It encompasses external capacitors that

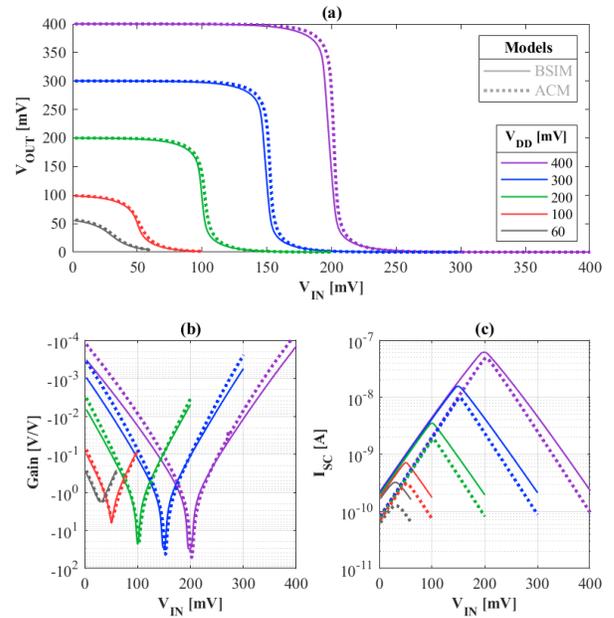


Fig. 4. (a) Voltage transfer characteristic (VTC), (b) small-signal gain and (c) short-circuit current for BSIM and ACM models of CMOS inverter

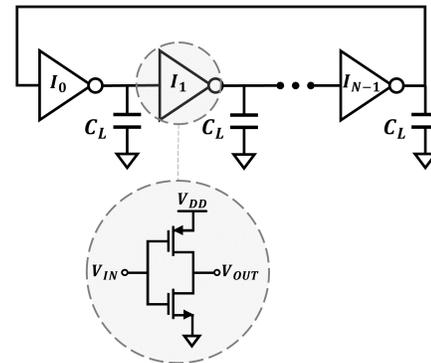


Fig. 5. Ring oscillator

load each node, as well as the intrinsic and extrinsic transistors capacitances [3], [11].

In accordance with the guidelines for ULV ring oscillators discussed in [12], we chose the number of stages $N=11$. Fig. 6 shows a comparison between the simulation results of the ring oscillator at $V_{DD} = 100$ mV using the ACM and BSIM models. Table II demonstrates the accuracy of ACM in relation to BSIM for various V_{DD} .

The frequency of oscillation using the ACM model differed in over 200% from the BSIM result at $V_{DD} = 300$ mV and 400 mV. The implemented dynamic model does not include the extrinsic capacitances related to fringing and diode junctions [11], which contributes to this difference. However, Table II shows that for subthreshold voltages, specially at 100 mV, the implemented dynamic model is enough to describe the

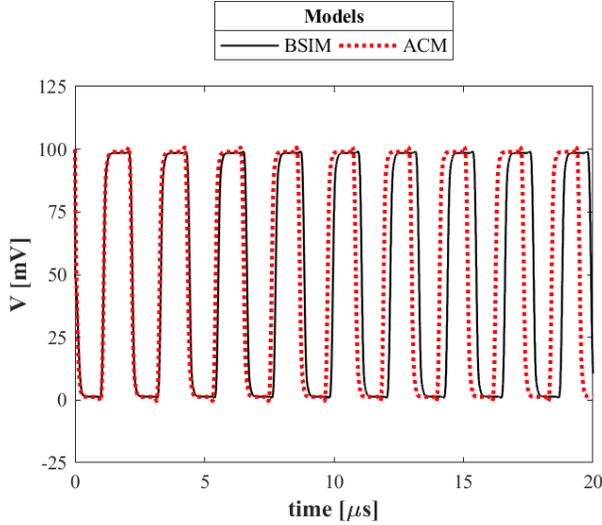


Fig. 6. Result of a transient simulation for Ring oscillator at $V_{DD} = 100$ mV.

TABLE II

FREQUENCY RESULTS OF TIME-DOMAIN SIMULATION OF 11-STAGE RING OSCILLATOR WITHOUT EXTERNAL C_L

V_{DD}	BSIM	ACM	f_{ACM}/f_{BSIM}
400 mV	81.3 MHz	187.2 MHz	2.30
300 mV	23.7 MHz	52.1 MHz	2.20
200 mV	3.79 MHz	5.87 MHz	1.55
100 mV	452 kHz	463 kHz	1.02
60 mV	198 kHz	177 kHz	0.89

electrical behavior of a ring oscillator.

C. Self-biased current source (SBCS)

The design of the SBCS in Fig. 7 follows the steps presented by Camacho in [13]. The target output current is 100 nA at a supply voltage of 1.8 V.

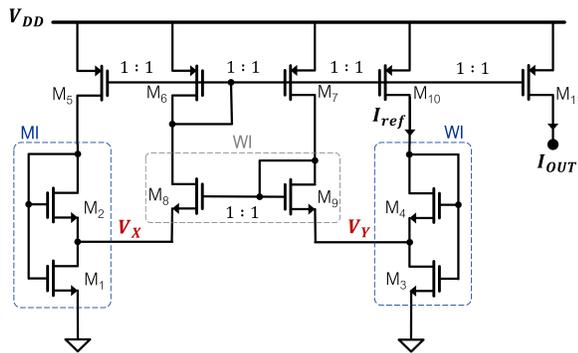


Fig. 7. Self-biased current source (SBCS)

The core of the SBCS in Fig. 6.6 is the self-cascode MOSFET (SCM) composed of transistors M_1 and M_2 , which operate in moderate inversion. The second SCM, formed by M_3 and M_4 , is biased in weak inversion to generate a

proportional to absolute temperature (PTAT) voltage V_Y . Table III summarizes the sizes and inversion levels used in the design.

TABLE III
TRANSISTOR SIZES FOR THE SBCS

Transistor	$\frac{W}{L} \times \frac{N_{parallel}}{N_{series}}$	i_f
$M_{1,2}$	$\frac{0.5 \mu m}{2.0 \mu m} \times \frac{1}{4}$	15
M_3	$\frac{0.5 \mu m}{2.0 \mu m} \times \frac{20}{1}$	0.32
M_4	$\frac{4.0 \mu m}{2.0 \mu m} \times \frac{40}{1}$	0.01
$M_{8,9}$	$\frac{0.5 \mu m}{2.0 \mu m} \times \frac{35}{1}$	0.1
$M_{5-7,10,11}$	$\frac{0.5 \mu m}{2.0 \mu m} \times \frac{1}{1}$	10

Fig. 8 presents the DC simulation results of the SBCS using the BSIM and ACM models for a voltage sweep on V_{DD} from 0 to 1.8 V. Note that the output current and the voltages at nodes V_X and V_Y present similar results for both models. The calculated intermediate voltage at nodes V_X and V_Y was 88 mV, while in simulation, the average intermediate voltages for the start-up range were $V_X \cong 86$ mV and $V_Y \cong 81$ mV. For improved results, the design of the SBCS can be optimized as in [13] and [14], but the goal here is to compare the BSIM model with the ACM model.

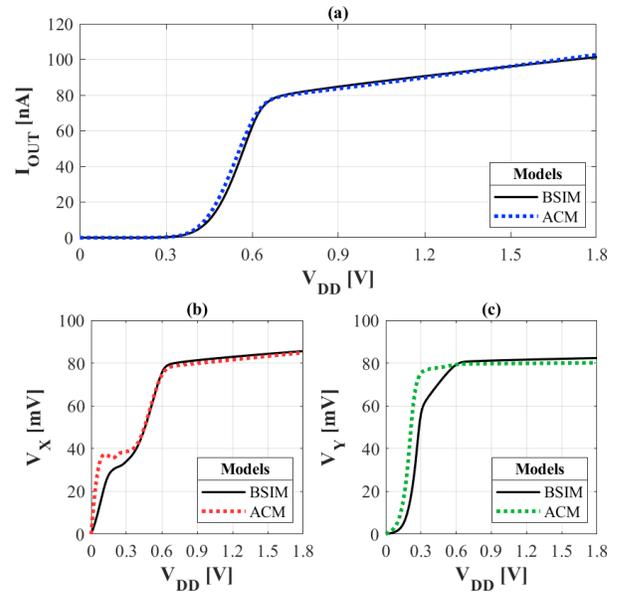


Fig. 8. Results of DC simulation with sweep on the supply voltage V_{DD} : (a) output current, (b) V_X , (c) V_Y

VI. CONCLUSION

This paper introduced a 4-parameter model based on the ACM model, which approaches design through inversion levels. The model can also be used to simulate circuits

within commercial simulators by implementation in Verilog-A. The circuits herein, simulated using the 4-parameter model, presented consistent results with BSIM, especially for ultra-low-voltages. The 4-parameter model is a minimalist model which requires only four parameters to describe DC and small-signal characteristics of a transistor, while BSIM requires over 60 parameters for a DC analysis. The 4-parameter model, therefore, helps to bridge the gap between hands-on design and simulation.

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