Analysis and Design of the Classical CMOS Schmitt Trigger in Subthreshold Operation

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***Abstract*— In this paper, the classical CMOS Schmitt trigger (ST) operating in the subthreshold regime is analyzed. The complete DC voltage transfer characteristic of the CMOS ST is determined. The metastable segment of the characteristic is explained in terms of the negative resistance of the NMOS and PMOS subcircuits of the ST. Small-signal analysis is carried out to determine the minimum supply voltage at which the hysteresis appears and to obtain a rough estimation of the hysteresis width. It is shown that the theoretical minimum supply voltage required to obtain hysteresis is $2\ln(2+\sqrt{5})kT/q = 75$ mV at room temperature. A test chip with CMOS Schmitt triggers was designed and fabricated in a 180 nm technology in order to study their operation at supply voltages between 50 mV and 1000 mV.**

***Index Terms*— CMOS inverter, Schmitt trigger, subthreshold operation, ultra-low power, ultra-low voltage.**

I. Introduction

ULTRA-low-voltage circuits have gained considerable attention in voltage-constrained applications. Small supply voltages generally force the MOS transistors to operate in the subthreshold regime. One of the most useful circuits for both analog and digital applications is the standard CMOS Schmitt trigger (ST) [1]. In contrast to the bipolar and OP-AMP based ST circuits, which have been analyzed in detail in the literature [2]–[5], there are few in-depth studies on the CMOS ST [6]–[7]. Even though some authors [8]–[9] have claimed that the pile-up of four transistors between power and ground rails means that the classical CMOS ST shown in Fig. 1 is not appropriate for low-voltage applications, it has been employed as the key element in several ultra-low-voltage (ULV) circuits [10]–[14]. In [11], ST-based logic gates, designed for the maximization of the on-to-off current ratio, were able to operate from a supply voltage as low as 62 mV. This remarkable result motivated us to carry out an in-depth study of the Schmitt-trigger in the subthreshold regime.

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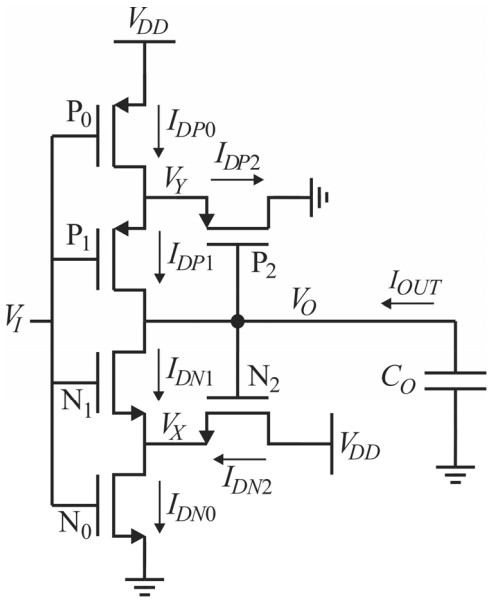

Fig. 1. Classical 6-transistor CMOS Schmitt trigger circuit [1], with the output capacitance, C_O.

In general, the operation of CMOS digital circuits from supply voltages of 500 mV or less forces the transistors to operate in the weak inversion, or subthreshold, regime [15], which is characterized by an exponential relationship between the current and the terminal voltages. Even though the standard CMOS circuits have been extensively analyzed in weak inversion [15]–[17], very little effort has been directed toward modeling the ST in weak inversion. In [10], the trip point of a 10-transistor SRAM cell based on the ST designed to work in weak inversion is determined, while in [11] the on-to-off current ratio of the ST in weak inversion operation is calculated.

This paper explores the subthreshold operation of the ST and provides complete analytical expressions for its design. In Section II, the voltage transfer characteristic of the ST is analyzed and the origin of the hysteresis is explained in terms of the current characteristics of the n- and p-subcircuits, similarly to the work reported in [7]. In Section III, small-signal analysis allows the minimum supply voltage at which hysteresis starts to appear to be determined and an approximation for the hysteresis width is given. Section IV presents the experimental results, while conclusions are drawn in Section V.

II. DC Transfer Characteristics

The MOSFET drain current in weak inversion is given [15], [18] by

$$I_{DN(P)} = I_{N(P)} \cdot e^{\frac{V_{GB(BG)}}{n_{N(P)} \cdot \phi_t}} \cdot \left(e^{-\frac{V_{SB(BS)}}{\phi_t}} - e^{-\frac{V_{DB(BD)}}{\phi_t}} \right) \quad (1)$$

$$I_{N(P)} = \mu_{N(P)} \cdot n_{N(P)} \cdot C'_{ox} \cdot \phi_t^2 \cdot \frac{W}{L} \cdot e^{-\frac{|V_{T0N(P)}|}{n_{N(P)}}+1} \quad (2)$$

where $I_{N(P)}$ is the NMOS(PMOS) transistor strength, or current scaling factor, which is dependent on the aspect ratio $W/L$and the technological parameters $\mu_{N(P)}$ (mobility), C'_{ox} (oxide capacitance per unit area), and $V_{T0N(P)}$ (threshold voltage). $\phi_t = kT/q$ is the thermal voltage and $n_{N(P)}$ is the slope factor. G, S, D and B are the gate, source, drain, and bulk nodes, respectively. For n-channel transistors the nodal voltages referred to the bulk are positive while for p-channel transistors they are negative.

In this study, for the sake of simplicity, we consider that the NMOS and PMOS networks have the same strength. Thus, $I_{N0} = I_{P0} = I_0$, $I_{N1} = I_{P1} = I_1$, and $I_{N2} = I_{P2} = I_2$. Note that I_0, I_1, and I_2 are the main design parameters of the CMOS Schmitt trigger.

Calculating the currents $I_{DN0(P0)}$, $I_{DN1(P1)}$, and $I_{DN2(P2)}$ from (1), the DC equations for nodes V_X and V_Y, for $n_N = n_P = 1$ are

$$e^{\frac{V_X}{\phi_t}} = \frac{I_0 + I_1 + I_2 \cdot e^{\frac{V_O - V_I}{\phi_t}}}{I_0 + I_1 \cdot e^{-\frac{V_O}{\phi_t}} + I_2 \cdot e^{\frac{V_O - V_I}{\phi_t}} \cdot e^{-\frac{V_{DD}}{\phi_t}}} \quad (3)$$

$$e^{\frac{V_Y}{\phi_t}} = \frac{I_0 \cdot e^{\frac{V_{DD}}{\phi_t}} + I_1 \cdot e^{\frac{V_O}{\phi_t}} + I_2 \cdot e^{\frac{V_I - V_O}{\phi_t}}}{I_0 + I_1 + I_2 \cdot e^{\frac{V_I - V_O}{\phi_t}}}. \quad (4)$$

The DC equation for node V_O, with unloaded ST ($I_{OUT} = 0$) is given by

$$e^{\frac{V_I - V_X}{\phi_t}} - e^{\frac{V_I - V_O}{\phi_t}} = e^{\frac{V_Y - V_I}{\phi_t}} - e^{\frac{V_O - V_I}{\phi_t}}. \quad (5)$$

The DC nodal equations of the ST circuit of Fig. 1 are given in Appendix A for general values of n_N and n_P.

Fig. 2 shows the voltage transfer characteristic (VTC) of the ST in Fig. 1, calculated from equations (3)–(5). For $V_{DD} = 150$ mV the VTC presents hysteresis, but for $V_{DD} = 60$ mV it does not.

In order to understand the origin of the hysteresis we follow [7] and split the Schmitt trigger inverter into two parts, the PMOS network (PN), shown in Fig. 3(a), and the NMOS network (NN), shown in Fig. 3(b).

The currents through P_1 and N_1 as functions of both the input and output voltages are obtained from equations (1)–(2), along with (3) and (4). Fig. 4 shows the currents for $V_{DD} = 60$ mV and $I_0 = I_1 = I_2 = 1$ nA. Note that, for a fixed input voltage, the curves of the currents through P_1 and N_1 intersect at a single point, indicated by the open circles for $V_I = 20$ mV, 30 mV and 40 mV. In this example, any value of the input, from 0 to V_{DD}, is mapped into a single value of the output; therefore, hysteresis does not appear. It will be shown later that, for the parameters chosen in this example, the minimum supply voltage at which hysteresis starts to appear is around 84 mV.

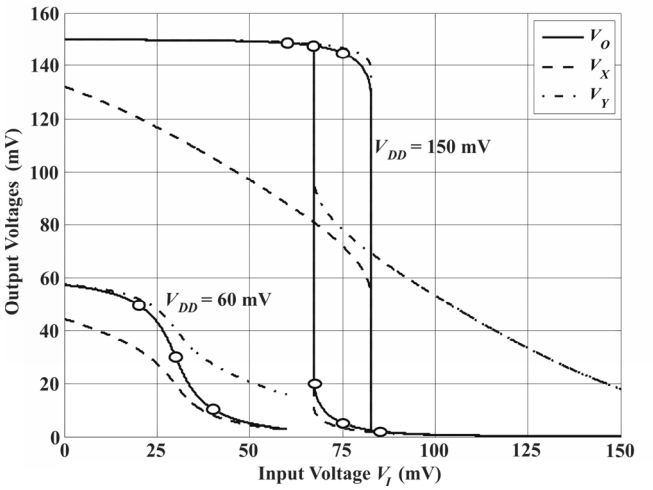

Fig. 2. Output voltages V_O, V_X and V_Y of the Schmitt trigger obtained from analytical expressions (3)–(5) with $I_1/I_0 = I_2/I_0 = 1$ for $V_{DD} = 60$ mV and 150 mV.

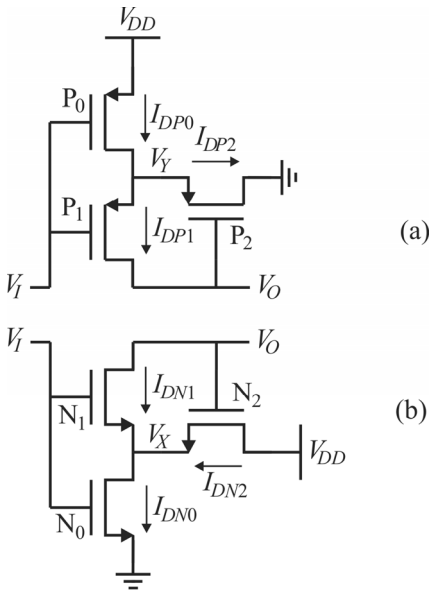

Fig. 3. Schmitt trigger split into the (a) PMOS network (PN) and (b) NMOS network (NN).

It can also be seen in Fig. 4 that, for a fixed input voltage, above a certain output voltage for the NN and below another for the PN, the output resistance becomes negative. However, this phenomenon is not pronounced due to the low value of the supply voltage and has no further consequences.

Fig. 5 shows the drain current of the n- and p-subcircuits for $V_{DD} = 150$ mV. It can be noted that, for a fixed input voltage, the drain current that flows through N_1 initially increases with an increase in the output voltage up to a maximum value. Above this value the current decreases, thus presenting a negative resistance characteristic, which is much more pronounced than in the case where $V_{DD} = 60$ mV. In effect, the feedback transistor N_2 pulls up the node voltage

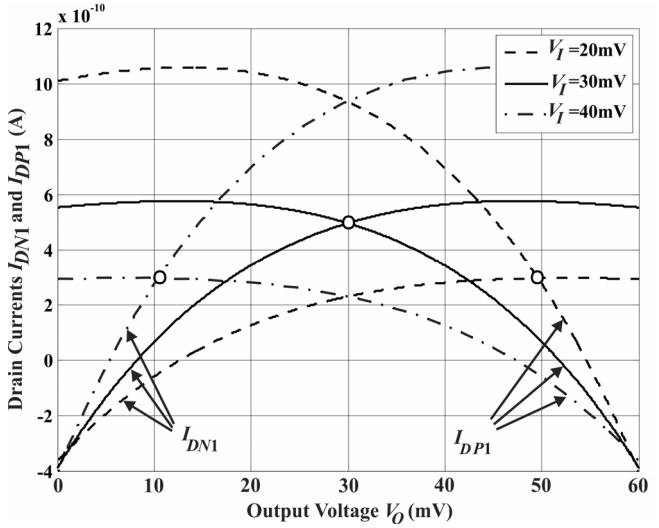

Fig. 4. Drain currents of N_1 and P_1 in terms of the output voltage, V_O, for different input voltages, V_I, with $I_0 = I_1 = I_2 = 1$ nA and $V_{DD} = 60$ mV.

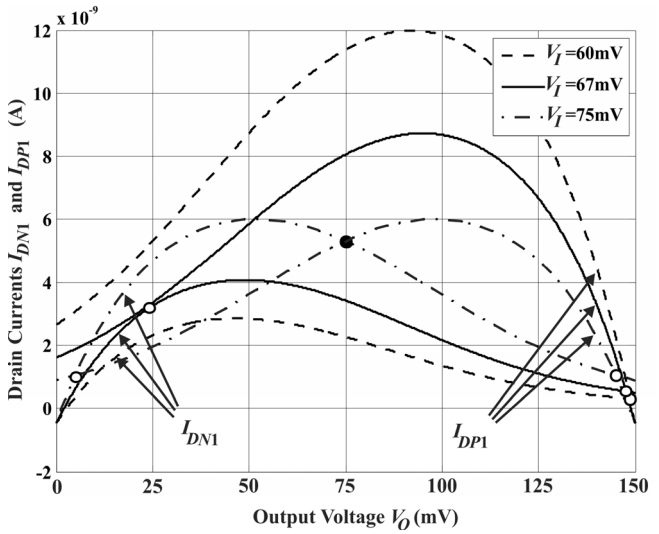

Fig. 5. Drain currents of transistors N_1 and P_1 in terms of the output voltage, V_O, for different input voltages, V_I, with $I_0 = I_2 = I_1 = 1$ nA and $V_{DD} = 150$ mV. Open circles are stable points, while the closed circle is a metastable point.

V_X as the output voltage increases. The increase in V_X causes the current through N_1 to decrease, whereas the increase in V_O tends to increase the current. The effect of the voltage increase in V_X can overwhelm that due to the V_O increase; thus, the output resistance can become negative. The same conclusion applies to the current flowing through P_1. Hysteresis arises as a consequence of the negative resistance of subcircuits PN and NN. In effect, for a fixed input voltage, the output characteristics of NN and PN intersect at either one or three points. In the latter case, the innermost point is metastable, i.e., any disturbance will move it either to the rightmost or to the leftmost points.

Let us now explain graphically the origin of the hysteresis. Initially, consider a negative-going input voltage. When the input voltage is high, e.g., $V_I = 85$ mV, there is only one

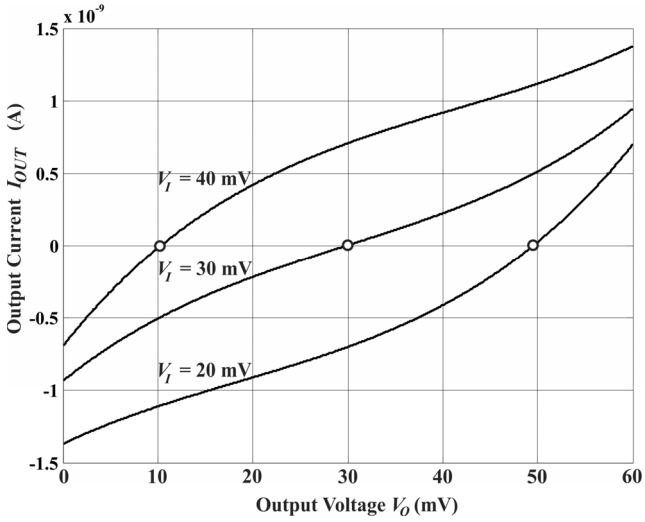

Fig. 6. Output current, I_{OUT}, as a function of the output voltage, V_O, for $V_I = 20$ mV, 30 mV, and 40 mV, with $I_0 = I_1 = I_2 = 1$ nA, $n = 1$, and $V_{DD} = 60$ mV.

stable point, for which V_O is close to ground (see Fig. 2). When the input voltage is lower and lies between the hysteresis limits, e.g., $V_I = 75$ mV, two stable outputs (close to ground and close to V_{DD}) and one metastable output point (at $V_O = 75$ mV) exist, as shown in Fig. 5. However, note that there is no physical stimulus to move the output to the high voltage stable point, and the output remains at the stable point close to ground. As the input voltage continues to decrease, the stable output and the metastable output points approximate and eventually become coincident at the hysteresis limit (see the two tangent curves in Fig. 5 for $V_I = 67$ mV). When the input voltage is below the hysteresis lower limit, e.g., $V_I = 60$ mV, only one operating point exists, which is close to V_{DD}. The transition of the output from the stable point close to ground to that close to V_{DD} is abrupt and is a dynamic phenomenon [5], since the output capacitor, C_O, must be charged or discharged as shown in Appendix B. The same conclusions can be drawn for a positive-going input voltage.

Fig. 6 shows the output current, $I_{OUT} = I_{DN1} - I_{DP1}$, which charges and discharges the output capacitor, C_O, as a function of the output voltage, V_O. In this example, $V_{DD} = 60$ mV and the input voltage takes the values 20 mV, 30 mV, and 40 mV. It can be observed that the output current varies monotonically with the output voltage. For each input voltage there is only one stable output voltage (at $I_{OUT} = 0$ A).

If the supply voltage is raised to 150 mV, as shown in Fig. 7, the output driving point characteristic presents a negative resistance region. In this figure, when the input voltage is 60 mV only one stable point exists, which is close to V_{DD}. As the input voltage is raised to 67 mV the curve for the output current is shifted upwards and reaches zero at two points. The leftmost point indicates the appearance of both a second stable point and a metastable point. At an input voltage of 75 mV, three different zeroes exist, one of which is metastable.

The metastable points of the output characteristics constitute the inner arc of the "Z"-shaped transfer curve shown in Fig. 8.

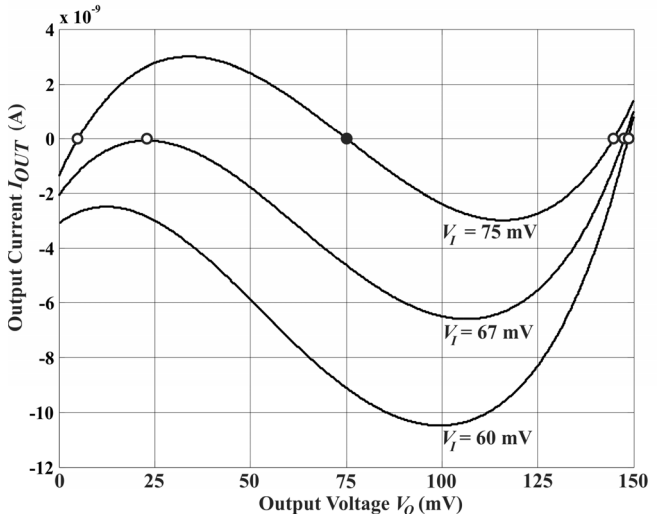

Fig. 7. Output current, I_{OUT}, as a function of the output voltage, V_O, for $V_I = 60$ mV, 67 mV, and 75 mV, with $I_0 = I_1 = I_2 = 1$ nA, $n = 1$, and $V_{DD} = 150$ mV. Open circles are stable points while the closed circle is a metastable point.

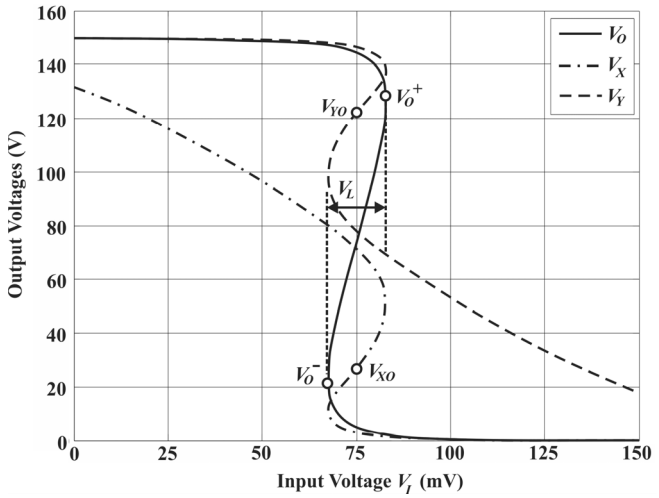

Fig. 8. "Z" curve formed by the metastable points for $V_{DD} = 150$ mV, $n = 1$, $I_1/I_0 = I_2/I_0 = 1$.

Thus, as for the bipolar and OP-AMP-based ST circuits [5], the DC voltage transfer characteristic of the classical CMOS ST is an unstable arc within the hysteresis region.

Since the ST circuit under analysis is symmetrical, it is interesting to note that, for any supply voltage, $V_I = V_O = V_{DD}/2$ is either a stable (for a non-hysteretic curve) or a metastable (for a hysteretic curve) operating point.

III. Small-Signal Analysis

The AC gain of the Schmitt trigger is derived by substituting each MOSFET with its equivalent small-signal model of three voltage-controlled current sources [18], as shown in Fig. 9, where g_m, g_{md}, and g_{ms} are the gate, drain and source transconductances, respectively.

The low-frequency small-signal circuit of an ST with matched n- and p-subcircuits for $V_I = V_O = V_{DD}/2$ is shown in Fig. 10, where v_I, v_O, v_X, and v_Y are small-signal voltages.

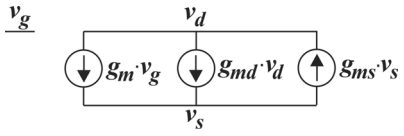

Fig. 9. Small-signal MOSFET model ($v_b = 0$).

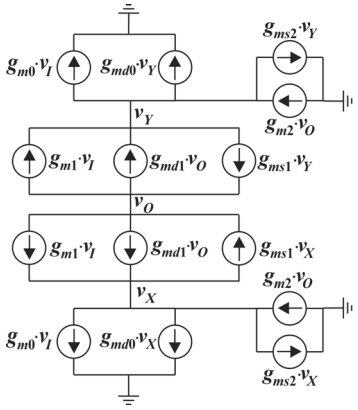

Fig. 10. Small-signal model of the Schmitt trigger with matched n- and p-subcircuits for $V_I = V_O = V_{DD}/2$.

TABLE I
Transconductances of the Schmitt Trigger for $V_O = V_I = V_{DD}/2$

	g_{ms}	g_{md}	g_m
N_0 or P_0		$\frac{I_0}{\phi_t} \cdot e^{\frac{V_{DD}-2V_{X0}}{2\phi_t}}$	$\frac{I_0}{\phi_t} \cdot e^{\frac{V_{DD}}{2\phi_t}} \cdot \left(1 - e^{-\frac{V_{X0}}{\phi_t}}\right)$
N_1 or P_1	$\frac{I_1}{\phi_t} \cdot e^{\frac{V_{DD}-2V_{X0}}{2\phi_t}}$	$\frac{I_1}{\phi_t}$	$\frac{I_1}{\phi_t} \cdot \left(e^{\frac{V_{DD}-2V_{X0}}{2\phi_t}} - 1\right)$
N_2 or P_2	$\frac{I_2}{\phi_t} \cdot e^{\frac{V_{DD}-2V_{X0}}{2\phi_t}}$		$\frac{I_2}{\phi_t} \cdot e^{-\frac{V_{DD}}{2\phi_t}} \cdot \left(e^{\frac{V_{DD}-V_{X0}}{\phi_t}} - 1\right)$

Applying KCL to v_X, v_Y, and v_O and solving for v_O/v_I results in $v_X = v_Y$, as expected, and

$$\left.\frac{v_O}{v_I}\right|_{V_O=V_I=\frac{V_{DD}}{2}} = -\frac{g_{m1}}{g_{md1}} \cdot \frac{1 + \frac{g_{ms1} \cdot g_{m0}}{g_{m1} \cdot (g_{ms2} + g_{md0})}}{1 - \frac{g_{ms1} \cdot g_{m2}}{g_{md1} \cdot (g_{ms2} + g_{md0})}}. \quad (6)$$

The small-signal gain given by (6) is the actual negative gain of the ST when no hysteresis is present and the positive gain of the metastable curve when the VTC presents hysteresis. We will use the positive gain for the estimation of the hysteresis width in Section III-B.

The transconductances [18] are given in Table I for $V_I = V_O = V_{DD}/2$.

From (3), $V_{X0} = V_X$ ($V_I = V_O = V_{DD}/2$) is given by

$$e^{\frac{V_{X0}}{\phi_t}} = \frac{I_0 + I_1 + I_2}{I_0 + I_1 \cdot e^{-\frac{V_{DD}}{2\phi_t}} + I_2 \cdot e^{-\frac{V_{DD}}{\phi_t}}}. \quad (7)$$

By substituting the values for the transconductances in Table I into (6), the small-signal voltage gain in terms of the transistor current strengths and the supply voltage are obtained, as shown in Appendix A.

A. Calculation of the Minimum Supply Voltage V_{DDH} Required for the Appearance of Hysteresis

A zero in the denominator of (6) results in an infinite gain, which is associated with the transition between the amplifier and the hysteretic operation modes.

Using Table I to calculate the transconductances of the denominator of (6) we obtain the condition for infinite gain as

$$\frac{e^{\frac{V_{DDH}}{2\phi_t}} \cdot \left(e^{-\frac{V_{X0}}{\phi_t}} - e^{-\frac{V_{DDH}}{\phi_t}}\right)}{1+\frac{I_0}{I_2}} = 1 \tag{8}$$

where V_{DDH} is the minimum supply voltage for hysteresis. Substituting the value of V_{X0} from (7) into (8), and neglecting e^{-V_{DD}/ϕ_t} compared to $e^{-V_{DD}/2\phi_t}$, we obtain the supply voltage limit V_{DDH} for the appearance of hysteresis as

$$V_{DDH} \approx 2\phi_t \cdot \ln\left(2+\frac{I_2}{I_0}+\frac{I_0}{I_2}+\frac{I_1}{I_2}\right). \tag{9}$$

Using (A5) to obtain the exact value of the lower bound of V_{DDH} with $n = 1$, which is reached for $I_2/I_0 = 1$ and $I_1/I_2 = 0$, results in

$$V_{DDH\min} = 2\phi_t \cdot \ln\left(2+\sqrt{5}\right) = 75\text{mV at 300 K}. \tag{10}$$

It is interesting to note that the value for V_{DDHmin} is approximately twice the well-known lower bound of the supply voltage of the CMOS inverter [19] at which the voltage gain is higher than unity.

B. Schmitt Trigger With Hysteresis ($V_{DD} > V_{DDH}$)

The sets of metastable points of the VTC, calculated from (3) – (5), form the "Z" curves plotted in Fig. 11 for V_{DD} in the range 200 mV to 400 mV. In Fig. 11(a)–(c) the feedback is low ($I_2/I_0 = 0.1$-0.5) and in Fig. 11(d)–(f) the feedback is high ($I_2/I_0 = 1$-5). It can be observed that the metastable arc is roughly linear for high feedback. For high feedback we approximated the hysteresis width V_L as follows (see Fig. 8):

$$V_L \approx \frac{V_O^+ - V_O^-}{\left.\frac{dV_O}{dV_I}\right|_{V_O=V_I=\frac{V_{DD}}{2}}} \approx \frac{V_{DD}-2V_{X0}}{\left.\frac{dV_O}{dV_I}\right|_{V_O=V_I=\frac{V_{DD}}{2}}} \tag{11}$$

where V_o^+ and V_o^- are the output voltages at the limits of the metastable arc (see Fig. 8).

Using the result for the slope of the VTC calculated in Appendix C, it follows that

$$V_L \approx \frac{(V_{DD}-2V_{X0}) \cdot \left(1-e^{\frac{V_{DDH}-V_{DD}}{2\phi_t}}\right)}{2+\frac{I_0}{I_2}+\frac{I_1}{I_2}}. \tag{12}$$

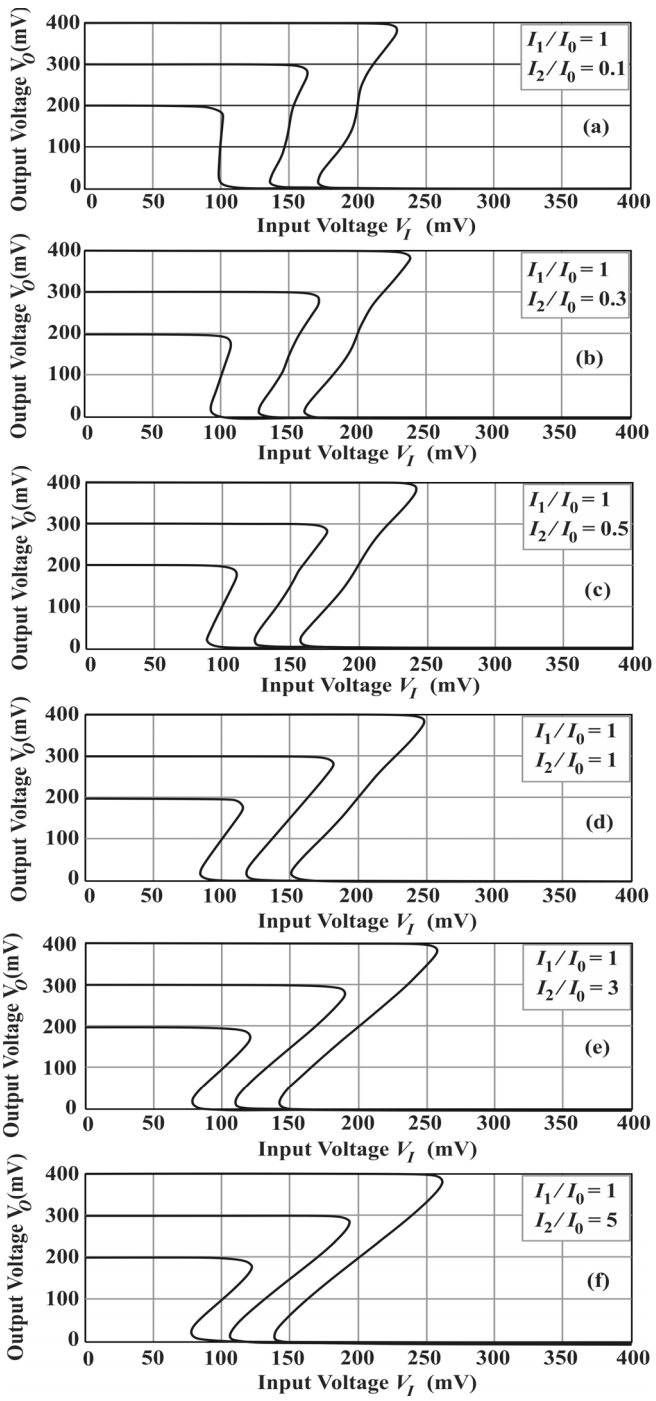

Fig. 11. VTC for V_{DD} = 200 mV, 300 mV, and 400 mV, $I_1/I_0 = 1$. Low feedback: (a) $I_2/I_0 = 0.1$; (b) $I_2/I_0 = 0.3$; (c) $I_2/I_0 = 0.5$. High feedback: (d) $I_2/I_0 = 1$; (e) $I_2/I_0 = 3$; (f) $I_2/I_0 = 5$.

IV. Experimental Results

In order to validate the theoretical study of the Schmitt trigger, a test chip was designed and fabricated in a 180 nm technology ($V_{TN0} = 397$ mV, $V_{TP0} = -394$ mV, $n_N = 1.32$, $n_P = 1.24$, for $L_N = 1.08$ μm, $L_P = 1.08$ μm). Two sets of Schmitt triggers were designed with different transistor sizes in order to evaluate the effect of the relative transistor strength on the hysteresis width. The length of the transistors was

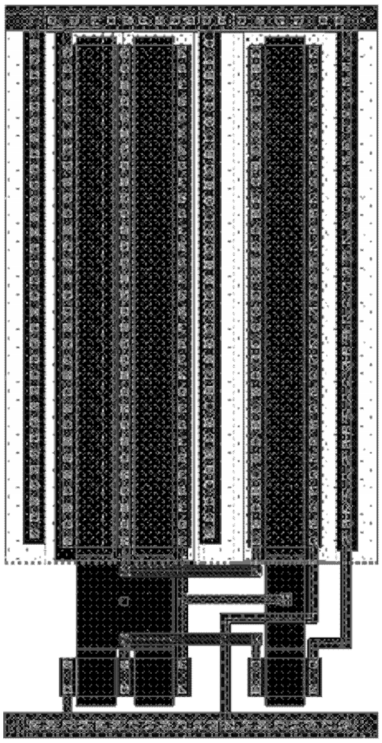

Fig. 12. Layout of the 180 nm Schmitt trigger with $I_1/I_0 = 1$ and $I_2/I_0 = 1$, where $(W/L)_{P0} = (W/L)_{P1} = (W/L)_{P2} = 14\mu m/1.08\mu m$, $(W/L)_{N0} = (W/L)_{N1} = (W/L)_{N2} = 1.08\mu m/1.08\mu m$.

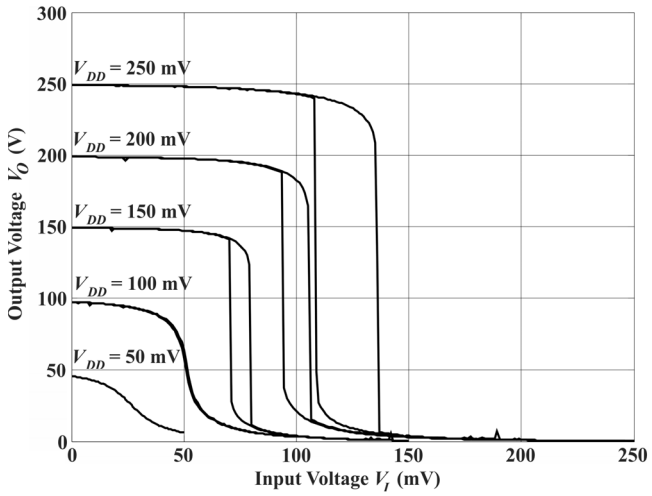

Fig. 13. Measured VTCs of the ST for V_{DD} between 50 mV and 250 mV.

fixed at 6 times the minimum transistor length allowed by the technology ($L_{MIN} = 180$ nm), in order to reduce both the threshold voltage spread and the short-channel effects. The transistor length and width were determined by simulation for the typical (TT) corner parameters for $V_{DD} = 150$ mV, in order to have the resulting VTC centered at $V_{DD}/2$. Two sets of Schmitt triggers with $I_1/I_0 = 0.4$ and $I_1/I_0 = 1$ and feedback ratios, I_2/I_0, of 0.1, 0.3, 1, and 3 were designed.

The Schmitt trigger with $I_1/I_0 = 1$ and $I_2/I_0 = 1$ (where $(W/L)_{P0} = (W/L)_{P1} = (W/L)_{P2} = 14\mu m/1.08\mu m$ and $(W/L)_{N0} = (W/L)_{N1} = (W/L)_{N2} = 1.08\mu m/1.08\mu m$)

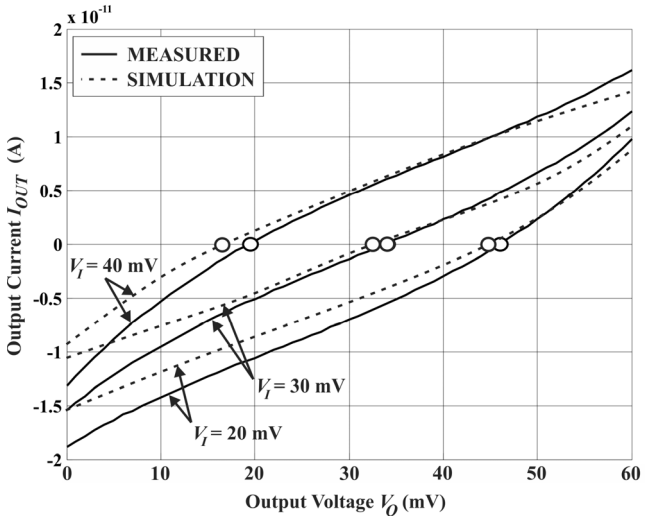

Fig. 14. Output current, I_{OUT}, as a function of the output voltage, V_O, for $V_I = 20$ mV, 30 mV, and 40 mV, with $V_{DD} = 60$ mV. Open circles are associated with $I_{OUT} = 0$.

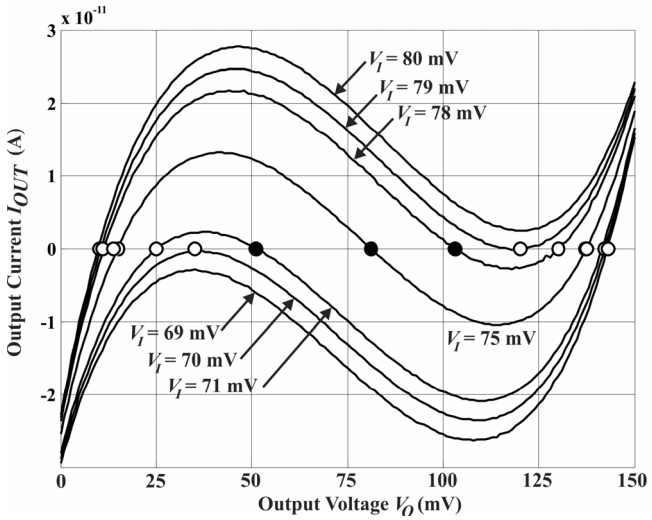

Fig. 15. Measured output current, I_{OUT}, as a function of the output voltage, V_O, for $V_I = 69$ mV, 70 mV, 71 mV, 75 mV, 78 mV, 79 mV, and 80 mV, for $V_{DD} = 150$ mV. Open circles are stable points while the closed circles are metastable points.

was first used for the measurement of the VTC and output currents. The standard cell layout of the designed Schmitt trigger is shown in Fig. 12, and it occupies an area of 10.41 μm $\times$ 20.37 μm.

The VTCs of the ST for supply voltages of 50 mV, 100 mV, 150 mV, 200 mV, and 250 mV are shown in Fig. 13. For supply voltages below 100 mV hysteresis is not present, which is in well agreement with (A6), with $n = 1.3$ extracted from the simulation.

The output current, I_{OUT}, of the ST in Fig. 12, measured for $V_{DD} = 60$ mV, can be seen in Fig. 14. In this example, for fixed input voltages of 20 mV, 30 mV, and 40 mV, there is only one stable state; consequently, no hysteresis is present. Note from the simulation that the zero-crossing values (17 mV, 33 mV, and 45 mV) are very close to those measured in the fabricated chip (19 mV, 34 mV, and 46 mV).

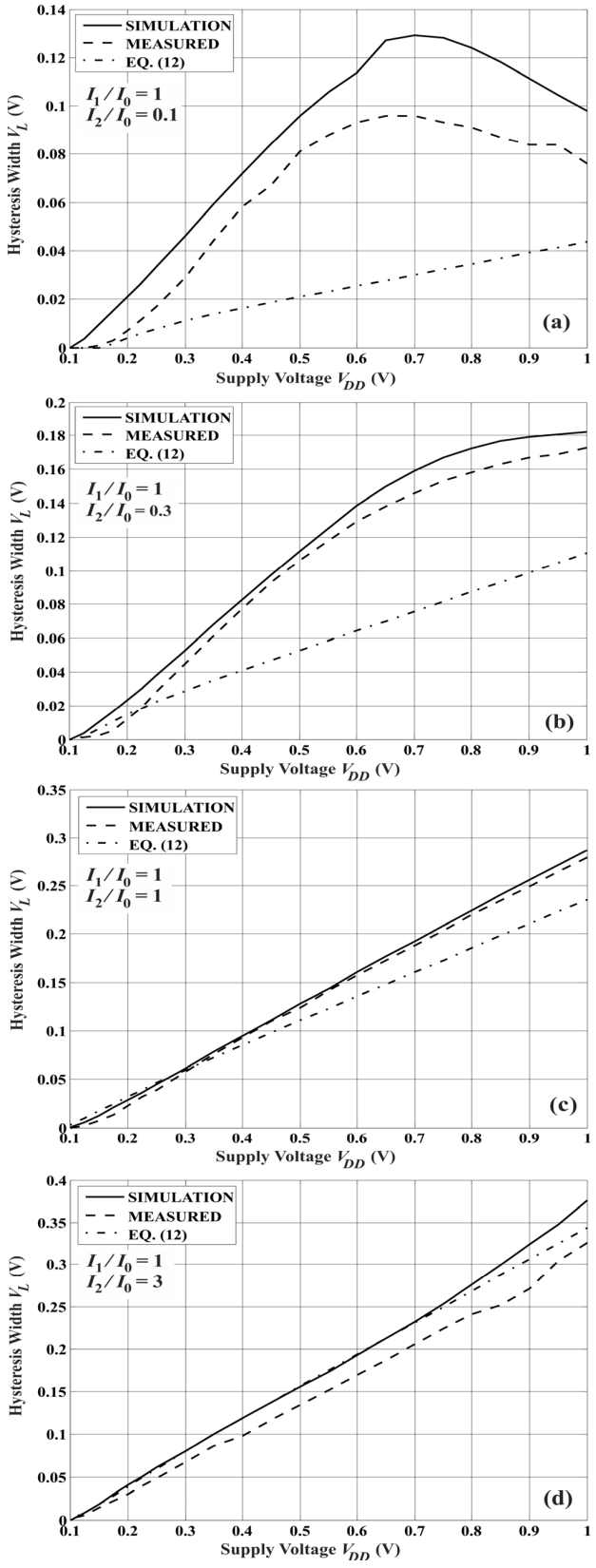

Fig. 16. Comparison of values for the hysteresis width obtained from measurements, simulations and (12) with $I_1/I_0 = 1$ and (a) $I_2/I_0 = 0.1$; (b) $I_2/I_0 = 0.3$; (c) $I_2/I_0 = 1$; and (d) $I_2/I_0 = 3$.

The measured output current for $V_{DD} = 150$ mV can be seen in Fig. 15. When the input voltage is 71 mV, the output current is zero for three values of the output voltage. Two of these points are stable, whereas the third is metastable. When the input voltage is lowered to 70 mV the metastable point coincides with the leftmost stable point, which indicates that the low limit of the hysteresis has been reached. For an input voltage $V_I = 69$ mV, only one stable point exists, clearly showing that this input voltage is not within the hysteresis limits. Analogous conclusions can be drawn when $V_I = 78$ mV, 79 mV, and 80 mV; in this case, note that $V_I = 78$ mV is the high limit of the hysteresis curve. When $V_I = 75$ mV, the metastable point is not exactly at $V_O = 75$ mV, showing that the p- and n- networks are not perfectly matched.

Note that the experimental curves in Figs. 14 and 15 are in close agreement with the theoretical curves of Figs. 6 and 7, respectively.

The hysteresis width was measured for the two sets of Schmitt triggers that were integrated and compared with circuit simulations (Cadence Virtuoso, IBM 180 nm design kit) and equation (12). The results in Fig. 16, for $I_1/I_0 = 1$, show that the hysteresis width varies almost linearly with the supply voltage, for supply voltages higher than around 100 mV. For the cases studied herein, (12) shows acceptable results for feedback ratios I_2/I_0 higher than 0.5. For feedback ratios lower than 0.5, the hysteresis width predicted by (12) is lower than the measured or simulated value due to the nonlinearity of the metastable arc in the vicinity of the midpoint. For the cases in Fig. 16(c)–(d) where $I_2/I_0 = 1$ and $I_2/I_0 = 3$, respectively, the small difference between the values obtained through the simulations, measurements and (12) can be readily explained by variations in the technological parameters and mismatch (mainly associated with the threshold voltage and the width and length of the transistors, which leads to differences in the current strength of the p- and n- networks). Note that in (12) the ST is considered to be composed of well-matched PMOS and NMOS circuits. However, the transistor current is exponentially dependent on both the slope factor and the threshold voltage; therefore, these two factors affect the value of the hysteresis width. The maximum differences in the values for the hysteresis width obtained through measurements and (12) were 43 mV (–15.5% at 1 V) for the case $I_2/I_0 = 1$ and 36.4 mV (14.5% at 850 mV) for the case $I_2/I_0 = 3$. The results for the set in which $I_1/I_0 = 0.4$ are very similar to those for $I_1/I_0 = 1$, showing a difference of only a few millivolts between simulated and measured values. Therefore, the results for $I_1/I_0 = 0.4$ will not be shown here.

Finally, it should be noted that, for supply voltages higher than 500 mV, the analysis of the ST must use the transistor model in either moderate or strong inversion.

V. Conclusions

Analytical expressions were derived for the operation of the classical CMOS Schmitt trigger in weak inversion. The hysteresis width was estimated analytically and a simple expression for the minimum supply voltage needed for the appearance of hysteresis in terms of the current strength of the transistors was given. In particular, it was shown that the theoretical lower bound of the supply voltage for hysteresis is $2\ln(2+\sqrt{5})kT/q = 75$ mV at room temperature.

APPENDIX A
DC AND SMALL-SIGNAL ANALYSIS OF THE CMOS ST

The nodal equations of the ST in the general case $n_n \neq n_p \neq 1$ are obtained from $I_{DN0} = I_{DN1} + I_{DN2}$, $I_{DP0} = I_{DP1} + I_{DP2}$ and $I_{DN1} = I_{DP1}$, and results in

$$e^{\frac{V_X}{\phi_t}} = \frac{I_{N0} + I_{N1} + I_{N2} \cdot e^{\frac{V_O - V_I}{n_N \cdot \phi_t}}}{I_{N0} + I_{N1} \cdot e^{-\frac{V_O}{\phi_t}} + I_{N2} \cdot e^{\frac{V_O - V_I}{n_N \cdot \phi_t}} \cdot e^{-\frac{V_{DD}}{\phi_t}}} \quad \text{(A1)}$$

$$e^{\frac{V_Y}{\phi_t}} = \frac{I_{P0} \cdot e^{\frac{V_{DD}}{\phi_t}} + I_{P1} \cdot e^{\frac{V_O}{\phi_t}} + I_{P2} \cdot e^{\frac{V_I - V_O}{n_P \cdot \phi_t}}}{I_{P0} + I_{P1} + I_{P2} \cdot e^{\frac{V_I - V_O}{n_P \cdot \phi_t}}} \quad \text{(A2)}$$

$$e^{\frac{V_I - n_N \cdot V_X}{n_N \cdot \phi_t}} - e^{\frac{V_I - n_N \cdot V_O}{n_N \cdot \phi_t}} = \frac{I_{P1}}{I_{N1}} \cdot e^{\frac{V_{DD} \cdot (1 - n_P)}{n_P \cdot \phi_t}} \cdot \left(e^{\frac{-V_I + n_P \cdot V_Y}{n_P \cdot \phi_t}} - e^{\frac{-V_I + n_P \cdot V_O}{n_P \cdot \phi_t}} \right). \quad \text{(A3)}$$

The small signal voltage gain for $n_n = n_p = n$ is (A4), as shown at the bottom of this page.

A zero in the denominator of (A4) results in an infinite gain, which indicates the transition from the inverting amplifier mode to the hysteresis mode, as explained in Section II. In order to determine the supply voltage required to sustain the hysteresis, the denominator of equation (A4) is made equal to 0. After some lengthy algebra, we have

$$e^{\frac{V_{DDH}}{2\phi_t}} = \frac{n \cdot \left(1 + \frac{I_2}{I_0}\right) \cdot \left(1 + \frac{I_1}{I_0} + \frac{I_2}{I_0}\right) - \frac{I_1}{I_0} \cdot \frac{I_2}{I_0}}{2\frac{I_2}{I_0}} + \sqrt{\left[\frac{n \cdot \left(1 + \frac{I_2}{I_0}\right) \cdot \left(1 + \frac{I_1}{I_0} + \frac{I_2}{I_0}\right) - \frac{I_1}{I_0} \cdot \frac{I_2}{I_0}}{2\frac{I_2}{I_0}}\right]^2 + \left(1 + \frac{I_1}{I_0}\right)} \quad \text{(A5)}$$

which can be approximated as

$$V_{DDH} \approx 2\phi_t \cdot \ln\left[n \cdot \left(1 + \frac{I_0}{I_2}\right) \cdot \left(1 + \frac{I_1}{I_0} + \frac{I_2}{I_0}\right) - \frac{I_1}{I_0}\right]. \quad \text{(A6)}$$

APPENDIX B
DYNAMIC BEHAVIOR OF THE CMOS ST

The sharp transition shown in the VTC of the ST with hysteresis is inherently a dynamic phenomenon [5]. As soon as the input voltage crosses the hysteresis limit the output current starts to flow and charges the output node, just to the value of V_O at which the output current becomes zero again.

To illustrate the dynamics of the ST with $I_1/I_0 = 1$ and $I_2/I_0 = 1$, having as the load an identical ST, Fig. 17 shows the simulated transient response to an input step voltage.

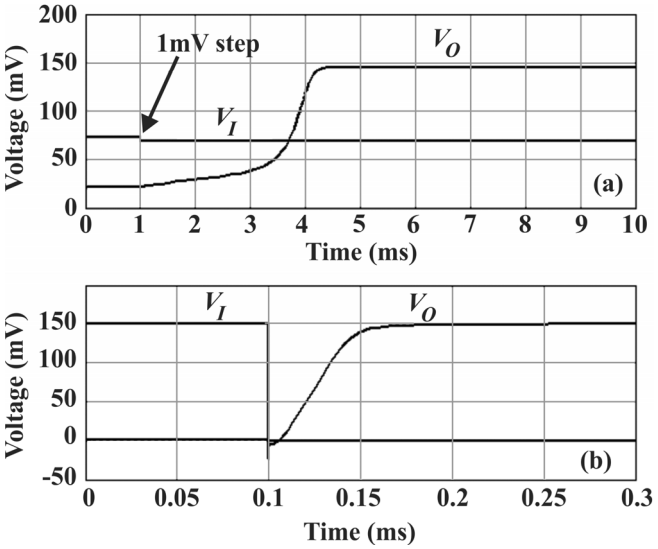

Fig. 17. Transient time for $V_{DD} = 150$ mV, with $I_1/I_0 = 1$ and $I_2/I_1 = 1$ for: (a) 1 mV input step; (b) 150 mV input step.

For $V_{DD} = 150$ mV, the hysteresis low and high limits are 69.5 mV and 82.3 mV, respectively, and these are very close to the measured limits of 70 mV and 79 mV, respectively, as shown in Fig. 15. The step input in Fig. 17(a) changes from 70 mV to 69 mV while the output node is initially charged to 20 mV. A step of –1 mV is sufficient to force a transition in the output voltage from 20 mV to approximately V_{DD}. Initially, the current that charges the output capacitor is low, since the drive input voltage is only 69 mV and very close to one of the metastable points. However, it increases to an absolute maximum value of $I_{OUT} = -35$ pA (absolute maximum measured $I_{OUT} = -26$ pA as shown in Fig. 15 for $V_I = 69$ mV). The resulting rise time is approximately 3 ms. The same analysis can be carried out for a falling transition of the output with input voltages from 81.8 mV to 82.8 mV.

When the step changes from 150 mV to 0 mV, the drive current is high and the rise time lowers to approximately 400 μs, as can be noted in Fig. 17(b).

For a step input between GND and V_{DD}, the rise (T_{LH}) and fall times (T_{HL}) of the output voltage, between 10% and 90% of V_{DD}, can be numerically solved from

$$-I_{OUT} = C_O \cdot \frac{dV_O}{dt}. \quad \text{(B1)}$$

For a positive-going input step, where the input is V_{DD}, the current of P_1 MOSFET is negligible, and $I_{OUT} = I_{DN1}$. For a negative-going input step, where the input is GND, the current of the N_1 MOSFET is negligible, and $I_{OUT} = -I_{DP1}$.

$$\left.\frac{v_O}{v_I}\right|_{V_O = V_I = \frac{V_{DD}}{2}} = \frac{\left(e^{\frac{V_{DD}}{2\phi_t}} - 1\right) \cdot \left(1 + \frac{I_1}{I_0} + 2\frac{I_2}{I_0}\right) + \left(\frac{I_2}{I_0}\right)^2 \cdot \left(e^{-\frac{V_{DD}}{2\phi_t}} - 1\right)}{\frac{I_2}{I_0}\left(e^{\frac{V_{DD}}{2\phi_t}} - e^{-\frac{V_{DD}}{2\phi_t}}\right) + \frac{I_1}{I_0} \cdot \frac{I_2}{I_0}\left(1 - e^{-\frac{V_{DD}}{2\phi_t}}\right) - n\left(1 + \frac{I_2}{I_0}\right) \cdot \left(1 + \frac{I_1}{I_0} + \frac{I_2}{I_0}\right)} \quad \text{(A4)}$$

APPENDIX C
ESTIMATION OF THE HYSTERESIS WIDTH OF THE CMOS ST IN WEAK INVERSION

Substituting the transconductances given in Table I with $n = 1$ in (6) we obtain

$$\left.\frac{dV_O}{dV_I}\right|_{V_O=V_I=\frac{V_{DD}}{2}} = \frac{I_0 \cdot \left(1 - e^{-\frac{V_{DD}}{2\phi_t}}\right) + I_2 \cdot \left(e^{-\frac{V_{X0}}{\phi_t}} - e^{-\frac{V_{DD}}{2\phi_t}}\right)}{I_2 \cdot \left(e^{-\frac{V_{X0}}{\phi_t}} - e^{-\frac{V_{DD}}{2\phi_t}} - e^{-\frac{V_{DD}}{\phi_t}}\right) - I_0 \cdot e^{-\frac{V_{DD}}{2\phi_t}}}. \tag{C1}$$

By substituting the value of $e^{-\frac{V_{X0}}{\phi_t}}$ calculated from (7) into (C1), after some lengthy algebra we obtain

$$\left.\frac{dV_O}{dV_I}\right|_{V_O=V_I=\frac{V_{DD}}{2}} = \frac{\left(2 + \frac{I_0}{I_2} + \frac{I_1}{I_2} - \frac{I_2}{I_0} \cdot e^{-\frac{V_{DD}}{2\phi_t}}\right) \cdot \left(1 - e^{-\frac{V_{DD}}{2\phi_t}}\right)}{1 - \left(2 + \frac{I_0}{I_2} + \frac{I_1}{I_2} + \frac{I_2}{I_0}\right) \cdot e^{-\frac{V_{DD}}{2\phi_t}} - \left(1 + \frac{I_1}{I_0}\right) \cdot e^{-\frac{V_{DD}}{\phi_t}}}. \tag{C2}$$

Using (9), we can rewrite (C2) as

$$\left.\frac{dV_O}{dV_I}\right|_{V_O=V_I=\frac{V_{DD}}{2}} \approx \frac{\left(2 + \frac{I_0}{I_2} + \frac{I_1}{I_2} - \frac{I_2}{I_0} \cdot e^{-\frac{V_{DD}}{2\phi_t}}\right) \cdot \left(1 - e^{-\frac{V_{DD}}{2\phi_t}}\right)}{1 - e^{\frac{V_{DDH} - V_{DD}}{2\phi_t}}}. \tag{C3}$$

Thus from (11) and (C3), neglecting the terms in $e^{-V_{DD}/2\phi_t}$ in the numerator, we obtain

$$V_L \approx \frac{(V_{DD} - 2V_{X0}) \cdot \left(1 - e^{\frac{V_{DDH} - V_{DD}}{2\phi_t}}\right)}{2 + \frac{I_0}{I_2} + \frac{I_1}{I_2}}. \tag{C4}$$

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