A g_m/I_D Design Methodology for 28 nm FD-SOI CMOS Resistive Feedback LNAs

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***Abstract*—This paper presents a simple and efficient methodology for Resistive Feedback LNAs (RF-LNAs) design which uses the inversion level of the transistor as a design parameter in order to optimize the energy efficiency. The method uses a simple 4 parameter-based model valid in all regions of operation and allows a preliminary sizing based on an analytical study. A practical design in a 28 nm FD-SOI technology shows that this methodology is well suited for design at low to moderate inversion level in an advanced technology for which simulation-based studies are often used by designer as early sizing stage. The designed LNA consumes 0.57 mW and achieves an 18.4 dB gain with 3.3 dB of NF.**

Keywords—LNA; resistive feedback; low power; inversion coefficient; 28 nm FD-SOI

I. INTRODUCTION

The use of region based analytical models to achieve a first sizing of a topology is less and less accurate especially in a low power context and in advanced technologies where weak or moderate inversion gives the best compromise at RF frequencies [1]. This leads to an extensive use of simulations with numerous iterations to obtain the desired requirements.

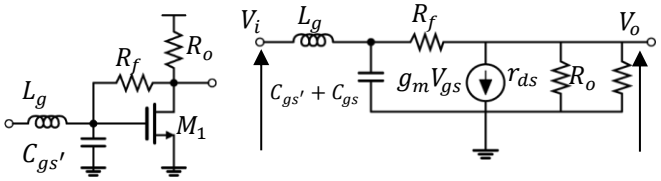
With the advance of CMOS technologies which offer very high f_T and f_{MAX}, g_m/I_D design methods introduced in the early 80's for low frequency design are more and more suited to RF application. Some works propose the use of a FOM such as $g_m f_T/I_D$ [1] or g_m^2/I_D [2] to determine the optimal operation region of a device for a RF application. In the case of specific RF building blocks design, some authors use the inversion level to optimize a particular FOM related to the studied function [3]. However, considering just a FOM could lead to non-optimal sizing when specific requirements are targeted. Other design methods have been proposed based on LUT in [4] or based on an abacus in [5]. Such approaches are efficient and accurate but the building of the LUT or the abacus is cumbersome. By replacing LUT or abacus by simple compact model such as EKV or ACM, a gm/I_D approach allows the designer to use the inversion level (i_f) as a design parameter to explore the design space as presented in [6].

In this trend we propose a simple analytical method for the sizing of a RF-LNA for Low Power applications such as IoT, in which the trade-off between gain, noise, and consumption has to be carefully optimized [7]. With this method the designer can choose, for a given gain and noise figure, the minimum inversion level to maximize the MOS efficiency and can size the circuit components with no need for intensive simulations or optimizations. The method is experimentally validated with a practical implementation in silicon.

In the second section, the analytical equations of the RF-LNA used in the method are introduced. The following section presents the compact model [8] used is this work. Then, section IV describes the sizing method and section V details the implementation in the 28 nm FD-SOI technology and the measurement results. Finally, section VI summarizes our main contributions.

II. RESISTIVE FEEDBACK LNA

The studied topology is shown in Fig. 1(a) with its small signal equivalent circuit in Fig. 1(b).



(a) (b)

Fig. 1: RF-LNA topology (a) and its small signal equivalent circuit (b).

The input impedance of the structure is given in (1)

$$Z_{in} = L_g p + \left(\frac{1}{(C_{gs'} + C_{gs})p} // Z_P\right) \quad (1)$$

with L_g the input inductance, C_{gs} the input parasitic capacitances of the transistor M_1, $C_{gs'}$ a parallel capacitance added for matching purpose and Z_p the impedance seen at the gate due to the resistive feedback which can be expressed as follows:

$$Z_p = R_p = \frac{R_l + R_f}{1 + g_m\ R_l} \quad (2)$$

with $R_l = r_{ds} // R_o$. Hence the real and imaginary part of Z_{in} can be written as:

$$R_e(Z_{in}) = R_{in} = \frac{R_l + R_f}{(1 + g_m\ R_l)(1 + Q^2)} \quad (3)$$

and

$$I_m(Z_{in}) = L_g\omega_0 - \frac{Q^2}{(1+Q^2)(C_{gs'}+C_{gs})\omega_0} \quad (4)$$

with

$$Q = R_p(C_{gs'}+C_{gs})\omega_0. \quad (5)$$

Considering the circuits in Fig. 1(b), the voltage gain at the matching frequency is given by:

$$G_t = \left|\frac{V_o}{V_i}\right| = |G_v|\sqrt{1+Q^2} \quad (6)$$

where G_v is the intrinsic gain of the RF-LNA topology given by:

$$G_v = \frac{V_o}{V_{gs}} = -\frac{(g_m R_f - 1)R_l}{R_l + R_f} \quad (7)$$

For a resistive feedback topology, the maximum noise figure NF_{max} is obtained when the inductor input L_g is null ($Q = 0$). By assuming $R_g \ll R_f$ and $\frac{1}{g_m} \ll R_f$ and considering gmR_g close to 1, NF_{max} is given by:

$$NF_{max} = 1 + \frac{(1+g_m R_g)^2}{R_g R_f g_m{}^2} + \frac{\gamma}{R_g g_m} + \frac{1}{R_g R_l g_m{}^2} \quad (8)$$

where R_g is the source impedance and γ is the excess noise factor.

III. Compact model for LNA sizing

Several compact models exist to describe the MOS transistor in all regions of operation. The most used are the EKV and ACM models which are both charge based models using a similar set of equations. In this work, we use the ACM terminolgy and equation sets but the given methodolgy can be also dervied following the EKV formalism. For the sake of simplicity and with the aim of deriving simple analytical expressions which can be easily handled for design, we used the simplest model which is based on only 3 physical parameters: the slope factor n, the normalized specific current I_{SQ} and the threshold voltage V_t, and one empirical parameter: the Early voltage V_A. Given the very high available f_T of the 28 nm FD-SOI, $L = 40\,nm$ is chosen to increase the gain margin. The main parameters of the transistor are given in TABLE I.

TABLE I. 40 nm LVT-RF MOS Characteristics

n	I_{SQ}	V_t
1.239	120.1 nA	371.6 mV

In a MOS transistor, the drain current can be expressed from the inversion level respectively in the drain (i_r) and in the source (i_f) as follows:

$$I_D = I_s(i_f - i_r) \quad (9)$$

with I_S the specific current which is technologically dependant and is defined as follows:

$$I_S = \mu C'_{ox} n \frac{\phi_t^2}{2}\frac{W}{L} = I_{SQ}\frac{W}{L}. \quad (10)$$

In saturation $i_f \gg i_r$ and the ratio g_m/I_D only depends on the inversion level i_f as follows:

$$\frac{g_m}{I_D} = \frac{2}{n\phi_t(\sqrt{1+i_f}+1)} \quad (11)$$

which gives a very simple equation to use in design. In addition, in saturation region, for $V_s = 0$, the gate voltage is related to the inversion level i_f by:

$$V_g - V_t = n\phi_t\left[\sqrt{1+i_f} - 2 + \ln\left(\sqrt{1+i_f}-1\right)\right] \quad (12)$$

In saturation region ($i_f \gg i_r$), based on (11) and (9), the MOS width is related to the inversion level i_f and the g_m as:

$$W(i_f) = \frac{L\, g_m\, n\, U_t}{2\, I_{sq}(\sqrt{1+i_f}-1)} \quad (13)$$

IV. LNA sizing

In this work, we target an intrinsic voltage gain $|G_v| = 6.15$ and a $NF = 2.5$. The first step of the proposed sizing method is to define the inversion level needed to achieve a given gain. To this end, the intrinsic voltage gain is derived as a function of i_f. To do so, the ratio g_m/I_D is introduced in the gain expression (7) through the Early voltage (V_A) as follows:

$$\begin{aligned} G_v &= -\frac{(g_m R_f - 1)}{1+\frac{R_f}{R_l}} \\ &= -\frac{k-1}{1+\frac{k}{\frac{g_m}{I_d}\frac{(V_{DD}-V_{DS})(V_A+V_{DS})}{V_{DD}+V_A}}} \end{aligned} \quad (14)$$

where $k = g_m R_f$. For low values of $V_A (i.e.\ V_{DD} \gg V_A)$ as it is the case in advanced technologies, G_v is maximum for $V_{DSOPT} = (V_{DD} - V_A)/2$. Hence, the maximum gain is obtained when:

$$r_{ds} = R_o = \frac{(V_{DD}+V_A)}{2I_D} \quad (15)$$

and is given by:

$$G_{v\_\max} = -\frac{k-1}{1+\frac{k}{\frac{g_m}{I_D}\frac{V_A+V_{DD}}{4}}} \quad (16)$$

Note that, when $V_{DD} \ll V_A$, as it is often the case in large technology nodes, R_o must be maximized to maximize the gain.

With (11) we can express the gain as a function of i_f as follows:

$$G_v(i_f) = -\frac{k-1}{1+\frac{2\,n\,U_t\,k(\sqrt{1+i_f}+1)}{V_A+V_{DD}}} \quad (17)$$

$G_v(i_f)$ and $g_m/I_D(i_f)$ are plotted in Fig. 2 from (17) and (11) for a 40 nm LVTN-RF transistor of the 28 nm FD-SOI technology from STMicroelectronics which is used in this study. In our case, we have chosen $k = 20$ to have sufficient headroom to comply with the gain requirement. As shown in Fig. 2, to perform a voltage gain of $|G_v| = 6.15$, the maximum inversion level is $i_f = 2.1$ which corresponds to $g_m/I_D =$

$22.6\,V^{-1}$. Note that a lower i_f could be chosen to further improve the efficiency. However, this leads to a larger transistor which will reduce the bandwidth. Hence, the maximum inversion level is the one that gives the targeted gain with the largest bandwidth.

In a second step, the value of g_m is determined for a targeted NF_{max}. With (8) we can derive g_m as a function of NF_{max} as follows:

$$g_m \approx \frac{\gamma + \frac{1}{G_v}}{R_g(NF_{max} - 1)} \tag{18}$$

From (18), with $\gamma = 0.808$, the required g_m to perform a $NF_{max} = 2.49$ is 13.1 mS.

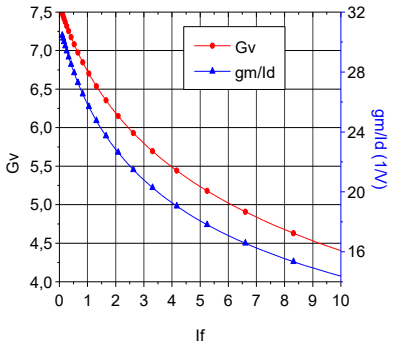


Fig. 2: $G_v(i_f)$ and $g_m/I_D(i_f)$ for k=20, V_{DD}=1V, V_A =650mV, n=1.239

From that point, the sizing of the circuit is straight forward. Knowing g_m and g_m/I_D, the bias current can be evaluated, resulting in $I_D = 579\,\mu A$. Assuming that $i_r = 0$ in saturation region, the width of the transistor is obtained with (9) and (10) resulting in $78.5\,\mu m$ in our case study. From (15) the load resistance is $R_o = 1.43\,K\Omega$ and the feedback resistance is $R_f = 1.6\,K\Omega$ to have the chosen k factor ($k = 20$). From (2) the equivalent input resistance seen at the gate is $R_p = 224\,\Omega$.

On the basis of (3), (4) and (5), the impedance matching is done as follows. Knowing R_p, the input Q factor needed to synthesize 50 Ω is calculated with (3) and is 1.86. The value of the capacitance added in parallel with $C_{gs}(C'_{gs})$ is evaluated with (5) and the inductor needed to cancel the imaginary part is calculated with (4). With this approach, it is possible to match the LNA for different frequencies up to a maximum frequency given by:

$$f_{max} < \frac{Q}{(1+Q^2)R_{in}C_{gs}} \tag{19}$$

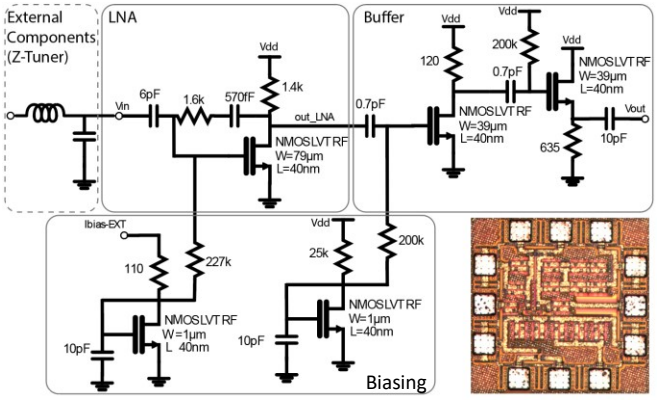
TABLE II gives L_g and C'_{gs} for different matching frequencies.

TABLE II. COMPONENT VALUES FOR TUNER MATCHING

Freq (GHz)	C'_{gs} (pF)	L_g (nH)
1	1.31	14
1.8	0.72	8.2
2.4	0.53	6.2

V. IMPLEMENTATION AND MEASUREMENTS

The LNA has been designed with the 28 nm FD-SOI technology from STMicroelectronics. The schematic and the die photograph of the complete circuit are given in Fig. 3. Given that the aim of this work is to validate a design method, L_g and C'_{gs} are not included in the test chip to facilitate the test at multiple frequencies and a DC block capacitor of 6 pF has been included. An active output buffer is integrated for measurements under 50 Ω environment. The core area is 0.07 mm^2.



a) b)

Fig. 3: Schematic (a) and die photograph (b) of the implemented circuit

The post layout simulations of the gain of the integrated circuit are given in Fig. 4. The maximum gain (MaxGain) is the gain of the matched device at all frequencies. The DC gain of the LNA is in good agreement with the target stated in the analytical sizing. At 1 GHz a discrepancy of 1.5 dB is observed due to frequency behaviour which is not taken into account in the presented methodology. The simulated gain of the buffer is -3.5 dB and the maximum gain at 1 GHz is 18.4 dB which corresponds to G_t.

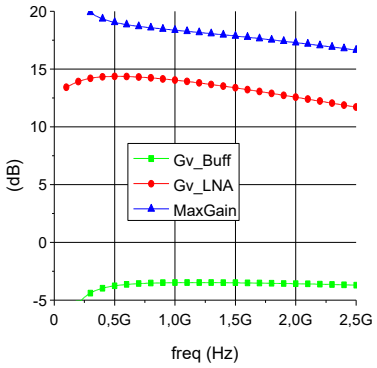
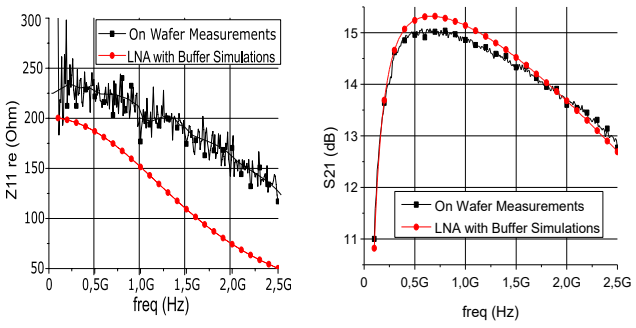


Fig. 4: Simulations of the buffer, the LNA and the maximum gain.

As shown in Fig. 5, on-wafer measurements show good agreement between simulation and measurements. The measured DC value of R_p is 225 Ω and the $S_{21} = 15$ dB at 1 GHz. The LNA consumes $570\,\mu A$ (instead of $579\,\mu A$ in simulation).



a) b)

Fig. 5: On-wafer measurement of Re(Z11) a) and S21 b).

The circuit has been mounted on a FR4 PCB using a Chip On Board (COB) assembling technic. Measurements were performed with an impedance tuner (MAURY MICROWAVE 8045D) to synthesize L_g and C'_{gs}. Fig. 6 compares measurements with post layout simulations including a model of the die to PCB interconnection obtained with EM simulation and the measured S parameters of the impedance tuner. Simulations and measurements are in good agreement. The measured gain of the complete device is 18 dB which is close to the simulated maximum gain (18.4 dB). The bandwidth reduction comes from the impedance tuner and does not occur when lumped components are used as shown by simulation in Fig. 6a. This is confirmed by S_{11} simulation and measurement shown in Fig. 6c. The output buffer offers a wide matching bandwidth with a S_{22} lower than -10 dB from 595 MHz to 2.55 GHz. The measured noise figure is 3.3 dB and is slightly higher than the simulated one due to extra losses which has been underestimated in EM simulations. The IIP3 of the circuit is highly degraded by the buffer and is measured at -24.8 dBm. However, the simulation of the LNA without the buffer shows an IIP3 of -14.8 dBm.

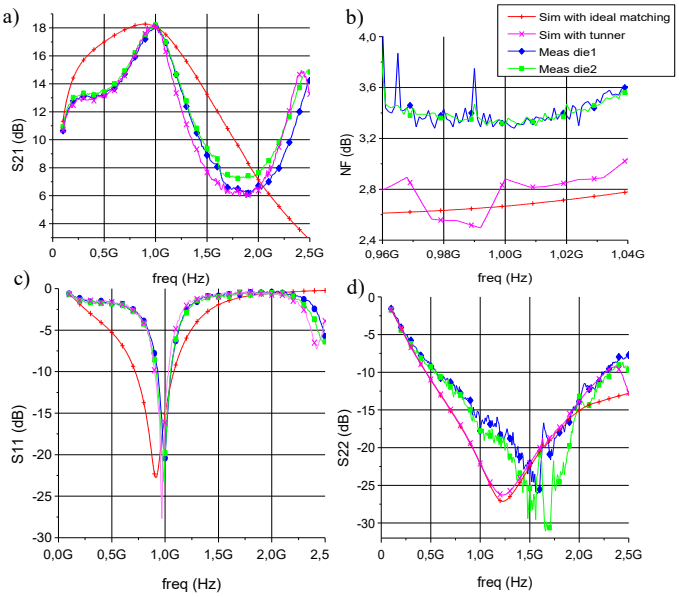


Fig. 6: Simulations and measurements of the S21 (a), NF (b), S11 (c) and S22 (d) of the circuit matched at 1GHz

Measurements have been achieved at 3 different matching frequencies and are reported in TABLE III where performances are summarized and compared with state-of-the-art resistive feedback LNAs. This circuit shows good power efficiency and achieves a reduced power consumption while maintaining an acceptable trade-off between gain and noise figure. A figure of merit (FoM) is used to compare the overall performance of the LNAs and it is given by:

$$FoM = \frac{G_{v[lin]}}{(F_{[lin]} - 1)I_{[mA]}} \qquad (20)$$

VI. Conclusion

This work presents a simple design method using a g_m/I_D approach suited for low power LNA in advanced technologies. It allows a fast and first-time right design of the LNA, based on a simple analytical study by using a compact model of the MOS transistor valid in all regions of operation. Thanks to this method, the designer can choose the inversion level that guarantees a given gain while ensuring a target NF. The method is validated through a practical design in an advanced technology for which a time-consuming CAD-based approach is generally used. Measurements show a good agreement between analytical sizing and experimental results demonstrating the robustness of the method in an industrial framework. As discussed in the paper, the method allows the exploration of the design space which gives the maximum inversion level needed to achieve the target performances. Lower inversion levels could also be used with the risk of lowering the bandwidth. Improving this method to take into consideration the effect of i_f on the bandwidth could be an interesting extension of this work.

TABLE III. Performance Summary and Comparison of RF-LNA

Ref	Frequency (GHz)	S11 (dB)	Gain (dB)	NF (dB)	IIP3 (dBm)	I_{dc} (mA)	Technology (nm)	External Comp.	Area (mm²)	FoM
This work	1	<-20	18	3.31	-24.86 -14.8*	0.57	28 FD-SOI	Yes	0.07	12.2
	1.3	<-10	17.84	3.5	-24.63 -14.8*					11.04
	1.8	-18	17.44	3.85	-24.48 -14.8*					9.16
[9]	1.57		18	2.5-3.8		2.14-3.28	28 FD-SOI	Yes		4.77 1.73
[10]	0.9	-16.6	13.87	0.98	-12	4.36	130 CMOS	Yes	0.047	4.47
[11]	2.4	-11	24	2	-22.4 -11*	4	130 CMOS	No	0.6	6.77
	2.4	-11	29	1.2	-21.5 -11*	3.5	130 CMOS	Yes	0.6	25.3
[12]	0.1-7	<-10	12.6	5.5-6.5	-6 -9	1.5	90 CMOS	No	0.23	1.12 0.82
[3]	0.2-6	<-10	17	3	7.9	3.36	28 FD-SOI	No	0.005	2.11
	0.2-3.9	<-10	15.7	3.1	8.7	2.75	65 CMOS			2.13
	0.1-2.1	<-10	19.2	2.4	8.6	2.38	130 CMOS			5.18

*LNA only

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