A 5-DC-parameter MOSFET model for circuit simulation in QucsStudio and SPECTRE

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***Abstract*—A minimalist MOSFET model for circuit simulation with only five DC parameters written in Verilog-A is presented. The five parameters can be extracted from direct and simple methods in common circuit simulators. The DC characteristics of transistors in both 180-nm bulk CMOS and 28-nm FD-SOI technologies generated by the five-parameter model are compared with those generated by the BSIM and UTSOI2 models, respectively. The simulation of some basic circuits using the proposed 5-DC-parameter MOSFET model shows good matching with the simulation using the BSIM model, at the benefit of a much simpler set of DC parameters.**

***Index Terms*—MOSFET modeling, circuit simulation, Verilog-A, QucsStudio**

I. INTRODUCTION

Many compact models of the MOS transistor have been developed along with the advances in CMOS technologies [1]–[4]. The early models were simple, based on physics, but used different equations for each operating region of the transistor [5]. In the meantime, the family of BSIM models was developed and adopted in circuit simulators [6]. Unfortunately, BSIM models are made up of an extremely complex set of equations characterized by several tens of parameters, many of them lacking clear physical meaning. A compact model with a reduced number of parameters should facilitate the understanding of the MOS transistor by designers, particularly the ones with little experience.

The Advanced Compact MOSFET (ACM) model has proved to be an interesting model for simulation and design [7], since the inclusion of only one short-channel parameter to the long-channel model rendered a 4-parameter model (4PM) that has successfully simulated MOS circuits operating at low voltages.

This work proposes a minimalist 5-parameter model (5PM), which consists of single-piece functions and is not restricted to the low-voltage domain. The 5 parameters are the threshold voltage V_{T0}, the specific current I_S, the slope factor n, the drain-induced barrier lowering (DIBL) coefficient σ and the parameter ζ associated to saturation velocity.

The paper is organized as follows. Section II introduces the main equations of the 5PM. Section III presents the extraction method of the velocity saturation parameter. Section IV validates the proposed 5PM for a 180-nm bulk CMOS and a 28-nm FD-SOI technologies against the BSIM 4.5 and UTSOI2 [8]- [9] models, respectively. Section V addresses the temperature dependence of each parameter of the 5PM and the noise model. In Section VI, a CMOS inverter and a ring oscillator exemplify the influence of the velocity saturation parameter in circuit simulations.

II. THE 5-PARAMETER MODEL

The 5PM takes into account both the drift and diffusion components of the current as well as the saturation velocity phenomenon [10], yielding (1).

$$I_D = I_S \frac{(q_S + q_D + 2)}{1 + \zeta \left| q_S - q_D \right|} (q_S - q_D) \tag{1}$$

The normalized inversion charge densities at source (q_S) and drain (q_D) are defined as the inversion charge densities $Q_{S(D)}$ normalized to the thermal charge density $-nC_{ox}\phi_t$ as given in (2).

$$q_{S(D)} = \frac{Q_{S(D)}}{-nC_{ox}\phi_t} \tag{2}$$

where C_{ox} is the the oxide capacitance per unit area, n is the slope factor and ϕ_t is the thermal voltage.

The specific current I_S, given in (3), is related to the gate width W and length L, and to technology parameters. μ is the carrier mobility.

$$I_S = \mu C_{ox} n \frac{\phi_t^2}{2} \frac{W}{L} \tag{3}$$

Parameter ζ is a short-channel parameter associated with the velocity saturation (v_{sat}) phenomenon. It is defined by (4) as the ratio of a diffusion-related velocity to the saturation velocity.

$$\zeta = \frac{\mu \phi_t / L}{v_{sat}} \tag{4}$$

The saturated drain current I_{Dsat} is related to the drain charge density Q_{Dsat} as

$$I_{Dsat} = -W v_{sat} Q_{Dsat} \tag{5}$$

From (1) and (5), the drain charge density normalized to the thermal charge density is given by

$$q_{Dsat} = q_S + 1 + \frac{1}{\zeta} - \sqrt{\left(1+\frac{1}{\zeta}\right)^2 + \frac{2q_S}{\zeta}} \qquad (6)$$

The unified charge-control model (UCCM) in (7) describes the relationship between the terminal voltages and the normalized charge densities at source and drain.

$$\frac{V_P - V_{S(D)B}}{\phi_t} = q_{S(D)} - q_{Dsat} - 1 + \ln(q_{S(D)} - q_{Dsat}) \quad (7)$$

The pinch-off voltage V_P is linearly approximated by (8). The introduction of σ, DIBL coefficient, at both source and drain, keeps the device symmetry. V_{T0} is the equilibrium threshold voltage.

$$V_P = \frac{V_{GB} - V_{T0} + \sigma V_{DB} + \sigma V_{SB}}{n} \qquad (8)$$

The source and drain charge densities q_S and q_D are calculated using (7), which is an extended version of the UCCM that includes the velocity saturation phenomenon.

It is important to remark that (1) and (7) preserve the symmetry of the transistor, $i.e.$ if we interchange q_S and q_D, both I_D and V_{DS} change sign.

Fig. 1 compares the single-piece model of saturation proposed herein with the most traditional one, which determines V_{DSsat} as in [11]. Note that [11] uses the interpolation function introduced in [12] to obtain the continuity between the triode and the saturation regions.

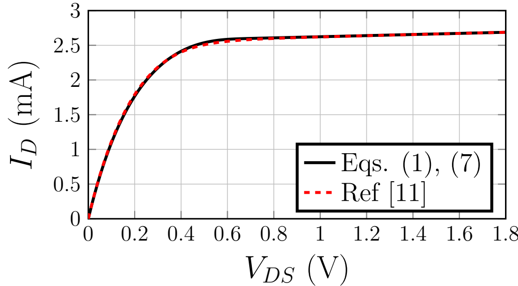

Fig. 1. DC characteristics $I_D \times V_{DS}$ with $V_{GB} = 1.8$ V of the n-channel MOSFET with W/L = 5 μm/0.18 μm from the 0.18 μm CMOS technology using equations (1), (7) and [11].

III. Parameter Extraction

The 5PM parameters are extracted by means of a set of simple circuits that can be measured either by simulation or in a workbench. The methodologies employed to extract V_{T0}, I_S, n and σ in this work are similar to those presented in [7].

The velocity saturation parameter ζ [10] that completes the 5PM can be found from either simulation or measurement of the g_m/I_D characteristic of a transistor in saturation compared with the $(g_m/I_{D,SAT})_{4PM}$ from simulation using the 4PM. The value of i_d for which the g_m/I_D value of the saturated transistor is one half of $(g_m/I_{D,SAT})_{4PM}$, as shown in Fig. 2, is used to determine the value of ζ. Here, g_m is the gate

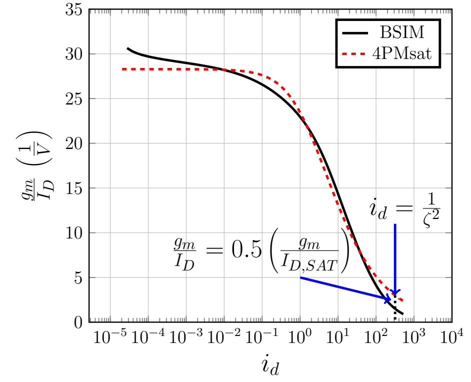

Fig. 2. DC characteristic $g_m/I_D \times i_d$ used to extract ζ.

transconductance and i_d is the drain current normalized to the specific current (I_S).

The parameters of the 5PM were extracted for 180-nm bulk CMOS and 28-nm FD-SOI technologies. Table I presents the extracted parameters of the NMOS and PMOS transistors standard threshold voltage (SVT) of the 180-nm CMOS process and low threshold voltage (LVT) of the 28-nm FD-SOI technology.

TABLE I
Extracted Parameters

Technology	**180 nm**		**28 nm**	
Transistor	**NMOS**	**PMOS**	**NMOS**	**PMOS**
W/L (μm/μm)	5/0.18	5/0.18	1/0.06	1/0.06
V_{T0} (mV)	528	- 525	389	- 404
I_S (μA)	5.52	1.82	3.15	0.76
n	1.37	1.40	1.15	1.01
ζ	0.056	0.035	0.039	0.024
σ	0.027	0.024	0.018	0.029

IV. DC Characteristics

Fig. 3 shows simulations of the diode-connected NMOS transistor from the 0.18 μm technology node in Table I. The 5PM was implemented in Verilog-A following a process similar to that in [7]. The results of the 5PM and the 4PM are compared to the BSIM 4.5 model implemented in the simulator.

The DC characteristics in Fig. 4-5 were obtained for the LVT transistor of the 28-nm FD-SOI technology in Table I. The results are compared to the UTSOI2 compact model.

The results in Fig. 3-5 show good matching of the 5PM with the simulation runs of the process design kit models. Hence, the simple 5PM is well adapted to model short-channel transistors.

V. Temperature and Noise

Each one of the 5 parameters was extracted for a temperature range of -25°C to 125°C. Fig. 6 shows the temperature dependence of each parameter. To incorporate the temperature variation in the simulation model, fitting curves were found for each parameter.

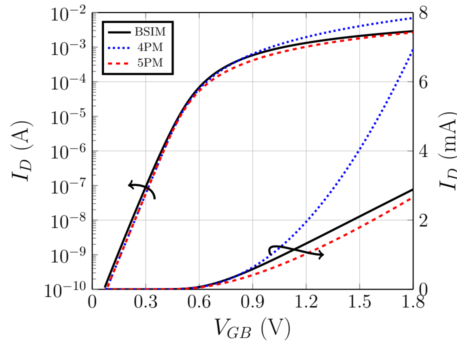

Fig. 3. DC characteristics $I_D \times V_{GB}$ at $V_{GB} = V_{DB}$ of the SVT n-channel MOSFET with W/L = 5 μm/0.18 μm from a 0.18 μm CMOS process.

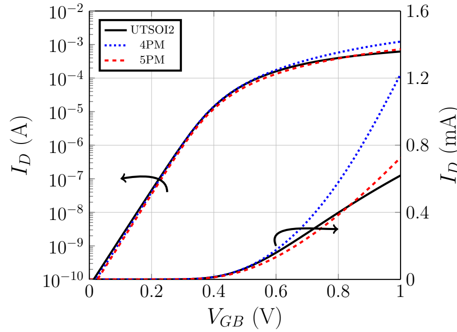

Fig. 4. DC characteristics $I_D \times V_{GB}$ with V_{DS} = 500 mV of the LVT n-channel MOSFET with W/L = 1 μm/60 nm from a 28-nm FD-SOI technology.

The threshold voltage dependence on the temperature, which is linear as expected from its physical definition [13] - [14], is given by (9).

$$V_{T0}(T) = V_{T0}(T_{ref}) + \alpha_{V_{T0}}(T - T_{ref}) \tag{9}$$

The specific current varies with temperature partially due to the mobility variation with temperature. The fitting expression (10) was derived based on the assumption that the mobility is proportional to $T^{-\alpha}$ [13], in which α is a fitting coefficient.

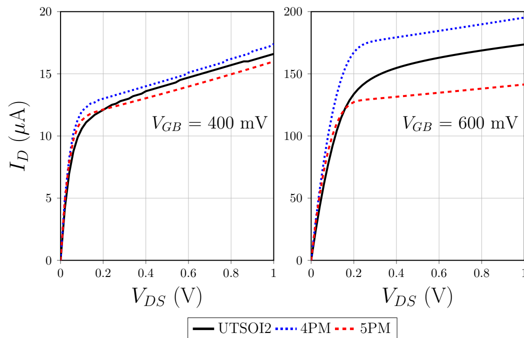

Fig. 5. DC characteristics $I_D \times V_{DS}$ with V_{GB} = 400 mV and of V_{GB} = 600 mV of the LVT n-channel MOSFET with with W/L = 1 μm/60 nm from the 28-nm FD-SOI technology.

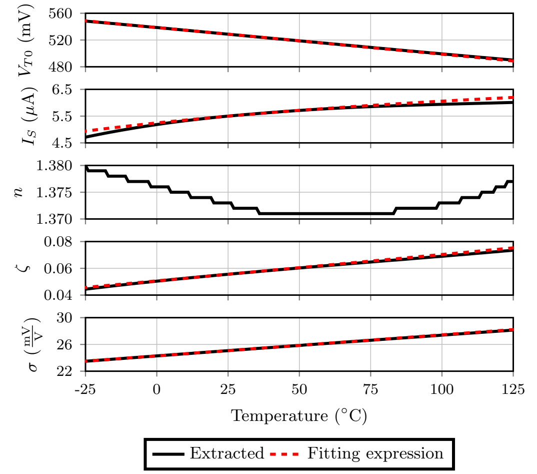

Fig. 6. Temperature variation of the 5 parameters (from top to bottom): $V_{T0}(T)$, $I_S(T)$, n, $\zeta(T)$ and $\sigma(T)$) and respective fitting curves for the NMOS transistor from the 0.18 μm CMOS process in Table I.

$$I_S(T) = I_S(T_{ref}) \left[1 + \frac{(2-\alpha)}{T}(T - T_{ref})\right] \tag{10}$$

The slope factor n is almost constant over the whole temperature range. The short-channel parameters ζ and σ also present a linear dependency on the temperature.

The fitting expressions have been determined for a reference temperature T_{ref} = 300 K. The temperature coefficients employed are $\alpha_{V_{T0}} = -0.4$ mV/K, α =1.5, $\alpha_\zeta = 0.2 \times 10^{-3}$ K^{-1}, and $\alpha_\sigma = 0.32 \times 10^{-6}$ K^{-1}. With these fitting parameters, the designer extracts the 5 parameters at T_{ref} to simulate MOS circuits over a wide range of temperatures.

Thermal and flicker noise valid for all regions of operation were included in the model, as in [15]. Fig. 7 shows the simulated PSDs of the channel noise for various operating points, which are consistent with the expected MOSFET noise models, despite some differences between the 5PM and BSIM.

VI. Circuit Examples

This section presents the simulations of a CMOS inverter and an 11-stage ring oscillator of a 180-nm bulk technology, using the 5PM, 4PM and BSIM 4.5 models.

The 5PM was carried out with two description languages, namely Verilog-A [16] and Verilog-AMS [17], the former to simulate circuits in Cadence® Virtuoso® Spectre® simulator [18] and the latter for simulation in the open-source software QucsStudio [19] - [20].

A. Inverter

The inverter herein is composed of SVT transistors with the respective geometry and extracted parameters presented in Table I.

Fig. 8 shows the simulated voltage transfer characteristic (VTC) and the short-circuit current I_{SC} for three values of the supply voltage. The DC characteristics of the inverter using either 4PM or 5PM presented results very similar to BSIM's.

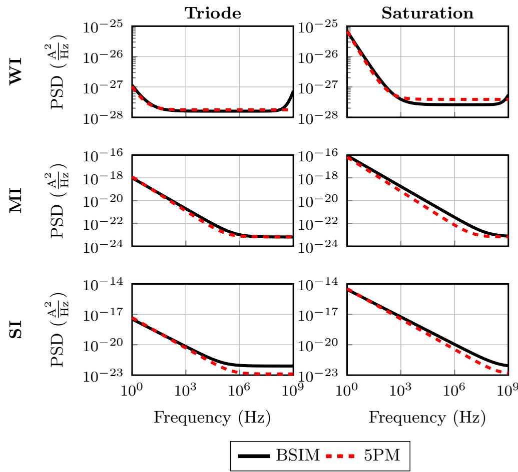

Fig. 7. Noise simulation results of the power spectral density (PSD) for SVT n-channel transistor with W/L = 5 μm/0.18 μm from 0.18 μm CMOS process. Operating points: in triode $V_D = 13$ mV and saturation $V_D = 1.8$ V; in weak inversion (WI) $V_G = 100$ mV, moderate inversion (MI) $V_G = V_{T0} = 528$ mV, strong inversion (SI) $V_G = 1$ V.

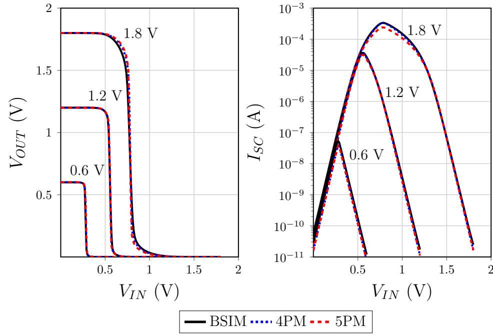

Fig. 8. VTC and short-circuit current of a CMOS inverter for the 4PM, 5PM and BSIM model.

An important characteristic of a CMOS inverter is the high-to-low transition time, which requires the knowledge of the transistor capacitances for its evaluation. For a proper comparison of the models, both the 4PM and 5PM included intrinsic capacitances as in [7]. In addition, the total output capacitance was extracted (13.8 fF) using the BSIM model and included as a load for the 4PM and 5PM simulations.

To determine the high-to-low transition at $V_{DD} = 1.8$ V, a voltage step was applied to the inverter input. Fig. 9 shows both the inverter response to a step and the pull-down current for the 4PM, 5PM, and BSIM model.

Fig. 9 highlights the effect of the velocity saturation parameter, which results in a transient current similar to BSIM's. As can be noted, the 4PM simulation shows a peak current which is twice the value of the maximum current in the 5PM. The 5PM produces a high-to-low transition much closer to BSIM's response than the 4PM.

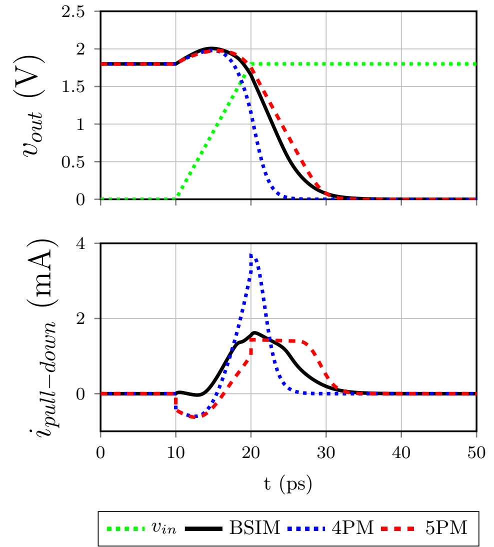

Fig. 9. Output voltage (top) and pull-down current (bottom) response to a step from 0 to 1.8 V, rise time of 10 ps applied to the inverter for 4PM, 5PM and BSIM model.

B. Ring oscillator

The ring oscillator is a basic circuit widely used in digital systems [21]. Fig. 10 shows the simulation of an 11-stage ring oscillator with a supply voltage of 1.8 V. The oscillation frequencies are 1.83 GHz, 1.81 GHz and 2.63 GHz using BSIM, 5PM and 4PM ($\zeta = 0$), respectively. The inclusion of the velocity saturation parameter rendered a significant improvement in the accuracy of the oscillation frequency.

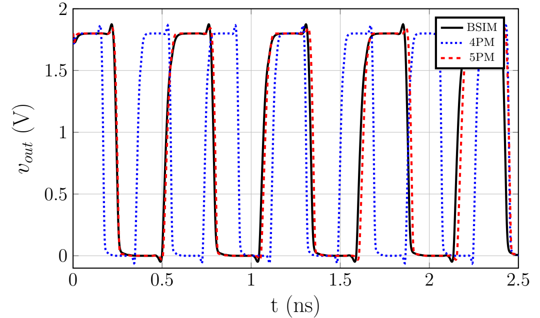

Fig. 10. Output voltage of the simulated 11-stage ring oscillator for 4PM, 5PM and BSIM model

VII. Conclusion

This paper introduced the main equations of the 5-parameter model of the MOSFET. The model consists of simple single-piece functions, derived from physics. The 5PM includes the effect of the velocity saturation in the UCCM, thus avoiding the use of interpolation functions routinely employed in compact models. The methodology to extract the velocity saturation parameter was presented along with the effect of this fifth parameter on the DC characteristics of n-channel transistors from two different technologies.

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