A 5-DC-parameter MOSFET model for circuit simulation in QucsStudio and SPECTRE

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Outline

- Introduction
- Velocity saturation effects
- Parameter extraction
- Intrinsic capacitances including velocity saturation and DIBL
- Circuit examples

Introduction: democratizing IC design

Open source PDK

Open source EDA tools

Open source IP & libraries

Available compact MOSFET models

We propose: **simple 5-DC-parameter MOSFET model**

Velocity saturation effects

Normalized current vs. normalized charge densities ⇒

$$i_D = \frac{(q_S + q_D + 2)}{1 + \zeta |q_S - q_D|}(q_S - q_D)$$

short-channel parameter :

$$\zeta = \frac{(\mu_s \phi_t / L)}{v_{sat}}$$

diffusion-related velocity /saturation velocity

Saturation current due to saturation velocity of the carriers

$$I_{Dsat} = -W Q_{Dsat} v_{sat}$$

Q_{Dsat} is the saturation inversion charge density at the drain end of the channel

or using normalized variables

$$i_{Dsat} = \frac{2}{\zeta} q_{dsat}$$

Physics-based saturation: design model

$$i_{Dsat} = \frac{2}{\zeta} q_{dsat}$$

$$i_{Dsat} = \frac{(q_S + q_{Dsat} + 2)}{1 + \zeta(q_S - q_{Dsat})}(q_S - q_{Dsat})$$

$$q_{Dsat} = q_s + 1 + \frac{1}{\zeta} - \sqrt{\left(1 + \frac{1}{\zeta}\right)^2 + \frac{2q_S}{\zeta}}$$

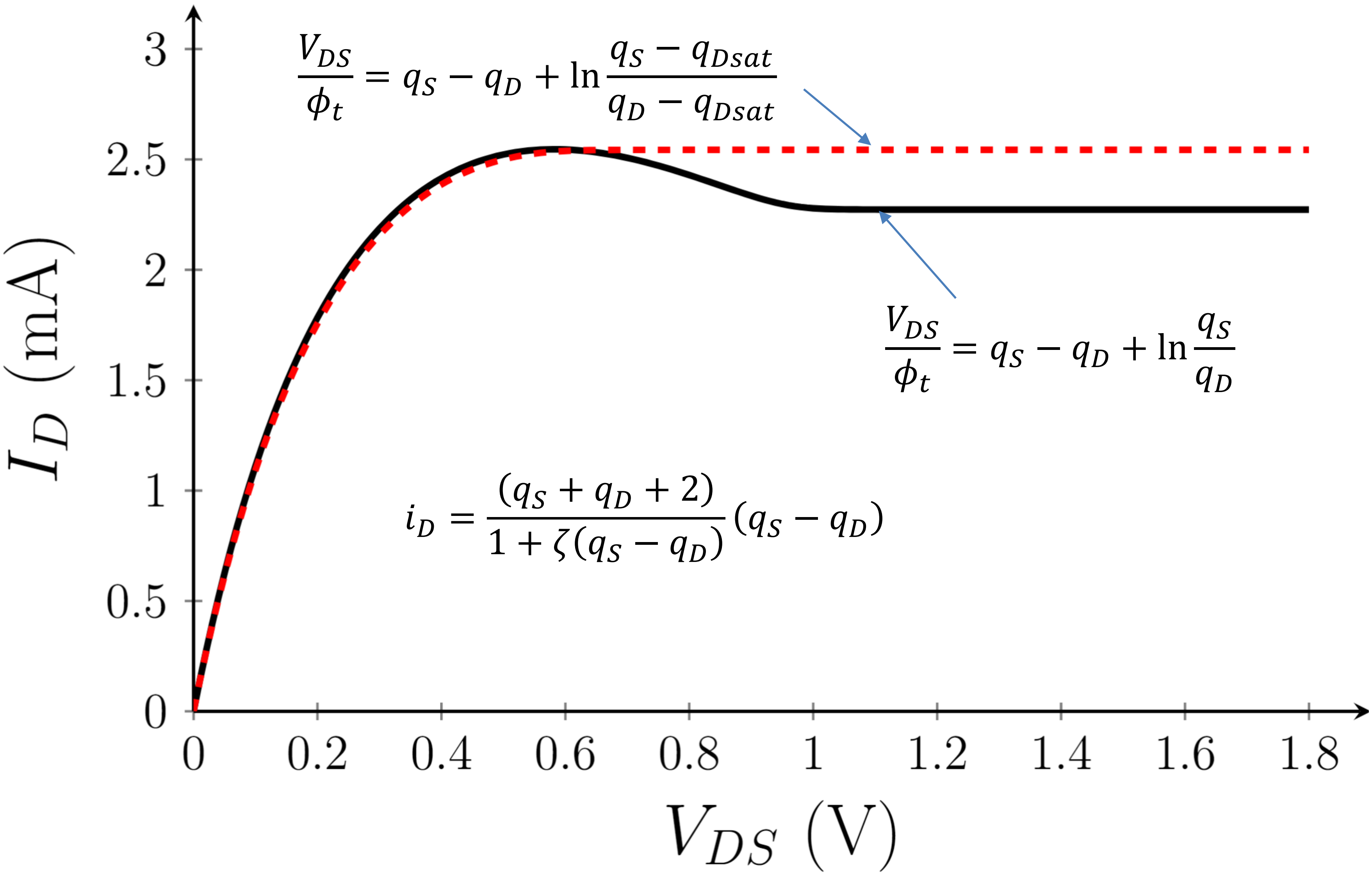
***U**nified **C**harge **C**ontrol **M**odel including the effect of velocity saturation*

$$\frac{V_P - V_{SB}}{\phi_t} = q_S - 1 + \ln q_S$$

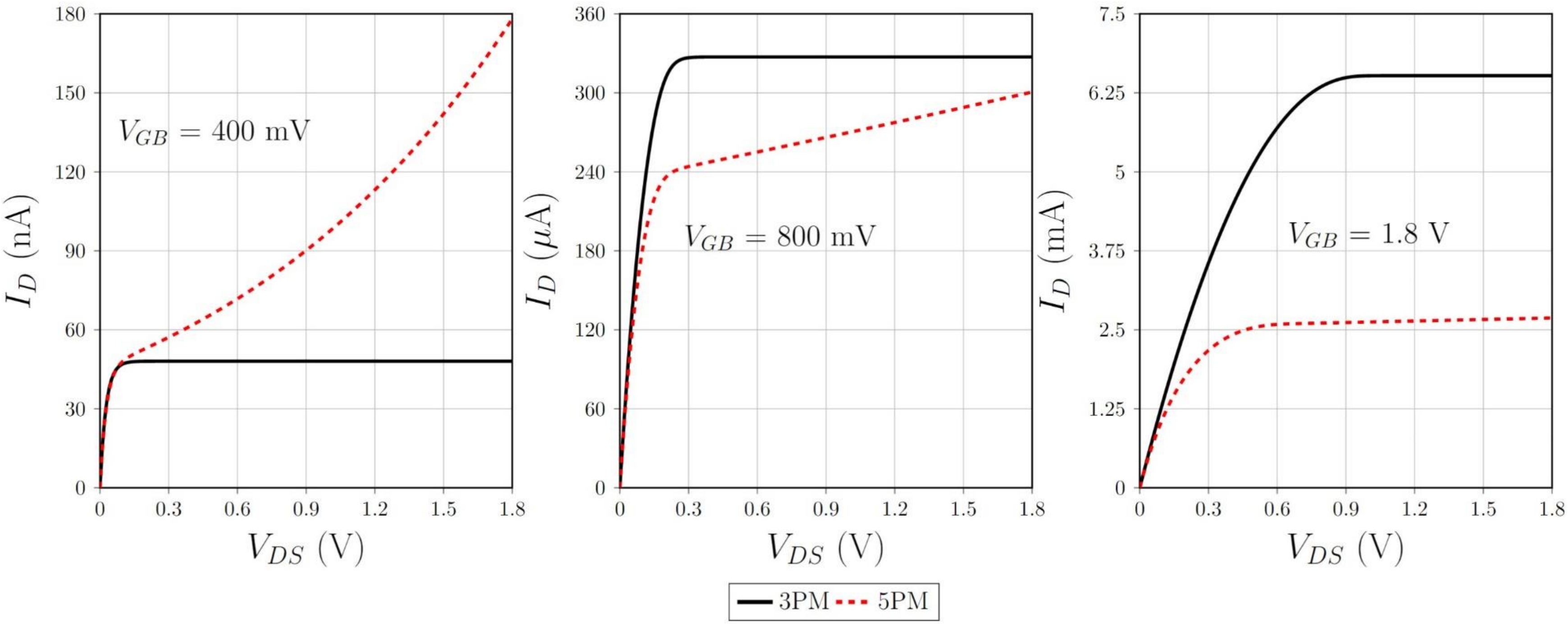
$$\frac{V_{DS}}{\phi_t} = q_S - q_D + \ln \frac{q_S - q_{Dsat}}{q_D - q_{Dsat}}$$

ϕ_t= 26 mV@ 300K

Effect of the maximum of $i_D(q_D)$ on the output characteristic $i_D(v_D)$



Output characteristics including DIBL and v_{sat}



$$DIBL\ model:\ V_T = V_{T0} - \sigma(V_{SB} + V_{DB})$$

Transistor	W/L $(\mu m/\mu m)$	V_{T0} (mV)	I_S (μA)	n	σ	ζ
NMOS2V	$\mathbf{5/0.18}$	528	5.52	1.37	0.025	0.056

V_T I_S and n extraction: The g_m/I_D method

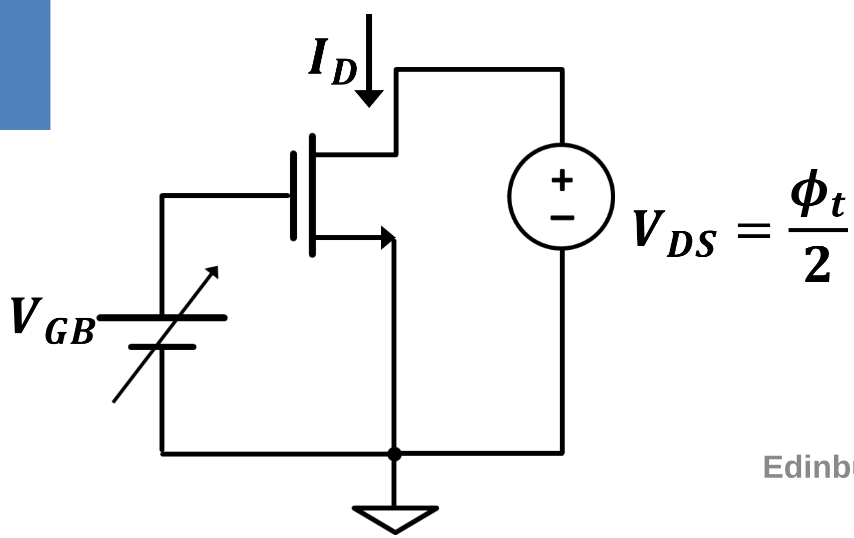
$$g_{ms} = \mu \frac{W}{L} n C_{ox} \phi_t q_S = \frac{2I_S}{\phi_t} q_S$$

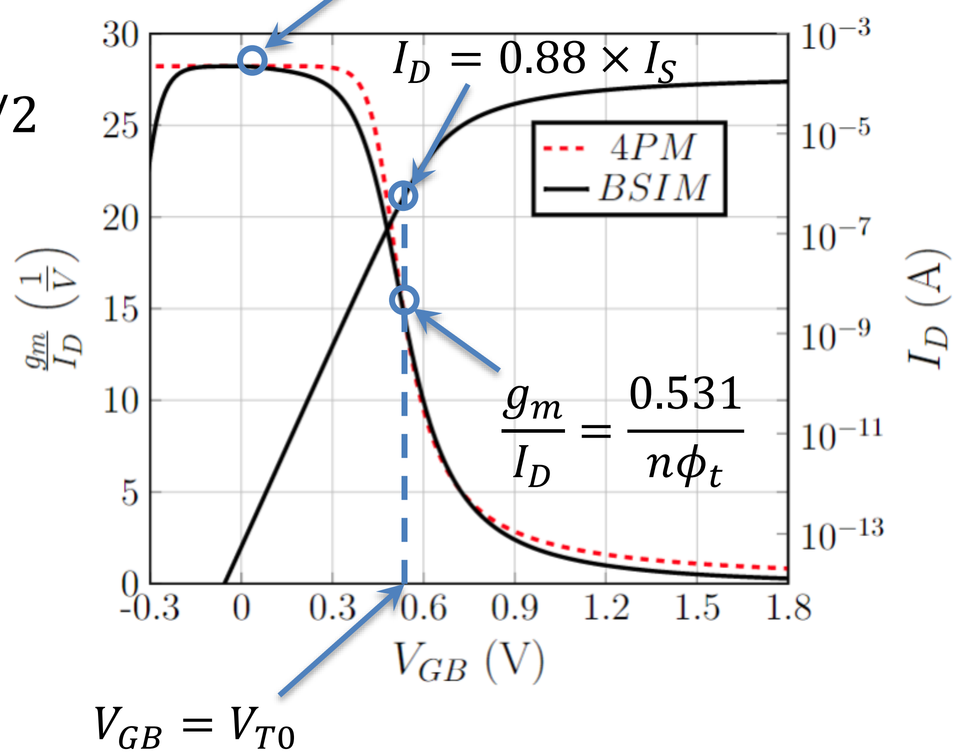
$$\left.\frac{g_m}{I_D}\right|_{V_{DS}\to 0} = \frac{1}{n\phi_t(1+q_S)}$$

Thus, at threshold (q_S = 1) g_m/I_D is at
½ of its maximum value,

$$\left(\frac{g_m}{I_D}\right)_{max} \cong \frac{1}{n\phi_t}$$

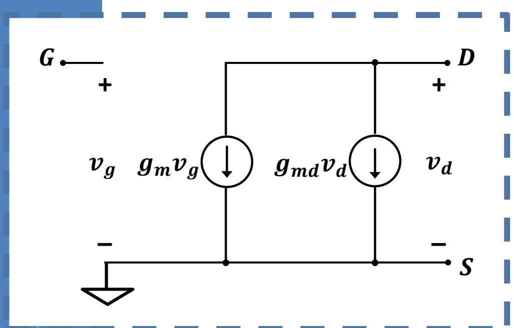
$$I_D(q_S = 1, V_{DS} = \phi_t/2) \cong g_{ms}\phi_t/2 = \frac{2I_S}{\phi_t}\phi_t/2 = I_S$$

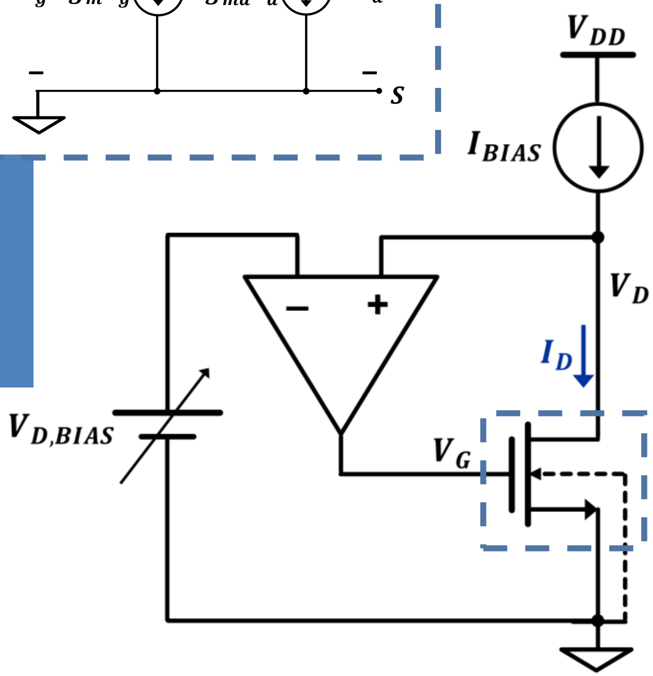




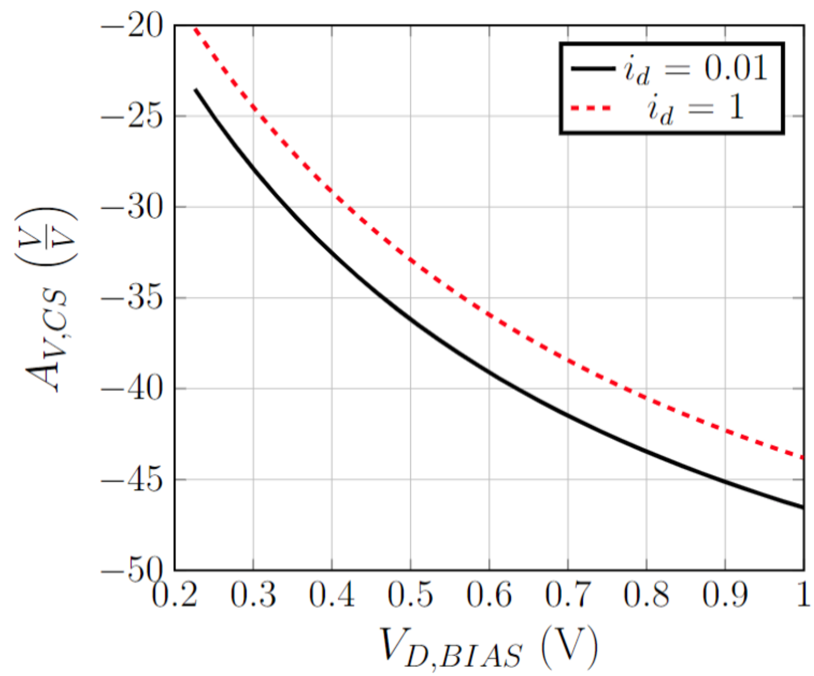
Extraction of σ in WI (MI) in saturation

Common Source Intrinsic Gain method





$$A_{V,CS} = \frac{v_d}{v_g} = -\frac{g_m}{g_{md}} = -\frac{\dfrac{g_m}{I_{D,sat}}}{\dfrac{g_{md}}{I_{D,sat}}} = -\frac{\dfrac{1}{\phi_t}\left(\dfrac{1}{n}\right)\dfrac{2}{q_S+2}}{\dfrac{1}{\phi_t}\left(\dfrac{\sigma}{n}\right)\dfrac{2}{q_S+2}} = -\frac{1}{\sigma}$$

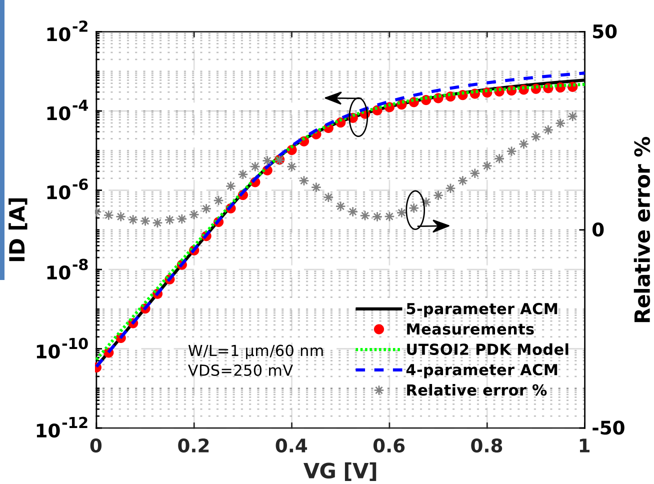


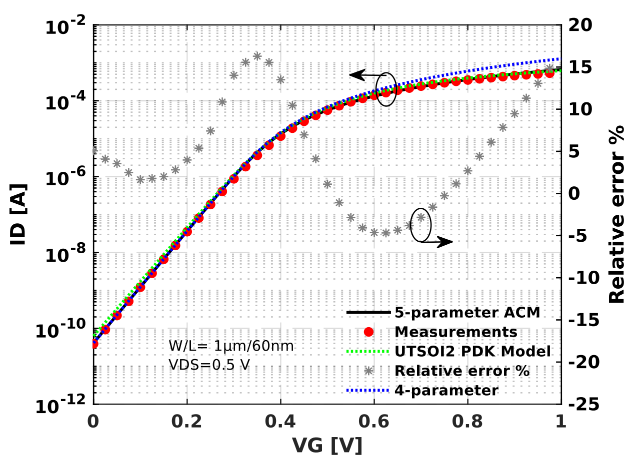
28 nm FD-SOI technology DC characteristics

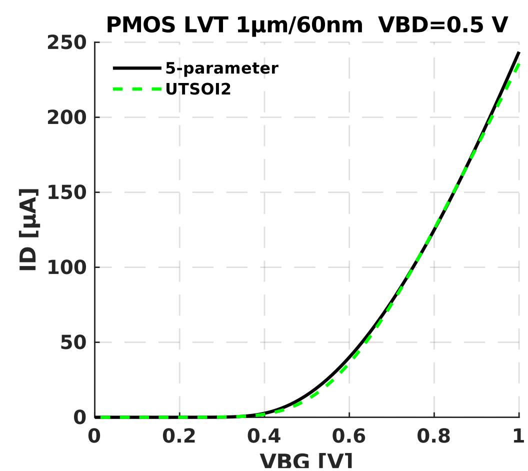
Parameter extraction for L=60 nm

Transistor	W/L	V_{T0} (mV)	I_S (μA)	n	σ	ζ
LVTNMOS	1µm/60 nm	390.5	3.25	1.138	0.018	0.039
LVTPMOS	1µm/60 nm	403.6	0.755	1.014	0.029	0.024

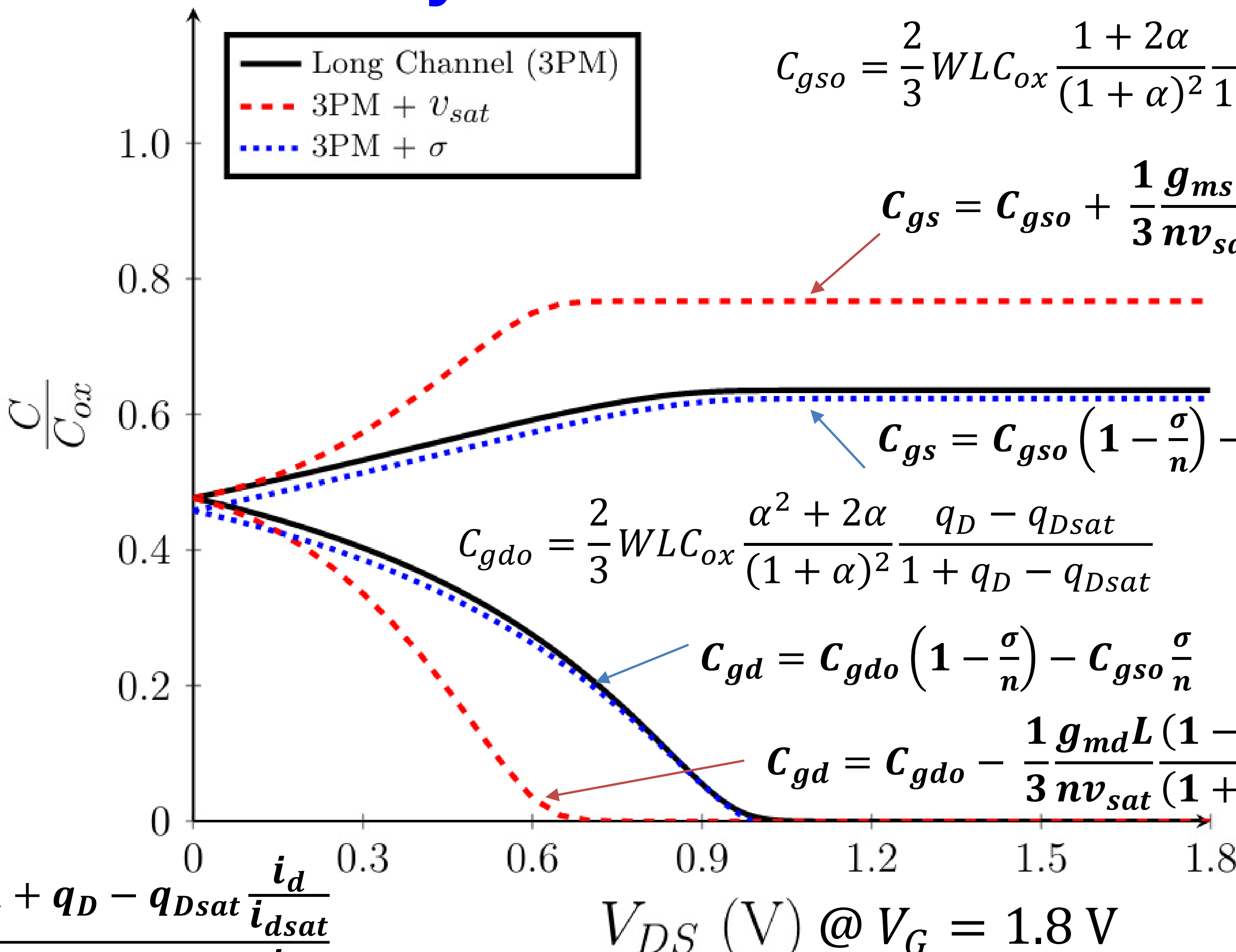
Model Verification: NMOS & PMOS TRANSISTORS







Intrinsic capacitances including velocity saturation and DIBL



$$C_{gso} = \frac{2}{3} W L C_{ox} \frac{1+2\alpha}{(1+\alpha)^2} \frac{q_S - q_{Dsat}}{1 + q_S - q_{Dsat}}$$

$$\boldsymbol{C_{gs} = C_{gso} + \frac{1}{3} \frac{g_{ms} L}{n v_{sat}} \frac{(1-\alpha)^2}{(1+\alpha)^2}}$$

$$\boldsymbol{C_{gs} = C_{gso}\left(1 - \frac{\sigma}{n}\right) - C_{gdo}\frac{\sigma}{n}}$$

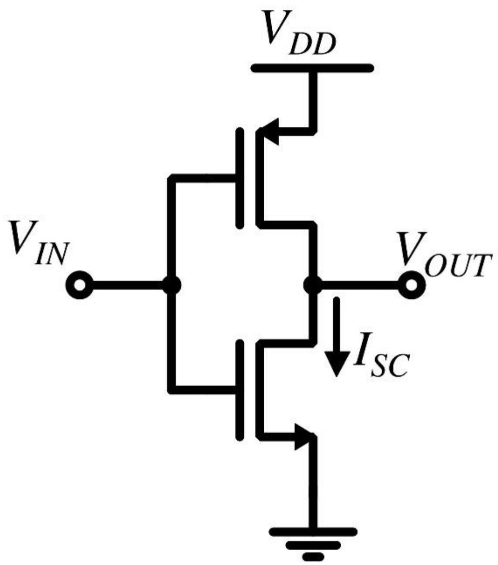
$$C_{gdo} = \frac{2}{3} W L C_{ox} \frac{\alpha^2+2\alpha}{(1+\alpha)^2} \frac{q_D - q_{Dsat}}{1 + q_D - q_{Dsat}}$$

$$\boldsymbol{C_{gd} = C_{gdo}\left(1 - \frac{\sigma}{n}\right) - C_{gso}\frac{\sigma}{n}}$$

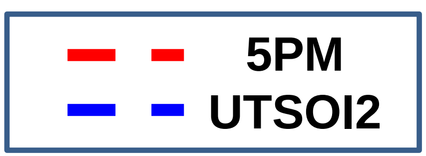
$$\boldsymbol{C_{gd} = C_{gdo} - \frac{1}{3} \frac{g_{md} L}{n v_{sat}} \frac{(1-\alpha)^2}{(1+\alpha)^2}}$$

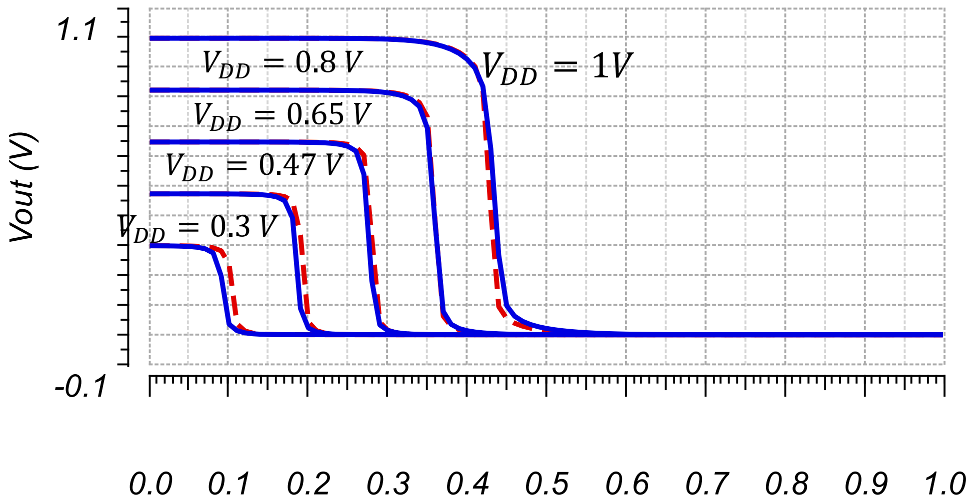
$$\boldsymbol{\alpha = \frac{1 + q_D - q_{Dsat}\frac{i_d}{i_{dsat}}}{1 + q_S - q_{Dsat}\frac{i_d}{i_{dsat}}}}$$

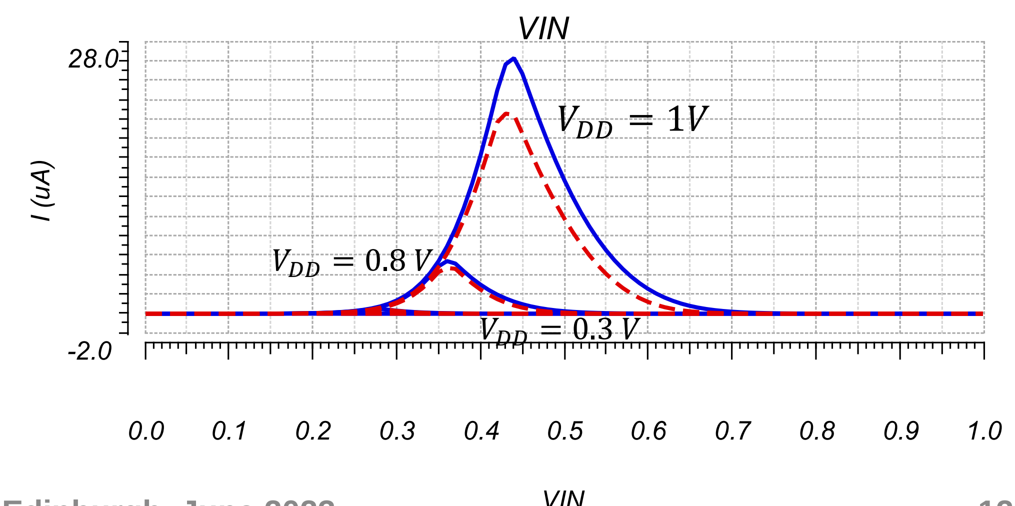
CMOS Inverter VTC and short-circuit current in 28 nm FD-SOI



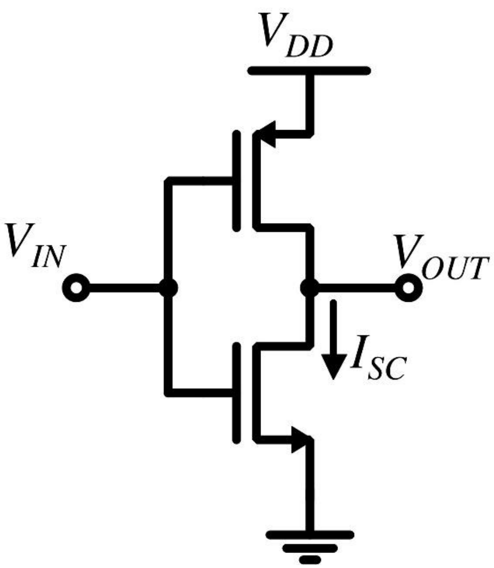
$$W_n = W_p = 1\ \mu m$$
$$L_n = L_p = 60\ nm$$

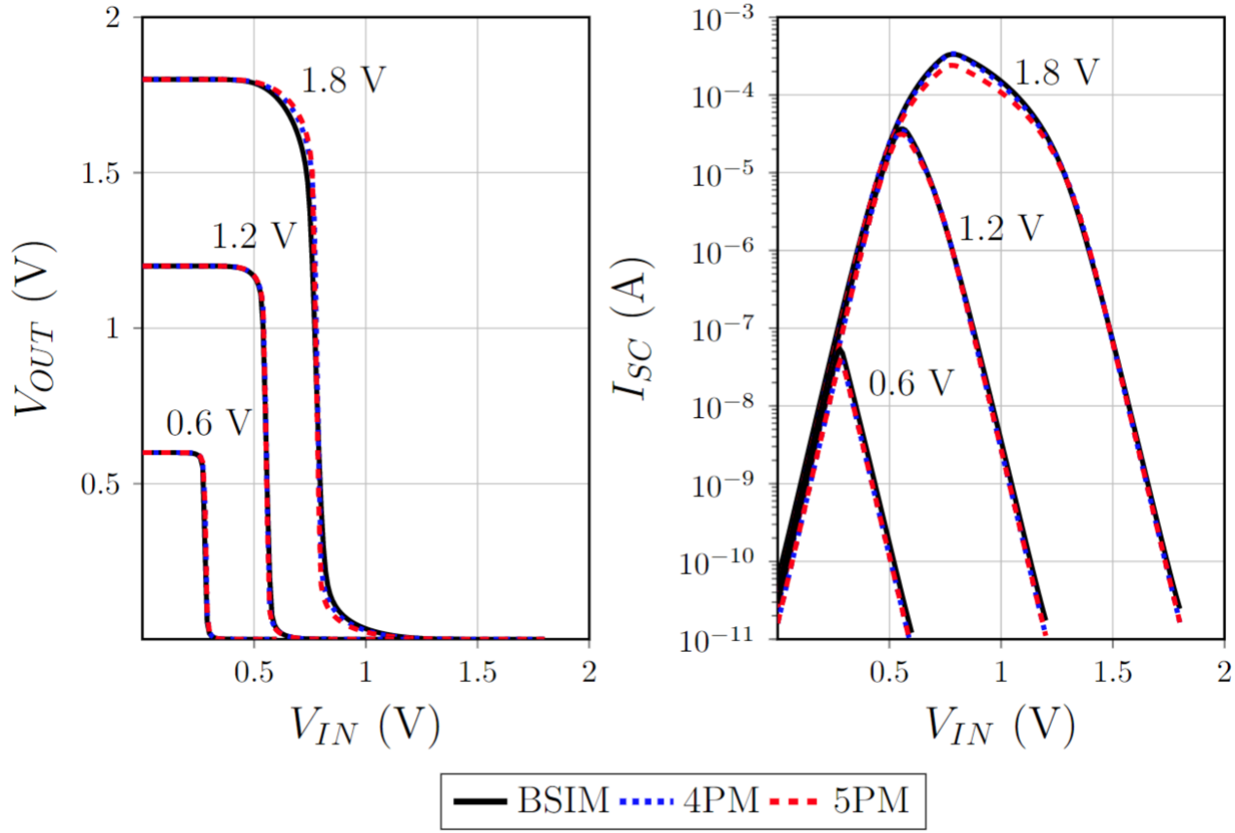






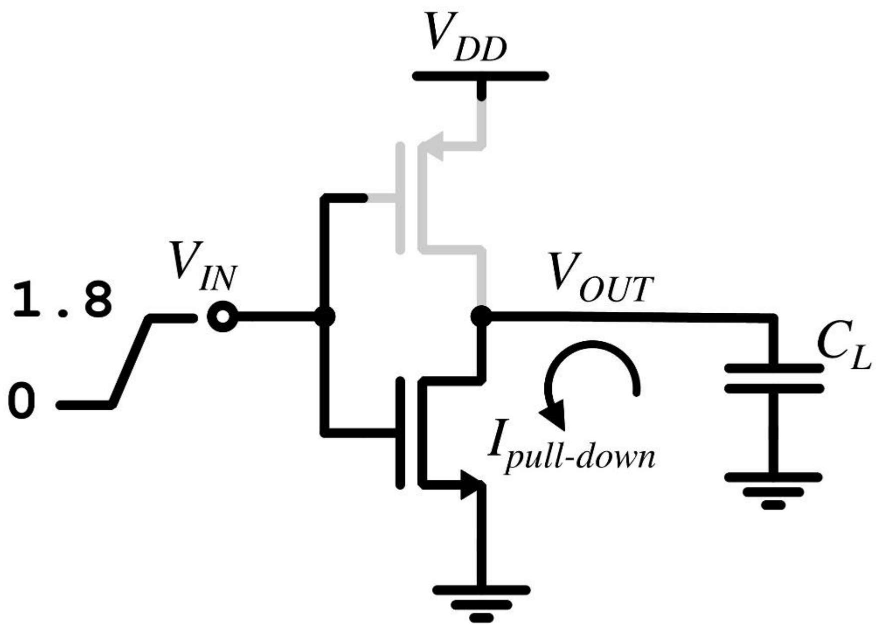
CMOS Inverter in 180 nm bulk
VTC and short-circuit current

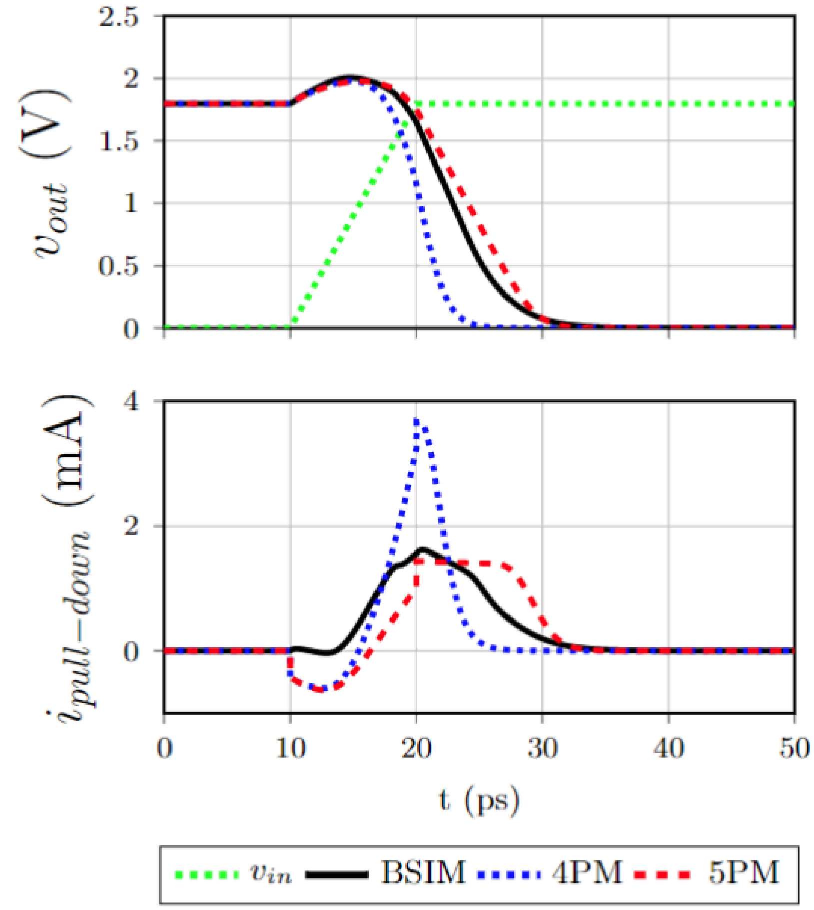




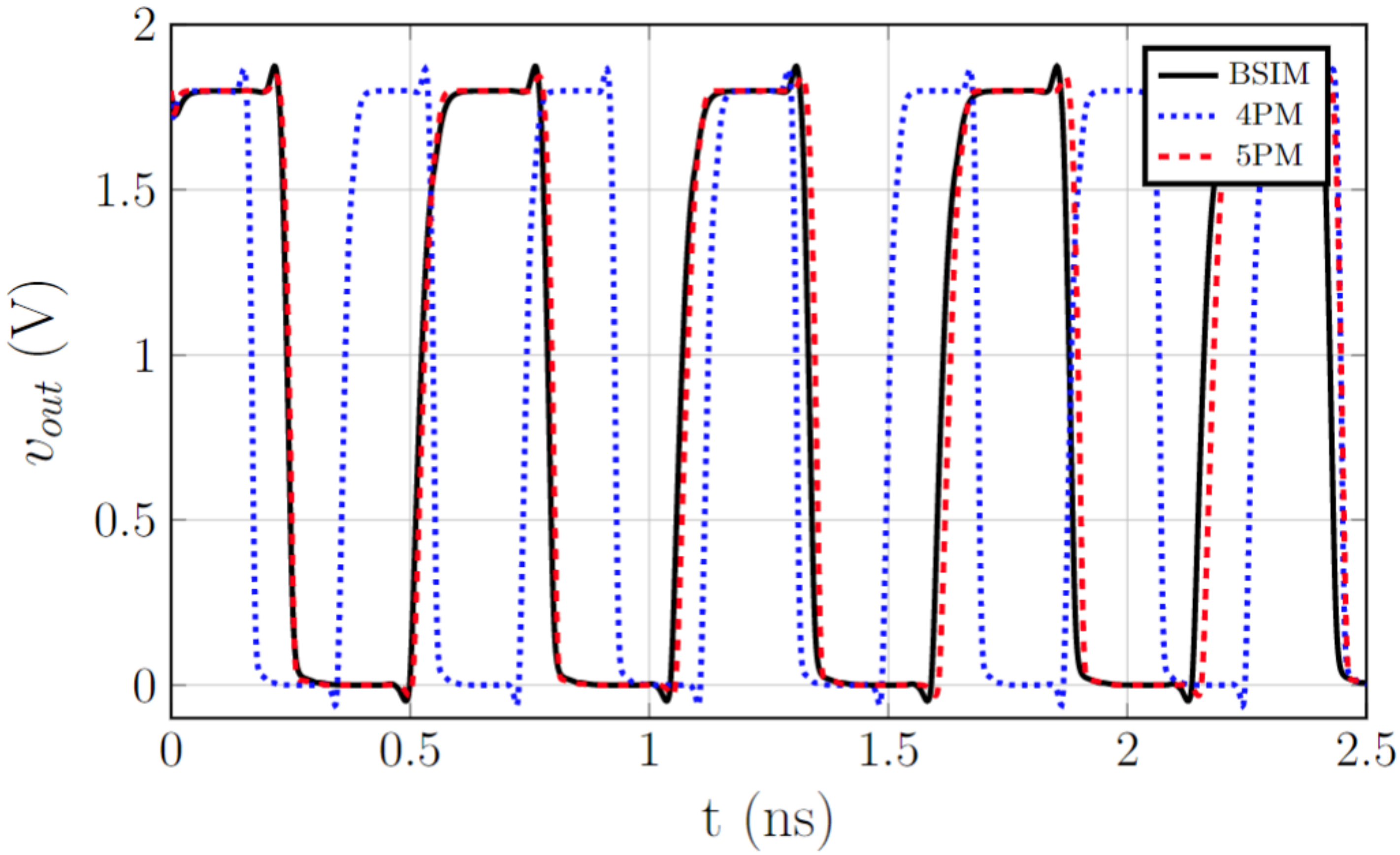
Transistor	W/L $(\mu m/\mu m)$	V_{T0} (mV)	I_S (μA)	n	σ	ζ
NMOS	5/0.18	528	5.52	1.37	0.027	0.056
PMOS	5/0.18	-525	1.82	1.40	0.024	0.035

CMOS Inverter in 180 nm bulk
Output Voltage and pull-down current





11- stage Ring Oscillator in 180 nm bulk
Output Voltage



Conclusion

- For the first time, a truly compact MOSFET model for SPICE formulated with single-piece functions

- With only 5 DC parameters that are extracted from simple and direct methods (automatized) using SPICE

- Good matching with circuit simulations with BSIM and UTSOI2 models

Main References

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- C. M. Adornes, D. G. Alves Neto, M. C. Schneider and C. Galup-Montoro, " Bridging the gap between design and simulation of low-voltage CMOS circuits ," Journal of Low Power Electronics and Applications, vol. 12, issue 2, June 2022.

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