A design-oriented single-piece short-channel MOSFET model

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***Abstract*—In this article we focus on the understanding of the MOSFET behavior allowed by the ACM2.0 model proposed last year. We discuss the concept of inversion level and its relationship with the carrier density taking velocity saturation into account. The extraction of the five DC parameters of the model based on circuit simulations is briefly developed, accounting for second-order effects. Finally, simple expressions for the drain current, the gate transconductance as well as the third-order derivative of the current with respect to the gate voltage, including the velocity saturation phenomenon, are provided.**

***Index Terms*—ACM Model, MOSFET compact model, Design-oriented model, MOSFET, parameter extraction**

I. Introduction

The first charge-controlled model for MOS transistors was proposed by Maher and Mead in 1987 [1]. Since then, several research groups have proposed different charge-based MOSFET models [2]–[11]. In this paper we focus on the ACM2.0 model proposed last year [12], [13], which has striking similarities with the Gummel-Poon [14] core equations, the use of only five DC electrical parameters being one of them. The great advantage of the single-piece equation DC model of the ACM2.0 is its usefulness not only for simulation, but also for properly sizing transistors in the pre-simulation phase of a design flow. Furthermore, jointly with the open-source PDKs and tools, simple and accurate compact models in open-source simulators also help the entrance of new engineers in the integrated circuit design domain [15].

Section II recalls the fundamentals of the ACM model while Sections III and IV discuss the carrier charge profile along the channel and its relationship with the inversion level. Section V briefly presents the parameter extraction based on specific circuit simulations. Finally, in Section VI some simplified expressions for the transconductance and its derivatives are compared with more exact ones.

II. Fundamentals

The fundamental approximation of the ACM model is the linear dependence of the inversion charge density Q_I on the surface potential ϕ_s, for constant gate voltage [1], [5], $i.e.$

$$dQ_I = nC_{OX}d\phi_s \tag{1}$$

In (1), C_{OX} is the oxide capacitance per unit area and n is the slope factor. The drain current, calculated using the charge-sheet model [16], [17], with both drift and diffusion currents, is

$$I_D = \mu W\left(-Q_I\frac{d\phi_s}{dy} + \phi_t\frac{dQ_I}{dy}\right) \tag{2}$$

where μ is the carrier mobility, ϕ_t is the thermal voltage, W is the channel width, and y is the coordinate along the channel length. The effect of carrier velocity saturation, included in the mobility model as in [1], [6]. is

$$\mu = \frac{\mu_s}{1+\frac{\mu_s}{v_{sat}}\frac{d\phi_s}{dy}} \tag{3}$$

where v_{sat} is the saturation velocity and μ_s the carrier mobility of a long-channel device. From (1), (2) and (3) the relationship between the differential of channel length and the differential of the inversion charge is

$$dy = -\frac{\mu_s W}{nC_{OX}I_D}\left(Q_I - nC_{OX}\phi_t + \frac{I_D}{Wv_{sat}}\right)dQ_I \tag{4}$$

Since n and I_D are constant along the channel, we can define a virtual charge density Q_V that differs from the real charge by a constant term, $i.e.$

$$Q_V = Q_I - nC_{OX}\phi_t + \frac{I_D}{Wv_{sat}} \tag{5}$$

Rewriting (4) in terms of the virtual charge (5) yields

$$dy = -\frac{\mu_s W}{nC_{OX}I_D}Q_V dQ_V \tag{6}$$

For convenience, in what follows, the charge densities are normalized to the thermal charge $-nC_{OX}\phi_t$ and the current is normalized to the specific current I_S, given by

$$I_S = \frac{W}{L}\mu_s nC_{OX}\frac{\phi_t^2}{2} \tag{7}$$

where L is the transistor channel length.

Thus, we rewrite (5) in terms of the normalized variables q_v and i_d as

$$q_v = q + 1 - \zeta\frac{i_d}{2} \tag{8}$$

where ζ, the short-channel parameter, defined as the ratio of a diffusion-related velocity to the saturation velocity, is

$$\zeta = \frac{\mu_s\phi_t}{Lv_{sat}} \tag{9}$$

while (6) is rewritten as

$$\frac{dy}{L} = -\frac{2}{i_d} q_v dq_v \tag{10}$$

Integrating (10) between source and drain, we obtain the expression of the drain current in terms of the normalized virtual charges at source and drain, considering drift, diffusion and velocity saturation

$$i_d = q_{vs}^2 - q_{vd}^2 \tag{11}$$

Expression (11) is instrumental in understanding the effect of the velocity saturation on the MOSFET operation, as will be shown in the next section.

Finally, the complete set of five DC equations of ACM2.0 model [13] are shown in Table I, where the symbols have their conventional meanings.

TABLE I
THE FIVE DC EQUATIONS OF THE ACM MODEL.

Charge-based expression	
$V_P = \frac{V_{GB} - V_{T0} + \sigma V_{DB} + \sigma V_{SB}}{n}$	(12)
$\frac{V_P - V_{SB}}{\phi_t} = q_s - 1 + \ln q_s$	(13)
$q_s = \sqrt{1 + \frac{2}{\zeta} q_{dsat}} - 1 + q_{dsat}$	(14)
$\frac{V_{DS}}{\phi_t} = q_s - q_d + \ln\left(\frac{q_s - q_{dsat}}{q_d - q_{dsat}}\right)$	(15)
$i_d = \frac{(q_s + q_d + 2)}{1 + \zeta \lvert q_s - q_d \rvert} (q_s - q_d)$	(16)

III. CARRIER CHARGE PROFILE ALONG THE CHANNEL

Integrating (10) between source terminal (y = 0) and an arbitrary point y of the channel, along with (11), gives

$$q_v^2 = \left(1 - \frac{y}{L}\right) q_{vs}^2 + \frac{y}{L} q_{vd}^2 \tag{17}$$

which, after writing the virtual charges in terms of the real charges, gives

$$\left(q + 1 - \zeta\frac{i_d}{2}\right)^2 = \left(1 - \frac{y}{L}\right)\left(q_s + 1 - \zeta\frac{i_d}{2}\right)^2 + \frac{y}{L}\left(q_d + 1 - \zeta\frac{i_d}{2}\right)^2 \tag{18}$$

where q is the normalized carrier density at coordinate y.

For a long-channel transistor in weak inversion, (18) simplifies to the well-known linear variation [7] of the carrier charge density along the channel in (19).

$$q = \left(1 - \frac{y}{L}\right) q_s + \frac{y}{L} q_d \tag{19}$$

Figure 1 shows plots of equation (18) of the carrier charge density profile along the transistor channel, normalized to the source charge density, for ζ= 0.1, with $V_{DS} \to \infty$, while Fig. 2 represents the channel potential along the channel, calculated using the ACM2.0 model..

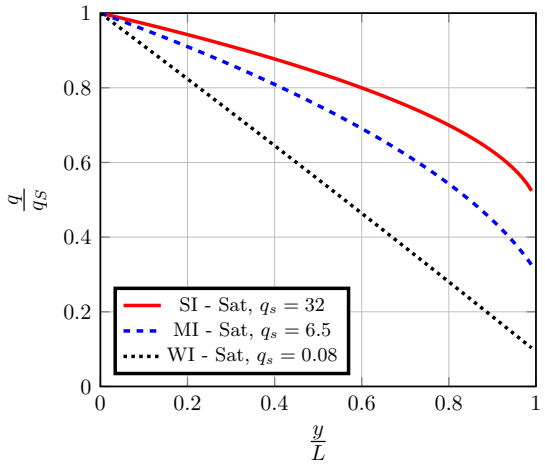

Fig. 1. Normalized carrier charge density along the channel for $\zeta = 0.1$.

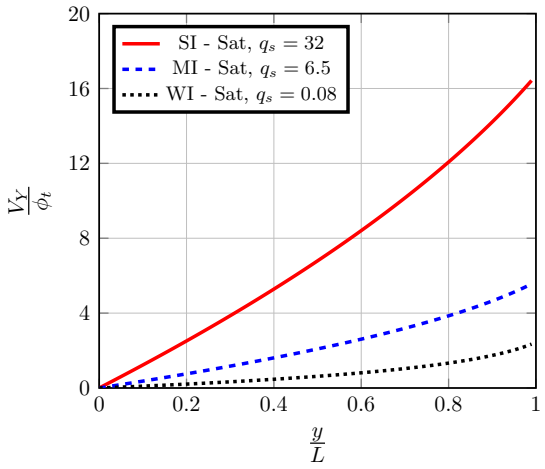

Fig. 2. Normalized potential profile along the channel for $\zeta = 0.1$.

IV. INVERSION-LEVEL-BASED DESIGN

For long-channel devices, as is the case for the V_T extractor circuit of Section V, the channel potential profile is easily determined using the inversion level concept, as explained next.

For ζ = 0, equation (11) can be rewritten as

$$i_d = i_f - i_r \tag{20}$$

where the normalized inversion levels $i_{f(r)}$ are defined in terms of the normalized carrier charge densities as

$$i_{f(r)} = \left(q_{s(d)} + 1\right)^2 - 1 \tag{21}$$

or, inversely as

$$q_{s(d)} = \sqrt{1 + i_{f(r)}} - 1 \tag{22}$$

Using (22) to write the inversion charge in terms of the inversion level in (10) we obtain, for $\zeta = 0$,

$$\frac{dy}{L} = -\frac{di}{i_d} \tag{23}$$

Clearly, from (23), the inversion level varies linearly across the channel as

$$i = \left(1 - \frac{y}{L}\right) i_f + \frac{y}{L} i_r \tag{24}$$

Before moving to the next section, we will explore a characteristic of the self-cascode MOSFET (SCM) that is employed to extract the threshold voltage V_T and the specific current I_S. The inversion coefficient i of the self-cascode transistor of Fig. 3a can be determined using its equivalent single transistor in Fig. 3b. Expression (24) gives, for $i_r = 0$, the inversion coefficient i at position y in the channel, in terms of the inversion level at the source as

$$i_f = \alpha i \tag{25}$$

where $\alpha = \frac{L}{L-y}$

Combining (22), (25) and (15) with $q_{dsat} = 0$ yields

$$\frac{V_Y}{\phi_t} = \sqrt{1 + i_f} - \sqrt{1 + \frac{i_f}{\alpha}} + \ln\left(\frac{\sqrt{1 + i_f} - 1}{\sqrt{1 + \frac{i_f}{\alpha}} - 1}\right) \tag{26}$$

In weak inversion ($i_f << 1$), (26) reduces to

$$\frac{V_Y}{\phi_t} = \ln \alpha \tag{27}$$

Thus, V_Y is proportional to the absolute temperature with a slope dependent only on a geometric ratio.

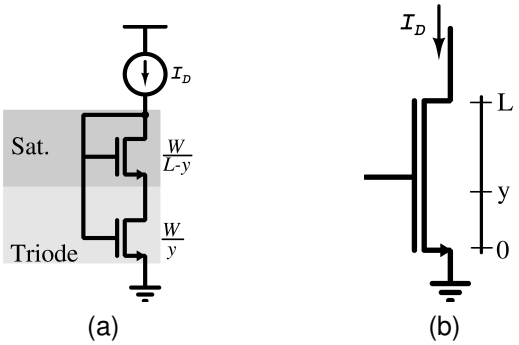

Fig. 3. (a) Self-cascode MOSFET or taped transistor [18] and (b) its representation as a single transistor with width and length equal to W and L, respectively.

V. Parameter Extraction Based on Circuit Simulation

A. Long-channel I_S and V_T extraction

In the self-biased current source (SBCS) of Fig. 4 [19]- [20] the two SCMs operate at the same current. The operational amplifier forces the intermediate voltages V_X and V_Y to be the same. If the self-cascode M_1-M_2 operates in weak inversion, it follows that

$$\ln \alpha_1 = \sqrt{1 + i_{f3}} - \sqrt{1 + \frac{i_{f3}}{\alpha_3}} + \ln\left(\frac{\sqrt{1 + i_{f3}} - 1}{\sqrt{1 + \frac{i_{f3}}{\alpha_3}} - 1}\right) \tag{28}$$

where $\alpha_1 = 1 + \frac{S_2}{S_1}$ and $\alpha_3 = 1 + \frac{S_4}{S_3}$ are geometric factors of the SCMs and $S = \frac{W}{L}$ is the transistor aspect ratio.

Thus, i_{f3} (the inversion level at the source of M_3) depends only on the geometrical factors α_1 and α_3; consequently, i_{f3} is independent of both the temperature and the technological parameters. The output current $I_{out} = I_{S3,4} i_{f3}$ is proportional to the specific current of M_4. The term $I_{S3,4}$ is the combination of the specific currents of M_3 and M_4. For simplicity, if M_3 is identical to M_4, $I_{S3,4} = \frac{I_{S3}}{2}$. Thus, the SBCS is a specific current extractor. If i_{f3} = 3, the gate-to-substrate voltage of M_3 equals V_T; thus, the circuit in Fig. 4 also operates as a threshold voltage extractor. However, under low inversion coefficients, the sensitivity of the current of the SBCS to the drain voltage of saturated transistors can be relatively high [21]. To reduce the sensitivity of the SBCS we designed a circuit for having i_{f3} = 81 and added the branch M_5-M_6 biased by the same current as in the core circuit. The SCM M_5-M_6 is a 27 times scaled replica of M_3-M_4. Such an arrangement allows obtaining i_{f5} = 3; thus, the gate voltage of M_5 equals the threshold voltage.

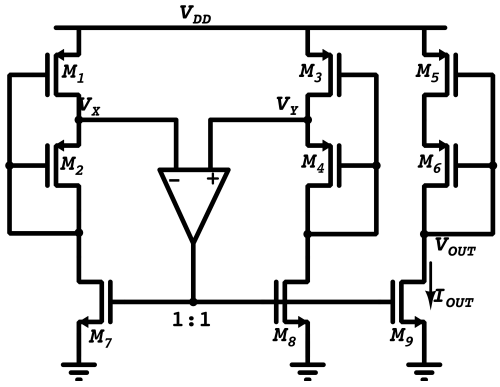

Fig. 4. Self-biased current source composed of two SCMs and an operational amplifier. A scaled replica (M_5-M_6) of SCM M_3-M_4 is included for the extraction of V_T.

B. Slope factor and short-channel parameters extraction

As shown in [10], the DIBL parameter σ can be determined as the inverse of the voltage gain of the common source topology. In an analogous way, the slope factor n is the inverse

of the voltage gain of the source follower. The saturation velocity parameter ζ can be calculated as in [12].

Fig. 5 compares the BSIM 4.5 with the ACM2.0 DC transfer characteristics of a minimum channel length pMOS.

The p-channel MOSFET used in Fig. 5 has the following parameters: $V_{T0} = -525$ mV, I_S= 1.82 μA, n = 1.40, σ = 0.024 and $\zeta = 0.035$.

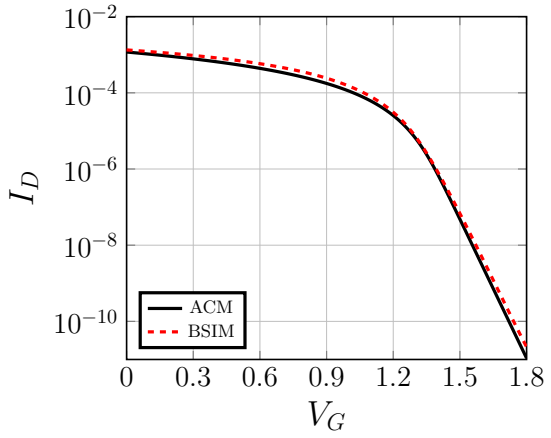

Fig. 5. DC characteristic I_D vs V_G for V_B = 1.8 V and V_{SD} = 1.8 V of a p-channel MOSFET with W/L = 5 μm /180 nm from a 180-nm technology.

VI. DESIGN-ORIENTED SMALL-SIGNAL PARAMETERS

When the electrons at the drain end of the channel reach the saturation velocity, the drain current is expressed as [16]

$$I_{Dsat} = -W v_{sat} Q_{IDsat} = \frac{2I_S}{\zeta} q_{dsat} \tag{29}$$

From (29) and (14) we get the transconductance in saturation

$$\begin{aligned} g_{msat} &= \frac{\partial I_{Dsat}}{\partial V_G} \\ &= \frac{2I_S}{n\phi_t} \frac{\sqrt{1+i_{dsat}}}{1+\zeta\sqrt{1+i_{dsat}}} \frac{\sqrt{1+i_{dsat}} - 1 + \frac{\zeta i_{dsat}}{2}}{\sqrt{1+i_{dsat}} + \frac{\zeta i_{dsat}}{2}} \end{aligned} \tag{30}$$

In most cases (30) can be approximated by

$$g_{msat} \approx \frac{2I_S}{n\phi_t} \frac{\sqrt{1+i_{dsat}} - 1}{1+\zeta\sqrt{i_{dsat}}} \tag{31}$$

if $i_{dsat} \to \infty$ then $g_m \to \frac{2I_S}{n\phi_t\zeta} = WC_{ox}v_{sat}$

Fig 6 shows the good matching between (30) and (31).

A minor correction of equation (5) in [22] gives

$$\frac{q_{dsat}}{q_s} \cong \frac{\zeta q_s + 2\zeta}{\zeta q_s + 2(1+\zeta)} \tag{32}$$

$$i_{dsat} = \frac{2}{\zeta} q_{dsat} \cong \frac{q_s^2 + 2q_s}{1 + \zeta\left(\frac{q_s}{2} + 1\right)} \tag{33}$$

Taking the third derivative of (33) and multiplying by I_S yields

$$g_{msat3} = \frac{16I_S}{(n\phi_t)^3} \frac{q_s}{(q_s+1)^3} \frac{2 - 2\zeta q_s - 3\zeta q_s^2}{(q_s+1)^4} \tag{34}$$

The unexpected accuracy of (34), particularly for the location of the so-called 'sweet spot', is shown in Fig. 7.

The n-channel MOSFET used in Figs. 6 and 7 has the following parameters: V_{T0} = 528 mV, I_S= 5.52 μA, n = 1.43, $\sigma = 0.026$ and $\zeta = 0.056$.

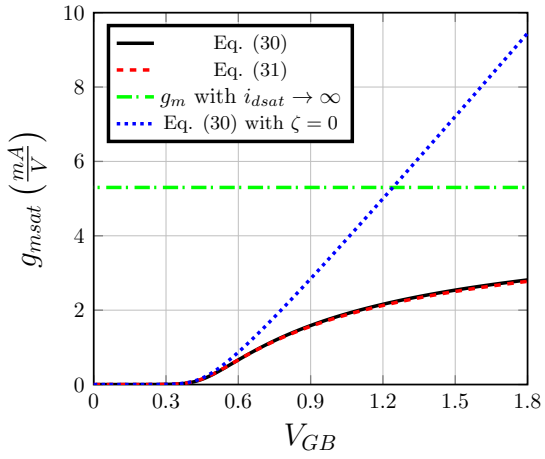

Fig. 6. g_{msat} for an n-channel MOSFET with W/L = 5 μm /180 nm from a 180-nm technology.

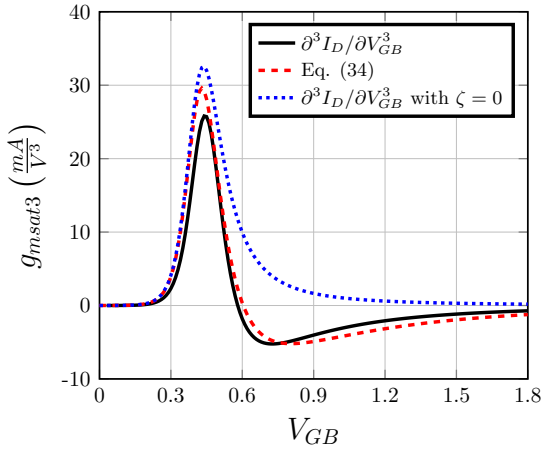

Fig. 7. g_{msat3} for an n-channel MOSFET with W/L = 5 μm /180 nm from a 180-nm technology.

VII. CONCLUSION

This paper presented several design-oriented approximations of the charge-based equations of the ACM model, useful for DC bias as well as for RF design. Additionally, a designer-friendly parameter extraction procedure based on circuit simulations was proposed.

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