A FULLY INTEGRATED 0.5 -7 Hz CMOS BANDPASS AMPLIFIER.

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ABSTRACT

In this paper, the design methodology of a fully integrated g_m-C, 0.5-7Hz band-pass amplifier is presented. The amplifier is designed to be employed in signal conditioning of a piezoelectric accelerometer, which is part of an implantable biomedical device. Transconductances of the OTAs range from 30pS to 100nS. Such low values of transconductances, which are required owing to the large time-constants involved, were obtained with the aid of a current division technique. Measurement results for OTA structures and part of the filter fabricated in a standard 0.8μm technology are presented.

1. INTRODUCTION

Implantable medical electronics usually requires active filters with very low cutoff frequencies. For this reason, in recent years there has been considerable research effort in the development of integrated OTAs with very small transconductance and improved linear range, and there are some examples of filters using these novel structures [1]. Several OTA topologies have been developed to achieve transconductances in the order of a few nA/V with linear range up to one volt [1-4]. The use of complex OTA architectures also increases noise, mismatch offset, and transistor area, and results in design trade-offs [1]. Simple division of the output current of a differential pair by a high ratio has been widely considered an expensive technique in terms of area. However, the use of series-parallel division of current [4-5] in an OTA allows the implementation of an area-efficient current divider.

In this paper, a fully integrated band-pass amplifier for a discrete piezoelectric accelerometer to be employed in the monitoring of human activity in adaptive pacemakers is presented. The resulting circuit is an OTA-C filter, and the transconductors ranging from 30pS to 100nS, with linear range up to 500mV, were obtained using series-parallel division of current. Due to its simplicity, the technique was demonstrated to be an excellent trade-off solution in terms of area, noise, mismatch offset, and current consumption. Another objective of the paper is to set a design methodology for g_m-C filters for ultra-low power, low frequency applications. Firstly, the filter topology and design methodology are presented. The OTA structures are then examined in detail and measurement results on isolated OTAs are presented. Finally, a brief noise analysis of the filter as well as some measurements of noise and transfer function of the filter input stage are shown.

2. FILTER TOPOLOGY AND DESIGN METODOLOGY

The filter topology is shown in Fig.1. It has two cascaded stages with a total gain A=410: a preamplifier stage with gain A_1=49 formed by G_{m1}, G_{m2}, G_{m3}, C_1, C_2, and a gain stage with gain A_2=8.4 formed by G_{m4}, G_{m5}, G_{m6}, C_3, C_4. Each stage has a low-pass structure (given by $G_{m1(4)}$, $G_{m2(5)}$, $C_{2(4)}$) similar to that proposed in [2], and a DC cancellation loop ($G_{m3(6)}$, $C_{1(3)}$). The external piezoelectric sensor is modeled as a capacitor (550pF) with an input voltage in series. Note in Fig.1 that the sensor capacitance itself is used in the filter.

Figure 1: Filter topology.

Figure 2. Topology for the transconductors G_{m6}, using series-parallel current division, and a linearized input differential pair.

The minimum signal to be processed is $25\mu V_{pp}$ and the maximum differential signal is $1.5mV_{pp}$ at the input, with an offset of up to $\pm 5mV$ due to gravity. The key specifications of this circuit are: low-noise, current consumption $<1\mu A$, and large time-constants. Once the filter architecture of Fig.1, area and current budgets are selected, the steps in the design methodology are:

(a) Assign enough area to the capacitors to relax requirements on the OTAs, and assign an area budget to the OTAs.

(b) Noise is critical and probably, mostly determined by G_{m1}; so, select G_{m1} transconductance to minimize noise [6], according to the area and current consumption budget. G_{m1} is a standard OTA.

(c) The closed loop gain of the preamplifier stage is approximately proportional to $1/G_{m3}$ so determine the minimum possible transconductance to G_{m3} (this is discussed in 3.2) and assign enough gain to the preamplifier to reduce noise.

(d) With (a), (b), (c), G_{m1}, G_{m3}, C_1, C_2, are determined. The remaining OTAs are designed to achieve the required transfer function (see Table 1).

	Transc.	V_{Lin} [mV]	Noise [μV_{RMS}]	Area [mm^2]	Current [nA]	Offset [mV]
G_{m1}	110nS	60	5 (4)	.019	28	<2.5
G_{m2}	2.58nS	150	42	.040	44	<8.5
G_{m3}	33pS	150	163(130)	.092	42	<2.5
G_{m4}	21nS**	150**	*	.051	48	*
G_{m5}	2.8nS	500	*	.18	44	<21
G_{m6}	100pS	500	*		42	<11

Table 1. Measured transconductance , linear range V_{Lin} (error $\alpha<5\%$), estimated (measured) input referred noise in the passband, total area, current consumption, and measured offset for the OTAs. (*) Due to circuit topology some measurements could not be obtained. (**) Estimated.

(e) To complete the specifications on the OTAs, their required input linear range V_{Lin} is determined for the maximum specified signal at the input. The linear range is defined [5] as the maximum input that results in an output current with an error $<\alpha$ with respect to the ideal linear output. The selected α for the design was 5%, which is considered an acceptable error for human motion determination. For the same reason, no tuning was employed in the filter because a slight shift in cutoff frequencies or gain does not affect the result once the device is calibrated for a patient.

3. CMOS OTAS WITH VERY LOW TRANSCONDUCTANCE AND EXTENDED LINEAR RANGE

Apart from G_{m1}, the rest of the transconductors are implemented using series-parallel current division [4-5] with the design procedure described in [5]. In Fig.2, the architecture for G_{m6} is shown, it is a symmetrical OTA with a linearized input pair [7], and a current division factor $N^2 = 784$. The effective transconductance is calculated as

$$G_{mX} = g_{m1}/N^2 \qquad (1)$$

where g_{m1} is the transconductance of the degenerate input pair. The sizes of M_2 and M_3 influence leakage currents, matching, and noise, and by using a high division factor N^2 it is possible to obtain transconductances in the order of pico-A/V. The number of parallel/stacked transistors is limited by leakage currents only. Since their required linear range is smaller, G_{m2}, G_{m3}, G_{m4} are implemented with nondegenerated differential input pair. Since the required division factor for G_{m4}, G_{m5} is not too large, transistor M_2" is composed of a rectangular array of unitary transistors. For example, the gain of the current mirror M2": M2'in G_{m4} is 1:8, the gain is obtained with M2'as an array of 28

unitary transistors in parallel while, M2"is composed of a 7-parallel-by-2-series array of unitary transistors. M2" is equivalent to a 3 ½ parallel array of unit transistors [12]. These numbers were chosen in order to reuse other layout blocks of the circuit.

3.1 What is the minimum effective G_m possible with this technique?

The output branch in Fig.2 is biased with a current in the order of a few pA. Operation at such low currents is still reliable when using long channel transistors (as M_2") [8]. Transistor size was demonstrated not to be a limitation [4-5]. Thus the only limitation is the sum of the leakage currents at the source (drain) of each series transistor in M_2". Leakage current should be much less than bias current not only to allow appropriate transistor operation, but also to reduce the offset due to leakage mismatch. For hand calculations, leakage mismatch was estimated as 25% [9]. For the selected technology, the leakage was estimated as $\sum I_{leak} = 0.3$pA with N=100 series transistors. The design criterion is

$$\sum I_{leak} < \frac{I_{Bias}}{10N^2} \qquad (2)$$

(I_{Bias} is the bias current of the differential input pair), which imposes a limit on the minimum achievable G_{mX} according to (1). Using a nondegenerate differential input pair, a worst case estimate for the minimum G_{mX} according to (2) is 10pS, equivalent to a 100GΩ resistor.

3.2 Noise calculation

In this design, noise analysis is critical; thus reliable tools to determine it, while preserving the properties of series-parallel association of transistors (particularly for flicker noise due to the low frequencies involved) are required. A first calculation is performed with the approximate noise equations for a single transistor presented in [6] considering that N>>1 and that M_2' and M_3 operate in weak inversion. The result for the input referred thermal noise is:

$$v_{n\_w}^2(f) \approx \frac{4nk_BT}{G_{m2}}\beta \qquad (3)$$

where i_{f1} is the inversion level of the input pair transistors [10] and $\beta = \left(\sqrt{1+i_{f1}}+1\right)$. For the flicker noise:

$$v_{1/f}^2(f) = \frac{2q^2}{C_{OX}'^2}\left[\frac{N_{otP}}{(WL)_1} + \beta^2\left(\frac{2N_{otP}}{N(WL)_2} + \frac{N_{otN}}{(WL)_3}\right)\right]\frac{1}{f} \qquad (4)$$

In (3), (4) C'_{OX}, q, $(WL)_X$, k_B, T, are, respectively, the oxide capacitance per unit area, electron charge, gate area for each transistor, Boltzman's constant, and absolute temperature. n is the slope factor, slightly dependent on the
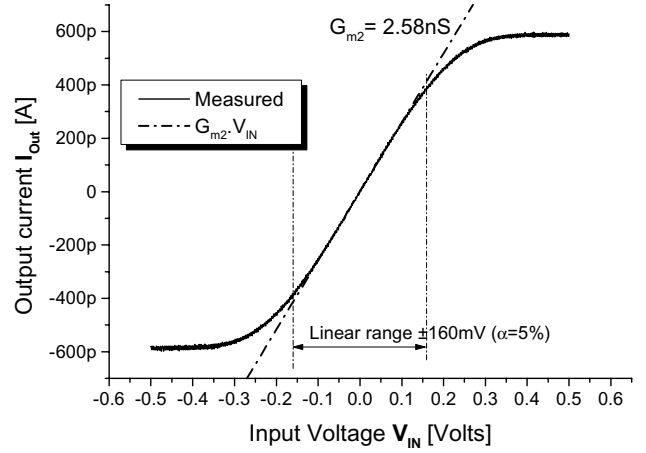

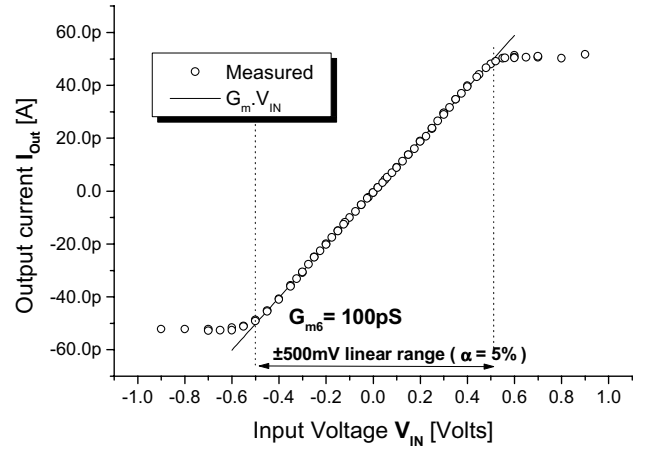**Figure 3**. Measured transfer characteristic of G_{m2}.

Figure 4. Measured transfer characteristic of G_{m6}.

gate voltage [10]. $N_{otN(P)}$ [6,11] are the effective traps densities per unit area for both N-MOS and P-MOS transistors. The results from (3) and (4) are verified later with the physical model presented in [11], which preserves the properties of series-parallel association of transistors. Note that the expressions in (3) and (4), are very similar to those of a classical OTA[6], but the price to pay for extending the OTA linear range is a corresponding increase in noise due to the factor β. In effect, the input pair must be biased in strong inversion to increase the linear range, but unfortunately it does so along with the noise. The analysis of (3), (4) can be extended with similar results to a linearized pair structure as in Fig.2.

3.3 Transconductor implementation and measurements

For test purpose, single OTA structures were fabricated. In Table 1, a comparison of the transconductors is shown. According to other reported studies [1-4,7] OTAs with series-parallel current division present a very good trade-

off between area, noise, current consumption, and offset. In Figs.3 and 4 the measured transfer functions of G_{m2} and G_{m6}, are shown along with their linear range.

4. PREAMPLIFIER NOISE ANALYSIS AND MEASUREMENT RESULTS

The preamplifier stage is critical in terms of noise. In Fig.5 the result of a noise analysis that represents the noise contribution at the output of each G_m is shown. In the passband , from 0.5 to 7Hz, the noise is dominated by G_{m1} as expected. The measured equivalent noise voltage at the input was $6\mu V_{RMS}$. Fig.6 gives the measured transfer function of the preamplifier. The preamplifier occupies an area of $0.29mm^2$ (C_I-$0.03mm^2$, OTA areas are given in Table 1), operates up to 2V, and consumes 120nA only.

5. CONCLUSIONS

The complete design methodology for a fully integrated g_m-C, 0.5-7Hz, CMOS bandpass amplifier has been presented. Large time-constants are obtained using series-parallel division of current in symmetrical OTAs to achieve low transconductances and extended linear range. This technique has been studied in detail; the measured and predicted performance of the OTAs resulted in a very good trade-off in terms of current consumption, linearity, noise, and mismatch offset. The design methodology for this filter can be easily extended to other micropower filters with low cutoff frequencies commonly employed in implantable medical electronics.

6. ACKNOWLEDGEMENT

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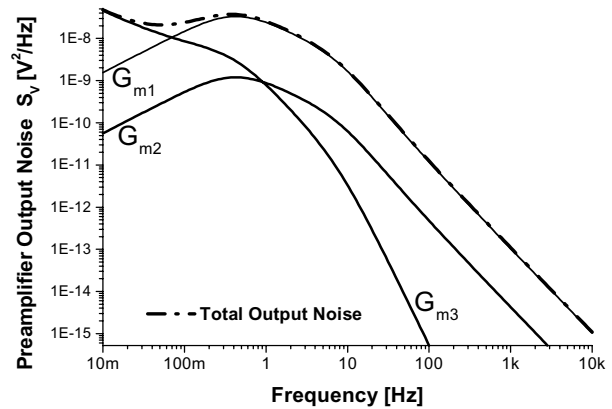

Figure 5. Estimated noise contribution of each OTA to the total output noise of the preamplifier stage.
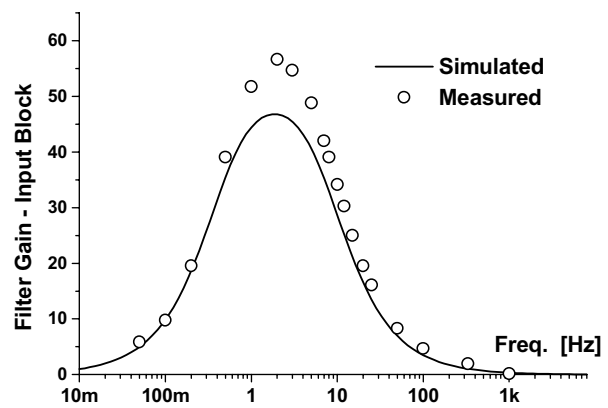

Figure 6. Measured preamplifier transference.

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