Transconductance-Based CMOS Analog Multiplier

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***Abstract*— In this paper we propose a four-quadrant multiplier based on a core cell that exploits the relationship between the saturation current of an MOS transistor and the source transconductance. The advantages of the proposed topology are simplicity and feasibility of low-power and low-voltage operation. Experimental results in a 0.35 μm CMOS prototype indicate 1 mA consumption for 1MHz bandwidth, and distortion level below 1% for an input current equal to 80% of the full scale range. The multiplier area is around 10,000 μm^2.**

I. INTRODUCTION

Analog multipliers are important subcircuits that find applications in filtering, neural networks, electronic instrumentation, and modulators, among others. Multipliers make use of nonlinear characteristics of transistors to generate an output signal equal to the product of two input signals. A good survey on MOS multipliers is presented in [1]. Several other more recent papers such as [2], [3], [4] have also published CMOS circuits for the implementation of analog multiplication.

In this work we propose an analog multiplier that makes use of the relationship between the saturation current and the source transconductance of a MOSFET as in reference [5]. The core cell of the multiplier, as in [5], is a "squarer" circuit that provides an output current proportional to the square of the input current. However, the core cell that we propose here is considerably simpler than the one used in the four-quadrant current-mode CMOS multiplier of [5]. The benefits of a simpler topology translate into lower power consumption, lower voltage operation, simpler design equations and less silicon area. As in [5], we make use of ACM (Advanced Compact MOSFET) model, an all-region MOSFET model [6], [7] to describe the design equations of the squarer circuit. The use of the all-region model allows deriving consistent equations for all regions and avoids the use of regional approximations that inevitably lead to a very poor modeling of harmonic distortion.

II. SQUARER CIRCUIT ARCHITECTURE

A. Model Equations

The main expressions of the ACM model used in this work are shown in Table I, where i_f (i_r) is the normalized forward (reverse) saturation current or the inversion level at the source(drain) end, ϕ_t is the thermal voltage, n is the slope factor, μ is the carrier mobility, C'_{ox} is the oxide capacitance per unit area, V_G is the gate-to-bulk voltage, $V_{S(D)}$ is the source (drain)-to-bulk voltage, γ is the body effect coefficient, ϕ_F is the Fermi level for majority carriers, V_{FB} is the flat-band voltage, V_{T0} is the threshold voltage, W is the channel width and L is the channel length.

TABLE I. EXPRESSIONS OF THE ACM MODEL

Parameter/ Characteristic	Symbol	Expression
Drain current	I_D	$I_S\,(i_f - i_r)$
Specific current	I_S	$\mu C'_{ox} n \frac{\phi_t^2}{2}\frac{W}{L}$
Pinch-off voltage	V_P	$V_P = \left(\sqrt{V_G - V_{FB} + \frac{\gamma^2}{4}} - \frac{\gamma}{2}\right)^2 - 2\phi_F \cong \frac{V_G - V_{T0}}{n}$
Source(drain)-to-bulk voltage	$\frac{V_P - V_{S(D)}}{\phi_t}$	$\sqrt{1+i_{f(r)}} - 2 + \ln\left(\sqrt{1+i_{f(r)}} - 1\right)$
Source transconductance	g_{ms}	$\frac{2I_S}{\phi_t}\left(\sqrt{1+i_f} - 1\right)$
Drain-to-source saturation voltage	V_{DSSAT}	$\phi_t\left(\sqrt{1+i_f} + 3\right)$

B. Squarer Circuit – The Forward-Current Mirror

The core cell of the multiplier (to be described in Section III) is the current "squarer" shown in Fig.1. Assuming that transistor M_1 operates in the linear region at constant drain-to-source voltage (V_Y), the inversion level at the source (i_{f1}) is a (quadratic) function of the drain current ($2I_B+I_{IN}$). Since M_1 and M_3 (the later operating in saturation) have the same gate and source voltages, $i_{f1} = i_{f3}$ and the output current $I_{OUT} = I_{S3}i_{f1}$ is a quadratic function of the current $2IB + I_{IN}$.

In the derivation that follows, we assume the transistor sets (M_B, M_2) and (M_A, M_1, M_3) to be matched. The input of the core cell, I_B+I_{IN} is a unidirectional current provided by a single p-channel transistor.

As will be shown later, the voltage at node X in the bias circuit of Fig.1 can be proportional-to-absolute temperature

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(PTAT). For the sake of convenience, we will use the notation $V_X = K\phi_t$ throughout the paper.

Assuming M_2 also in saturation, since the value of the drain currents of M_2 and M_B is the same and since their gates are connected (equal gate and pinchoff voltages), then $V_Y = V_X = K\phi_t$. Thus, the drain-to-source voltage across M_1 is independent of the current flowing through it. Let us now assume that, for low values of V_Y, M_1 behaves like a linear resistor whose resistance is controlled by the gate voltage, i.e.

$$\frac{I_{D1}}{V_{DS1}} = \frac{I_{D1}}{K\phi_t} \cong g_{ms1}. \qquad (1)$$

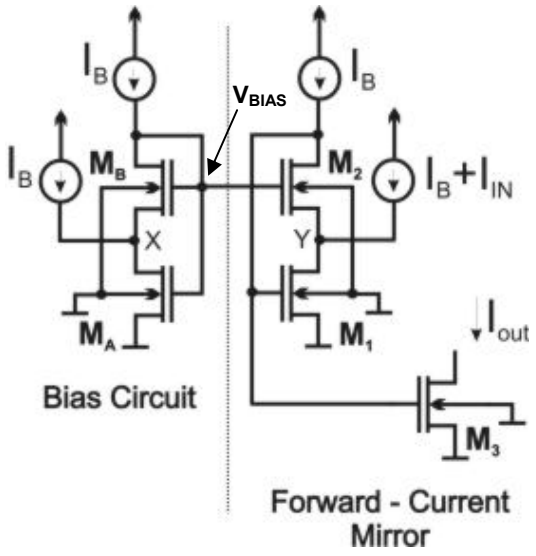

Figure 1. Core cell of the analog multiplier (squarer circuit).

In (1), g_{ms1} is the source transconductance, *i.e.*, the derivative of the drain current with respect to the drain voltage, measured for V_{DS}=0. The value of g_{ms1} is controlled by the inversion level i_{f1} at the source according to the expression in Table I. Particularly, in the circuit of Fig. 1, i_{f1} is controlled by input current I_{IN} and bias current I_B. Now, applying approximation (1) along with the expression for the source transconductance in Table I to the circuit in Fig. 1 we obtain

$$i_{f1} = \left(\frac{2I_B + I_{IN}}{2KI_{S1}}\right)^2 + \frac{2I_B + I_{IN}}{KI_{S1}}. \qquad (2)$$

The forward inversion level of transistor M_1 contains linear and quadratic terms of the input signal besides a dc level associated with the bias current.

Since transistors M_1 and M_3 share common gate, source and bulk terminals, the forward inversion levels i_{f1} and i_{f3} are equal. Assuming that M_3 operates in saturation, the output current I_{OUT} is

$$I_{OUT} = I_{S3} i_{f1} = I_{S3}\left[\left(\frac{2I_B + I_{IN}}{2KI_{S1}} + 1\right)^2 - 1\right]. \qquad (3)$$

Therefore, the output current is a replica of the forward current that flows through M_1. Due to this property, the pair M_1-M_3 can be designated as forward current mirror.

The linear approximation given by (1) is more accurate if the transistor drain-to-source voltage is much smaller than the saturation voltage, given in Table I. At a first glance, low values of V_Y seem to be a good choice for improving accuracy but, unfortunately, they make the circuit more sensitive to mismatch. Typically, one can choose V_Y in the range $V_{DSSAT}/8$ to $V_{DSSAT}/5$.

C. Squarer Circuit – The Bias Circuit

The function of the bias circuit in Fig. 1 is to provide a PTAT voltage at node X and transfer it to node Y of the forward-current mirror. The drain-to-source voltage V_X across transistor M_A is calculated using the following set of equations.

$$\frac{V_{PB} - V_X}{\phi_t} = \sqrt{1 + i_{fB}} - 2 + \ln\left(\sqrt{1 + i_{fB}} - 1\right). \qquad (4a)$$

Transistor M_B is in saturation; therefore $i_f >> i_r$, and the drain current through M_B is

$$I_B = I_{SB} i_{fB}. \qquad (4b)$$

The drain current of M_A is

$$2I_B = I_{SA}\left(i_{fA} - i_{rA}\right). \qquad (4c)$$

The inversion level at the darin of M_A is equal to the invesion level at the source of M_B, i.e., $i_{rA} = i_{fB}$.

Finally, we can write, for the source of M_A

$$V_{PA}/\phi_t = \sqrt{1 + i_{fA}} - 2 + ln\left(\sqrt{1 + i_{fA}} - 1\right). \qquad (4d)$$

Noting that $V_{PA} = V_{PB}$, since the gates of M_A and M_B are connected together, we solve for V_X using (4a) through (4d), which gives

$$V_X/\phi_t = K = \sqrt{1 + \frac{I_B}{I_{SA}}\left(2 + \frac{I_{SA}}{I_{SB}}\right)} - \sqrt{1 + \frac{I_B}{I_{SB}}} + ln\left(\sqrt{1 + \frac{I_B}{I_{SA}}\left(2 + \frac{I_{SA}}{I_{SB}}\right)} - 1\right) - ln\left(\sqrt{1 + \frac{I_B}{I_{SB}}} - 1\right) \qquad (5)$$

The factor K is, in general, a function of temperature. However, if the current source I_B is obtained through a specific current generator, *i.e*, I_B is proportional to the specific current I_S, as described in [8], [9], V_X is PTAT as stated earlier.

D. Squarer Circuit – Design Considerations

The input of the core cell I_B+I_{IN} is a unidirectional current provided by a single p-channel transistor, that is, $|I_{IN}| \le I_B$.

If M_1 operates in weak inversion $i_{f1} = 2I_B/I_{S1} + I_B/I_{S1} \le 1$, the linear term in (2) prevails over the quadratic term.

Although the linear term in (2) is eliminated by an appropriate combination of squarer circuits (Section III), the efficiency of this elimination relies on the matching of the squarer circuits. Thus, the operation of the multiplier of this paper should not be in deep weak inversion. On the other hand, in strong inversion, the contributions of the linear and quadratic terms to the forward current are of the same order of magnitude for values of I_{IN} approaching I_B.

Now, let us calculate the minimum power supply voltage to keep the transistors in the appropriate operating region for the correct response of the squarer circuit. We assume here that the current source I_B requires a minimum voltage V_{CS} between its terminals to operate properly. Therefore, the minimum supply voltage is:

$$V_{DDmin} = V_{CS} + \tilde{V_{G1max}} \qquad (6a)$$

The maximum gate voltage of M_1, V_{G1max}, results from the maximum input current, I_{INmax}, which is assumed equal to I_B. Thus, we can use the relationship between voltage and forward current given in Table I at the source of M_1, which gives

$$\frac{V_{G1\max} - V_{T0}}{n\phi_t} \cong \frac{V_{P1\max}}{\phi_t} = \sqrt{1+i_{f1\max}} - 2 + \ln\left(\sqrt{1+i_{f1\max}} - 1\right). \qquad (6b)$$

In order to compute i_{f1max}, we can use the following relationships (Table I):

$$\frac{V_Y}{\phi_t} = K = \sqrt{1+i_{f1\max}} - \sqrt{1+i_{r1\max}} + \ln\left(\frac{\sqrt{1+i_{f1\max}} - 1}{\sqrt{1+i_{r1\max}} - 1}\right), \qquad (6c)$$

$$I_{D1\max} = 3I_B = I_{S1}\left(i_{f1\max} - i_{r1\max}\right). \qquad (6d)$$

If the current source I_B is implemented by a single p-channel transistor, V_{CS} is the source-to-drain saturation voltage of this transistor. The minimum supply voltage can be reduced by reducing the inversion levels of the current sources and of the transistors of the core cell at the expense of accuracy. The core cell of our multiplier is able to operate at low supply voltages as a result of operating transistor M_1 in the linear region.

III. MULTIPLIER ARCHITECTURE

The complete configuration of the multiplier is shown in Fig.2. The bias circuit generates V_{bias}, which is the gate voltage of transistor M_2 in Fig.1, to apply to the four squarer circuits. The input signals for the multipliers are $I_X + I_Y$, $I_X - I_Y$, $-I_X + I_Y$, and $-I_X - I_Y$. The outputs of the squarer circuits are added in pairs and the resulting outputs are subtracted from each other for the cancellation of the undesirable terms. The resulting output current I_{OUT}, using (3) for each square cell in Fig.2 with $I_{S3} = I_{S1}$, is

$$I_{OUT} = I_{OUTA} + I_{OUTD} - \left(I_{OUTB} + I_{OUTC}\right) = \frac{2I_X I_Y}{K^2 I_{S1}}. \qquad (7)$$

It is important to note that, to keep the input current of all core cells unidirectional, we must have $|I_X| + |I_Y| \le I_B$.

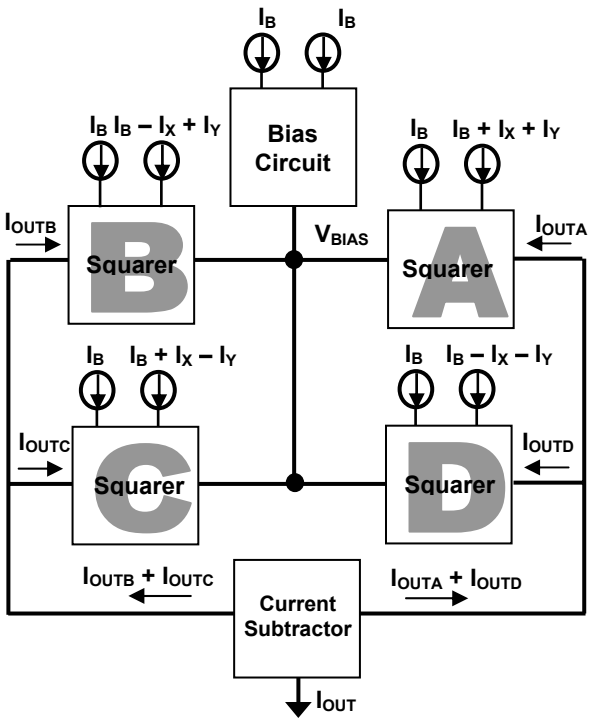

Figure 2. Block diagram of multiplier. Multiplier output is $(I_{OUTA}+I_{OUTD})-(I_{OUTB}+I_{OUTC})$.

IV. EXPERIMENTAL RESULTS

The design of the multiplier was implemented on the 0.35 μm technology of TSMC, according to which, for the n-channel transistor, $V_{T0} = 0.54$ V, $n \cong 1.3$ and $I_S/(W/L)$ is around 72 nA. In our design, I_B= 10 μA and for each core cell: $i_{fA} = i_{f1} = i_{f3} = 197$, $i_{fB} = i_{f2} = i_{f3} = 140$, $W_A = W_1 = W_3 = 19.2$ μm, $W_B = W_2 = 4$ μm and $L = 4$ μm for all five transistors.

We have chosen long-channel devices in order to reduce short-channel effects as well as to improve matching. I_{SA} = 346 nA and I_{SB} = 72 nA, thus from (5), we find that $K \cong 2.4$. The saturation voltage of M_1 $17\phi_t$, as calculated from Table I with $i_{f1} = 197$. Therefore, the drain-to-source voltage of M_1, $K\phi_t$ is around $V_{DSSAT}/7$.

Assuming $I_{INmax} = I_B$, we obtain $i_{f1max} \cong 410$, which gives, from (6b), $V_{G1max} \cong 1.25$ V. I_B is provided by a single p-channel transistor operating with inversion level equal to 100. Thus, $V_{CS} = 13\phi_t \cong 335$ mV and V_{DDmin} is around 1.6 V.

The experimental transfer characteristic of the squarer prototype as well as the simulation results obtained from SMASH [10] using BSIM 3v3.1, along with expression (3) based on the ACM model, are shown in Fig. 3. The description of the experimental results by (3) is quite good.

Fig. 4 shows the measured DC current transfer characteristics of the multiplier for constant current at input X and I_Y varying in the range ±5 μA. The linearity of the multiplier, later confirmed by measurements of harmonic distortion (Table II), is remarkably high for an input current up

to 5 μA. Fig 5 shows the simulated and experimental frequency response of the multiplier for 5 μA dc at input X and peak amplitude equal to 5 μA at input Y. The -3 dB frequency of the multiplier is about 1 MHz.

Table II summarizes the performance of the multiplier prototype.

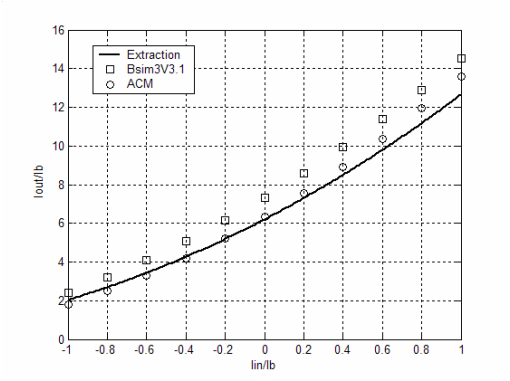

Figure 3. Transfer characteristic of the squarer: measured (solid line), simulated with BSIM 3v3.1 (squares) and calculated through (3) (circles).

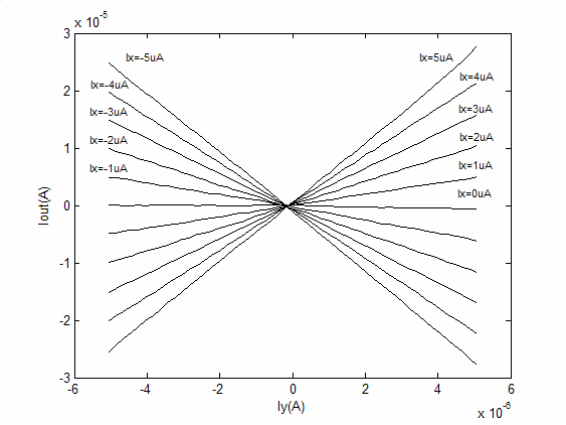

Figure 4. Experimental DC transfer characteristics of the multiplier (I_B = 10 μA).

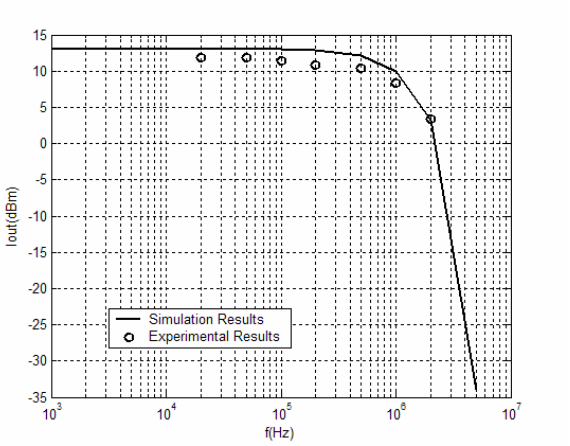

Figure 5. Simulated and experimental frequency response of the integrated multiplier for I_B= 10 μA, I_X= 5 μA (V-I input converter included).

TABLE II. PERFORMANCE OF THE MULTIPLIER PROTOTYPE

Supply voltage	3 V
Technology	0.35 μm
Current Consumption @ I_B= 10 uA **V-I converters included** **V-I converters not included**	 3 mA 1 mA
Input Current Range	10 μA
THD for Ix=5 μA @ 100 kHz **@ Iy=4.3 μA peak** **@ Iy=5 μA peak**	 1% 4%
RMS Output Noise Current (10kHz to 100kHz)	100 nA
-3 dB bandwidth	1 MHz
Multiplier area	~ 10,000 μm²

V. CONCLUSION

We presented a four-quadrant CMOS current-mode multiplier capable to operate at low voltage supplies. Its main advantages are the simplicity and feasibility of low-power and low-voltage operation. The multiplier functionality has been experimentally verified for a prototype implemented in 0.35 μm CMOS technology.

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