An *M-2M* Digital-to-Analog Converter Design Methodology Based on a Physical Mismatch Model

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***Abstract*—This paper presents a new approach for accurate M-2M MOSFET digital-to-analog converter (DAC) design. It describes a complete design methodology, where DAC inaccuracy is related to transistor geometry and bias through a powerful physics-based MOSFET mismatch model, very useful for hand design. Short-channel effects are also taken into account. Two versions of the converter were implemented in a 0.35 µm 3.3V CMOS technology, and corroborate the theoretical development with statistical experimental results.**

I. INTRODUCTION

Analog-to-digital (ADC) and digital-to-analog (DAC) converters are key blocks in mixed-signal circuits.

Any data converter requires a quantization technique to implement a binary current or voltage division; to that purpose, the R-2R ladder was the mainly used network over the 60's to the early 80's years. In 1992, Bult and Geelen proposed a linear current division technique by using MOS transistors only [1]. This principle, appropriate for application in CMOS processes, has been used to implement M-2M ladders [2], [3], which are the MOSFET-based equivalent to the resistor R-2R ladders. M-2M ladders do not consume too much silicon area. Also, they can be used for low voltage and low power applications. Since in advanced MOS processes transistor matching can be better than 0.1% [2], an effective resolution of 10-12 bits without trimming is attainable.

This paper presents a design methodology for M-2M MOS DACs that can predict the converter accuracy using a physics-based MOSFET mismatch model, also developed by the authors. Two 8-bit versions of the converter were designed, implemented in a 0.35 µm CMOS technology (Fig. 1), and fully characterized, to corroborate the theoretical development. To the best of our knowledge, this is the first successful design methodology based on mismatch data for M-2M DACs.

II. THE BINARY WEIGHTING PRINCIPLE

For a long-channel MOSFET under any bias condition, the drain current is directly proportional to the channel width (W), and inversely proportional to its length (L). Based on this statement, one can show that any series-parallel association of identical transistors (Fig. 2) works similarly to one device with equivalent aspect ratio (W/L). Using this association principle, transistor M_b in Fig. 2 can also be substituted by a series-parallel association of identical transistors, M_{ba}, M_{bb}, M_{bc} and M_{bd}, resulting the circuit in Fig. 3.

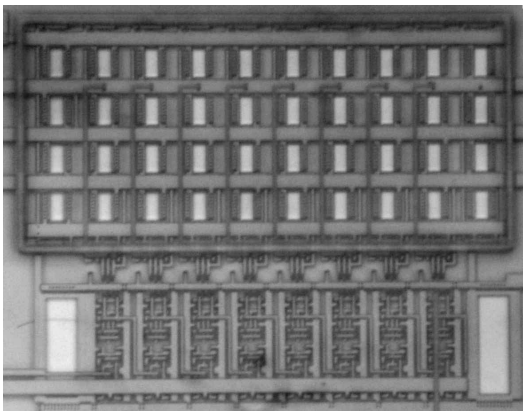

Figure 1. Micrograph of the 8-bit DAC (DAC1 shown). At the top area is the M-2M ladder and at the bottom area is the serial register.

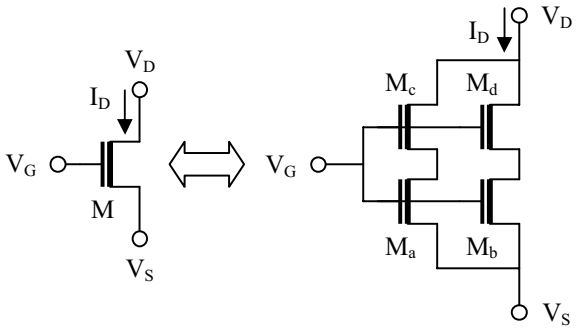

Figure 2. MOSFET association principle: one transistor can be substituted by a series-parallel association of identically designed transistors.

Since the main branches in Fig. 3 are equivalent, the applied current I_D is equally divided between them. The same

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current division principle can be used in the secondary branches, resulting in

$$I_{D1} = I_{D2} = I_D/2\,;\;\; I_{D2a} = I_{D2b} = I_{D2}/2 = I_D/4\,. \quad (1)$$

One can see that it is rather simple to establish a binary division of currents that flow through different branches of a series-parallel association of MOSFETs.

III. THE M-2M D/A CONVERTER

The transistor M_{bb} of Fig. 3 can also be substituted by another set of four transistors in series-parallel association, resulting in another binary division of the current. This procedure can be repeated successively, resulting in the network traditionally called the "M-2M ladder".

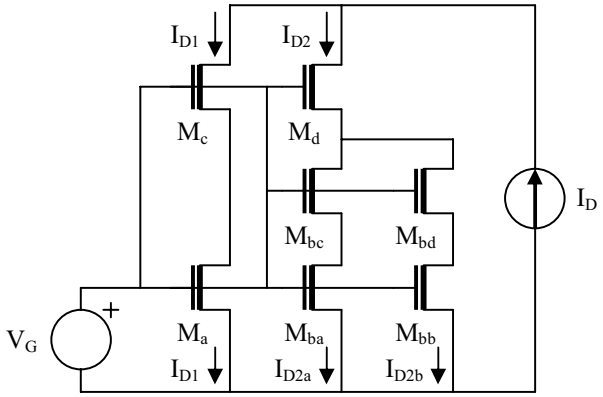

Figure 3. M_b in Fig. 2 can be substituted by a series-parallel equivalent association.

Fig. 4 shows the simplified schematic of the DAC, in which successive binary divisions of the input current I_R are performed. Here, each transistor in the bottom of the circuit in Fig. 3 is implemented by 2 drain-connected transistors (M_{i2} and M_{i3}, i = 7, 6…1, 0), which deviate the binary fraction of I_R to the nodes either I_0 (output node) or I_G (ground node), depending on the state of the register output Q_i. Both nodes I_0 and I_G are connected to zero Volt, as is also the reference G_B node. The gate voltage of the network, which together with the input current I_R defines the inversion level of the transistors, is generated by a bias circuit composed of M_{B1} and M_{B2}, which is current-biased through I_B. This strategy makes it possible to evaluate experimentally the impact of the inversion level of on the converter accuracy.

This programmable current divider has two major advantages: (a) MOSFETs perform simultaneously as elements of the divider network and as switches, and (b) the impedance of the current attenuator is independent of both the number of bits and the input data.

The branches where high currents can flow were implemented using the *Kelvin* (force-sense) technique, which require separated connection wires for current forcing and voltage measurement. This technique increases the accuracy of the characterization procedure, since all the voltage drops along these connections are compensated.

IV. MOSFET MISMATCH MODEL

MOSFET mismatch results from several process and geometric factors, which have been extensively studied, resulting in a dozen models in the last 20 years. The most used of them is known as Pelgrom's Model [4], which was proposed in 1989 and became an industry standard. Unfortunately, this model does not consider the nonlinear nature of MOSFETs in a proper manner, yielding to inconsistent formulas at high inversion levels. This inconsistency has been highlighted by the shrinking dimensions and reduced supply voltage of current submicron technologies, where transistors are designed to work from very weak to very strong inversion.

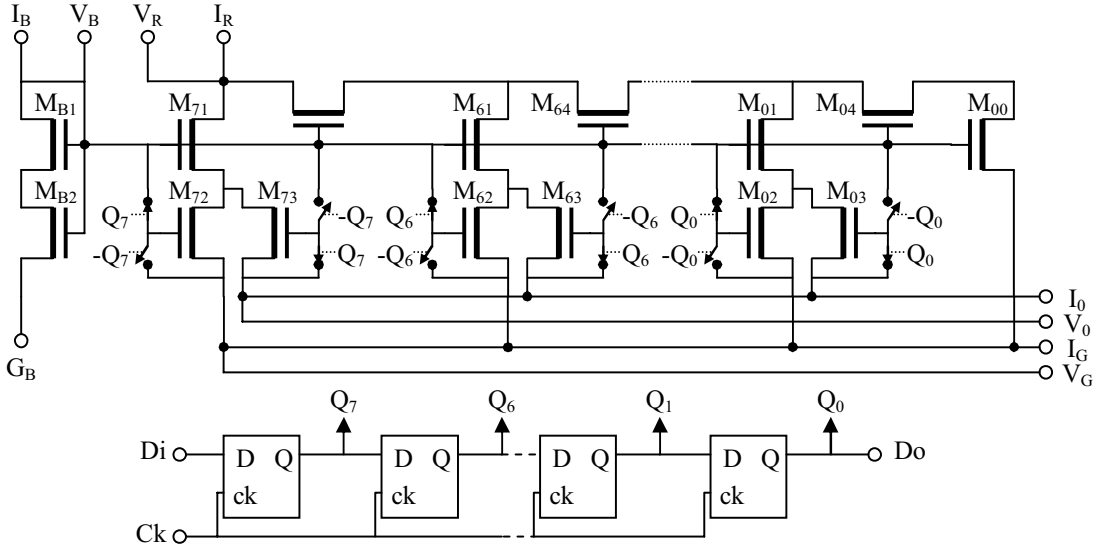

Figure 4. Simplified schematic of the 8 bit DAC that employs the M-2M ladder for the binary division of the reference current. The shift register at the bottom is used for the series-to-parallel conversion of the input word.

Recently we developed a new mismatch model, based on the integration of the contribution of the local dopant fluctuation along the MOSFET channel [5], keeping in mind the MOSFET nonlinearities through the use of the Advanced Compact MOSFET (ACM) model [6]. Doping concentration fluctuation that derives from the discrete nature of charges is widely recognized as the main mismatch cause for today's advanced technologies. The main result of our model [5] is a compact formula for current mismatch, in terms of geometry (W and L), bias (i_f and i_r) and technology (N_{oi} , B_{ISQ} and N^*)

$$\frac{\sigma^2_{I_D}}{I^2_D} = \frac{1}{WL}\left[\frac{N_{oi}}{N^{*2}}\frac{1}{i_f - i_r}\ln\left(\frac{1+i_f}{1+i_r}\right) + B^2_{ISQ}\right], \qquad (2)$$

where i_f and i_r are the forward and reverse inversion levels, and $N^* = -Q'_{IP} / q = nC'_{ox}\phi_t / q$ is the carrier density at pinch-off. N_{oi} is the main mismatch model parameter, representing the effective number of impurities per unit area in the depletion volume. B_{ISQ} is a less significant model parameter that accounts for variations in the specific current ($I_{SQ} = \frac{1}{2}\mu C'_{ox} n\phi_t^2$).

V. DAC DESIGN METHODOLOGY

To support experimentally our methodology, we have designed two versions of 8-bit M-2M DAC, being one (DAC1) with expected error within ±½ LSB, and the other (DAC0) with expected error within ±¼ LSB.

Designing the M-2M DAC can be understood as the transistor sizing, under some specified biasing condition (all devices of the ladder are identical). Basically, the DAC design involves:

- channel length determination (L), which is related to the impact of the short-channel effects on the converter performance, and;
- area determination (WL), since it is directly related to the matching of the transistors, and consequently to the accuracy of the converter.

One of the most significant short-channel effects that degrades the drain current is the *carrier velocity saturation* (CVS). This effect becomes significant when the channel length is reduced to such an extent that the carrier velocity is no longer proportional to the longitudinal electric field. To reduce the impact of this effect, we should either [2]: (a) operate any transistor far from saturation, or (b) chose L large enough such that the CVS phenomenon is made insignificant, even when the transistors saturate.

From Fig. 4, one can observe that only the transistors connected to I_R are prone to operate in saturation. But, unfortunately, these are the transistors with higher impact on the DAC accuracy, because they are related to the *most significant bit* (*MSB*).

Here we use the following expression [7] for the CVS effect on mobility

$$\mu_{sat} = \frac{\mu_0}{\sqrt{1+\left(\mu_0 V_{DS} / L v_{sat}\right)^2}}, \qquad (3)$$

where μ_0 is the low field mobility, v_{sat} is the carrier saturation velocity, and V_{DS} is the drain-source voltage. Equation (3) is known to describe the dependence of mobility under high longitudinal electric fields with quite good accuracy. The magnitude of v_{sat} is essentially independent of doping concentration, and is of the order of 10^7 cm/s for both electrons and holes at room temperature [8].

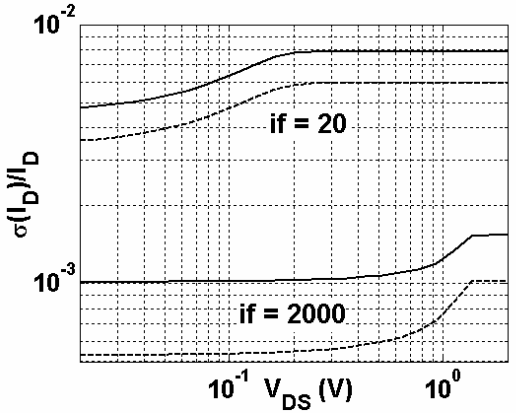

Figure 5. Normalized current mismatch for a 10 µm x 10 µm transistor, under two inversion levels (20 and 2000), using our mismatch model and *TSMC 0.35* extracted parameters. Dashed lines use $N_{oi} = 2\text{x}10^{12}$ cm^{-2} and B_{ISQ} = 0.4 %-µm. Solid lines use $N_{oi} = 3.5\text{x}10^{12}$ cm^{-2} and B_{ISQ} = 0.9 %-µm.

Considering $\mu_0 \approx 420$ cm^2/Vs (from MOSIS, for NMOS in *TSMC 0.35*) and a maximum drain voltage of 2V (high enough to saturate transistors biased at an inversion level around 5000), we calculated from (3) the minimum L necessary for an impact of the CVS effect less than ½ LSB on DAC1; the result is a minimum L equal to 9.81 µm. The resulting length is equivalent to the length of the series association of M_{71} and either M_{72} or M_{73}. Thus, we have used L = 5 µm for all transistors.

The transistor area was determined using the mismatch model described by (2). The mismatch parameters for this technology were experimentally extracted from another batch, using our custom-made test chip [9]. Measurements from 15 samples from the same run resulted in a N_{oi} that ranges between $2\text{x}10^{12}$ and $3.5\text{x}10^{12}$ cm^{-2}, and a B_{ISQ} between 0.4 and 0.9 %-µm. Using these set of data for N_{oi} and B_{ISQ}, Fig. 5 shows the expected mismatch for the series association of two transistors (W = 10 µm and L = 2 x 5 µm). We can see that, for the worst case, under saturation and i_f = 20, the maximum expected current deviation is 0.73%.

We chose two target inversion levels to make this DAC operate, one in very strong inversion (2000) and the other in moderate inversion (20). Since the DAC accuracy increases with the inversion level (matching improves), we designed the DAC to reach the minimum ±½ LSB accuracy for DAC1 under the lowest inversion level, which means a maximum mismatch of 0.78% (100%/128) for the current in the MSB branch. Using (2) with the worst case parameter, and

calculating the area for the saturation condition and $i_f = 20$, resulted, for two series-connected transistors, in an area equal to 94.4 μm^2. Thus, we have used for all transistors $W = 10$ µm.

DAC0 was designed for an accuracy 2 times better than that of DAC1; thus we used an area 4 times larger for DAC0, resulting in the following transistor geometry: $W = 20$ µm and $L = 10$ µm.

VI. MEASUREMENTS

The dc performance of the DACs was measured from 20 samples of the same *TSMC 0.35* process batch. It was done using the *Agilent 4156B* semiconductor parameter analyzer controlled by a PC computer, also responsible for programming the DAC data through a custom-made optically isolated serial interface.

DAC characterization was performed for inversion levels of 20 and 2000. The input reference current I_R was set equal to 1.9 times the bias current I_B, making the current in the MSB branch equal to 0.95 I_R, which means that the ladder operates near but out from saturation.

For each input data D, we calculated the error (Err) of the measured analog output current relative to an ideal output current equal to $(D/256)xI_R$. This procedure was repeated for every DAC sample, and finally the standard deviation of these errors was determined for every input data.

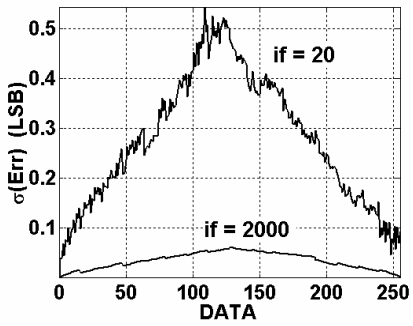

Figure 6. Standard deviation of the measured error from 20 samples of DAC1, versus input data, for inversion levels of 20 and 2000. Values are normalized to 1 LSB.

Fig. 6 shows the characterization results from 20 samples of DAC1. It can be seen that the measured average error is near ½ LSB, which agrees with the design. Maximum error occurs around one half of full scale, showing the predominance of the MSB error over the other bits. The DACs were characterized also for $I_R/I_B = 0.5$, 1.0, and 1.5, resulting in similar errors.

From Fig. 5 one can observe that the errors for inversion levels equal to 20 and 2000 result around 1 decade of mismatch difference. So, we could expect the same ratio for the DAC accuracy from our measurements, which can be seen in Fig. 6.

Fig. 7 shows the results from the same characterization procedure for DAC0. Here we can see that DAC0 is around 2 times more accurate than DAC1, as designed. Since the curves for both inversion levels present similar behavior to the results from DAC1, the same conclusions hold.

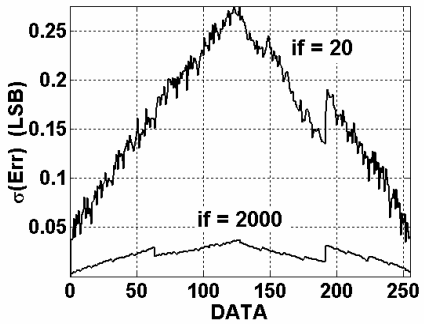

Figure 7. Standard deviation of the measured error from 20 samples of DAC0, versus input data, for inversion levels of 20 and 2000. Values are normalized to 1 LSB.

VII. CONCLUSIONS

A design methodology for M-2M DAC ladder was proposed. Through this methodology, transistor area (WL) is determined, based on our MOSFETs mismatch model, which is continuous in all operating regions. Carrier velocity saturation has also been taken into account for channel length determination. Two DACs were designed for different accuracies, and fabricated in *TSMC 0.35* technology. Experimental measurements were performed in 20 samples of each DAC, and statistical results corroborate our methodology.

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