# TEMPERATURE PERFORMANCE OF SUB-1V ULTRA-LOW POWER CURRENT SOURCES

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*Abstract*— **This paper presents the temperature performance of two self-biased current sources. We have employed a simple topology to design 4nA and 900pA current references implemented in both 0.35µm and 0.18µm technologies, respectively. Experimental results showed that the current source implemented in 0.35µm technology can operate at a supply voltage as low as 1V and at 650mV in 0.18µm CMOS technology. The temperature performance of the current source is analyzed in this paper. The association of a very simple topology, an efficient design procedure, low voltage cascode transistor and low output conductance trapezoidal transistors has resulted in small area, ultra low power consumption and a line regulation better than 0.2%/V of supply voltage.**

## I. INTRODUCTION

The increasing demand for inexpensive very low power portable and implantable medical applications has resulted in the integration of low-voltage CMOS analog circuits compatible with standard VLSI technologies [1], [5]. This tendency has motivated the development of systematic methodologies for analog design. Furthermore, efficient, simple and easy-to-design analog circuit structures are highly desirable [2]-[6].

Methodologies for CMOS analog design based on the concept of inversion level [1], [6], [7] have been shown to provide a robust alternative for high performance in very low power [6] and low-voltage circuits [1]. In these methodologies, the MOSFET bias current is dependent on technological parameters. Analog circuits based on such technique require a current reference to be generated on-chip or, in other words, the design calls for a self-biased current source (SBCS) that serves as a reference for the bias currents. The advantages of the SBCS presented here have already been summarized in [6].

This paper presents a design procedure and temperature analysis for a self-biased current source dedicated to technology-independent inversion level biasing, which is suitable for low-voltage and very low power applications. Our SBCS circuit uses MOSFETs only, can operate down to 650mV (in 0.18µm technology) supply voltage and exhibit an approximate proportional-to-absolute-temperature (PTAT) behavior from -70 to 130ºC.

In Section II, the Advance Compact Model (ACM) and the concept of inversion level are summarized. We develop the basic design equations for the SBCS using the ACM model in Section III. Section IV introduces the low-voltage CMOS SBCS. The temperature analysis is developed in Section V. As a design example, a sub-1V very low power SBSC is implemented in both 0.35µm and 0.18µm CMOS processes and the associated experimental results are presented in Section VI. Finally, concluding comments are presented in Section VII.

## II. THE ACM MODEL

In the design procedure of the self-biased current source, we have employed ACM, a current-mode MOSFET model that uses the concept of inversion level [7]. The ACM model provides continuous analytical functions for the transistor current from weak to strong inversion. According to the ACM model, the drain current of a long channel transistor can be split into the forward ($I_F$) and reverse ($I_R$) currents

$$I_D = I_F - I_R = I_S(i_f - i_r) \tag{1}$$

where

$$I_S = I_{SQ}\left(\frac{W}{L}\right) = I_{SQ}(S) \tag{2.a}$$

$$I_{SQ} = \mu C'_{ox}\, n \frac{\phi_t^2}{2} \tag{2.b}$$

$I_F(I_R)$ is dependent on the gate and source (drain) voltages. In forward saturation, $I_F >> I_R$; consequently, $I_D \cong I_F = I_S i_f$. $I_S$ is designated the normalization (specific) current and $I_{SQ}$ is the sheet specific current ($I_S$ for $W = L$), $i_{f(r)}$ is the forward (reverse) inversion level, and µ, $n$, $C'_{ox}$, $\phi_t$, and $W/L=S$ are the mobility, slope factor, gate oxide capacitance/area, thermal voltage, and the transistor aspect ratio, respectively. The relationship between current and voltage is given [7] by

$$\frac{V_P - V_{S(D)}}{\phi_t} = \sqrt{1+i_{f(r)}} - 2 + \ln\left(\sqrt{1+i_{f(r)}} - 1\right) \tag{3}$$

$$V_P \cong \frac{V_{GB} - V_{T0}}{n} \tag{4}$$

where $V_P$ is the pinch-off voltage and $V_{TO}$ is the zero bias threshold voltage. More details on (1)-(4) can be found in [7].

## III. DESIGN EQUATIONS FOR SCM

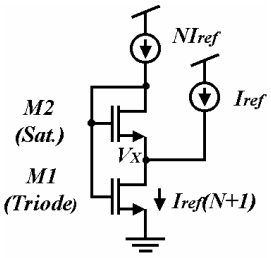


**Fig. 1.** Schematic of the SCM connected in diode configuration.

The association of transistors in Fig. 1, which is called here the self-cascode MOSFET (SCM), is the core of the SBCS. As will be seen next, the SCM can perform either as a PTAT voltage generator if $I_{ref}$ is a copy of the specific current of the technology or, conversely, as a specific current generator if voltage $V_X$ is imposed at the intermediate node is PTAT. The derivation of design equations (5) and (6) from (1) through (3) is straightforward [6] and will not be repeated here. The relationship between $i_{f1}$ and $i_{f2}$

$$\alpha = \frac{i_{f1}}{i_{f2}} = \left[1 + \frac{S_2}{S_1}\left(1 + \frac{1}{N}\right)\right] \qquad (5)$$

with factor $N$ defined by the gain of a PMOS current mirror. The application of (3) to $M_2$ an $M_1$ results in

$$\frac{V_X}{\phi_t} = \sqrt{1+\alpha i_{f2}} - \sqrt{1+i_{f2}} + \ln\left(\frac{\sqrt{1+\alpha i_{f2}}-1}{\sqrt{1+i_{f2}}-1}\right) \qquad (6)$$

We note here that (6) is valid for any inversion level; also, since $\alpha$ is independent of temperature, the voltage at the intermediate node $V_X$ is PTAT as long as the inversion level $i_{f2}$ at the source of $M_2$ is independent of temperature *i.e.*, provided that $I_{ref}$ is a replica of the specific current.

In order to get an insight into the design methodology, we show in Fig. 2 a family of curves that represents the variation of $V_X$ in terms of the inversion level of $M_2$ for several values of $\alpha$, according to expression (6). We observe in Fig. 2 that, for small values of $i_{f2}$ ($i_{f2}$ < 0.1), voltage $V_X$ is almost independent of the bias current but depends on $\alpha$ or, conversely, that the value of $i_{f2}$, *i.e.* the current is extremely sensitive to $V_X$. For moderate and high values of $i_{f2}$ ($i_{f2}$ >1) the dependence of $i_{f2}$ on $V_X$ decreases progressively. In our project we have decided to operate at a moderate level of $i_{f2}$. This choice of $i_{f2}$ serves two purposes: (i) the operation of $M_2$ in weak inversion would give rise to a current very sensitive to voltage $V_X$; in this case, the reference current would be very sensitive to errors in $V_X$ due to transistor mismatch, for example (ii) for the sake of operating the circuit under low supply voltages, the selected inversion level of $M_2$ should have a relatively small value in moderate inversion so that its gate-to-source voltage is close to the threshold voltage.

In our design methodology, we have chosen the SCM ($M_1$, $M_2$) to operate in moderate inversion with $i_{f2}$=10, $S_2 = S_1$ and $N$=1, thus yielding $\alpha$=3.

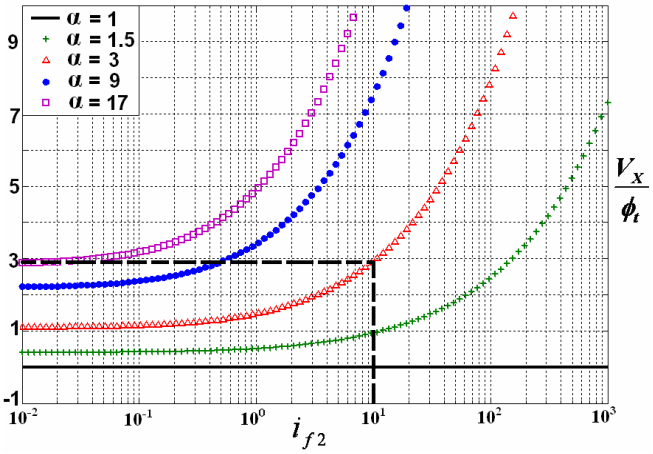


**Fig. 2.** Family of V-I curves of the SCM.

Now, since we have already defined $i_{f2}$=10, and $\alpha$=3, the choice of the aspect ratio will give the value of the reference current, i.e.,

$$NI_{ref} = I_{S2} i_{f2} = S_2 I_{SQ} i_{f2}$$

For $N$=1 and $i_{f2}$=10, we have $I_{ref}$ = $10 S_2 I_{SQ}$. Inserting the values of $i_{f2}$=10 and $\alpha$=3 in (6) we find $V_X/\phi_t \cong 2.93$. At this point the design methodology of the current generator is almost concluded. What we need now is to generate a PTAT voltage equal to $V_X$ and transfer this voltage to the intermediate node of the SCM and impose the equality of the current sources ($N$=1) through the use of current mirrors. This is the subject of next section, which will present the blocks needed to set the value of the PTAT voltage at the intermediate node of the SCM.

## IV. THE PROPOSED LOW-VOLTAGE SBCS

A full version of our SBCS circuit is shown in Fig. 3. We propose a simple power-efficient SBCS circuit that replaces the resistor of the implementation in [2] with an SCM operating in moderate inversion to achieve the requirements of low current and low voltage operation.

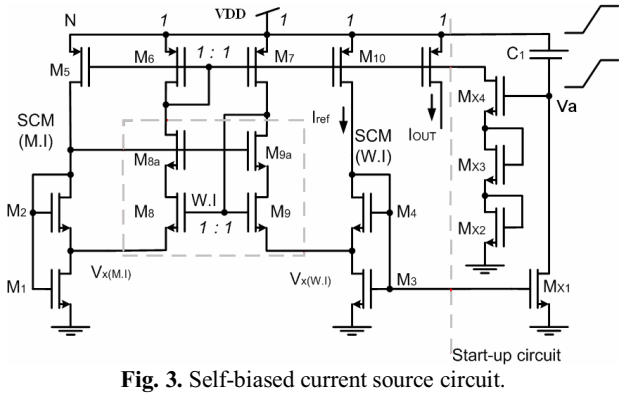


**Fig. 3.** Self-biased current source circuit.

The PTAT voltage reference is implemented by the SCM ($M_3$, $M_4$) biased in weak inversion ($i_f$ <1); and the V-I conversion is implemented by the SCM ($M_1$, $M_2$) biased in moderate inversion (1<$i_f$ <100). Transistors $M_6$-$M_9$ forms a self-biasing voltage-following (NMOS) current-mirror (PMOS) [12] which applies the PTAT voltage into the node

$Vx$ of the SCM ($M_3$, $M_4$). Transistors $M_{8a}$ and $M_{9a}$ are low-voltage cascode devices utilized to improve the power supply regulation. The PMOS devices $M_{5\text{-}7}$ and $M_{10}$ are unity-gain current mirrors for smaller consumption.

Using the cascode transistors ($M_{8a\text{-}9a}$) the implementation results in smaller systematic offsets [8]. The PMOS current mirror uses trapezoidal transistors [10] to improve the regulation of the current reference without requiring a large silicon area while maintaining low-voltage operation.

The minimum supply voltage, which is determined by the constraints imposed by the two leftmost branches in Fig. 3, can be approximated as

$$V_{DD} \geq \max\{|V_{DSsat,P}| + V_{GS,1}, |V_{GS,P}| + V_{DSsat,8} + V_{DS,8a} + V_X\} \qquad (7)$$

where $V_{DSsat,8} \cong 100mV$ since $M_8$ operates in weak inversion. The p-channel transistors are sized in order to operate in weak inversion, with an inversion level close to 1 or smaller; therefore, $|V_{DSsat,P} \cong 100\ mV|$ and $V_{GS,P} \cong V_{TP}$. Since $V_X$ is less than 100 mV, and $M_1$ operates in moderate inversion with $V_{GS,M1} \cong V_{TN} + 100$ mV and assuming that the minimum value of $V_{DS8a}$ is around 50 mV, the minimum supply voltage becomes approximately

$$V_{DD} \geq \max\{|V_{TP}|, V_{TN}\} + 200mV \qquad (8)$$

For a current reference $I_{ref} << I_{SQ}$ *(NMOS)*, $S_9$=1 keeps $M_9$ in weak inversion. The aspect ratio ($S_P$) of the PMOS transistors $M_5$-$M_7$ ($M_{10}$) is calculated using

$$S_P = \frac{I_{DP}}{I_{SQP} . i_{f\,P}}$$

and a proper choice of the inversion level $i_{fP}$ usually less than 1 for low-voltage applications.

The sensitivity of the circuit to supply power is associated with the short channel effect of $M_7$ and $M_8$. The short channel is reduced using long channel lengths that, however, demand large silicon area. One approach to obtain equivalent long channel devices with moderate area is the trapezoidal transistor proposed in [10] and low-voltage cascode transistors.

This SBCS has two operating points, the desired state $I_{ref}$ and the undesirable condition where all internal currents are zero. The zero current state can be proven to be meta-stable [11]; however, to reduce the time to charge up the internal nodes a capacitive start-up circuit that does not consume static power has been included in our design. This circuit, $M_{X1\text{-}4}$ and capacitor $C_1$, operates as follows: at power-on the voltage VDD changes from zero to its nominal value. The voltage Va accompanies the VDD ramp initially, and the current through $M_{x4}$ charges down the gate capacitance of the p-channel MOSFET's; so current appears in the whole circuit. $M_{x1}$ monitors the start-up current and charges the bottom plate of $C_1$ down to ground. When Va approaches 0V, $M_{x4}$ turns off. Transistors $M_{x2\text{-}3}$ limits the maximum start-up current and reduces the leakage current of $M_{x4}$ at high temperatures.

## V. TEMPERATURE ANALYSIS

The self-biased current-source circuit proposed in Fig. 3 is an extractor of the specific current ($I_{SQN}$) of NMOS transistors. An NMOS transistor biased with a scaled replica of the specific current $I_{SQ}$ presents an inversion level independent of process and temperature. The specific current is an intrinsic parameter that contains information about process and temperature, as defined by Eq. (2.b), where $\mu, C'_{ox}, n$ are temperature dependent parameters approximated by

$$\mu = \mu_0 . \left(\frac{T}{T_0}\right)^{-m} \qquad (9) \qquad C'_{ox}(T) = \frac{\varepsilon_{sio2}(T)}{T_{ox} + \Delta T_{ox}(T)} \qquad (10)$$

where $T_0$ is the reference temperature and $m$ is a positive constant in the range of 1.2 to 2 [9]. The gate capacitance changes with temperature according to (10), but its variation with temperature is usually negligible (<40ppm/°K).

Neglecting the weak dependence of the slope factor on the temperature, the specific current is written as

$$I_{SQ}(T) = \mu_0 C'_{ox}\, n_0\, \frac{\phi_{t0}^{\,2}}{2} \left(\frac{T}{T_0}\right)^{2-m} \qquad (11)$$

where $\mu_0$, $n_0$ and $\phi_{t0}^{\,2}$ are defined at room temperature, and 2-m≅1 for the CMOS process of the circuits designed in this research.

## VI. EXPERIMENTAL RESULTS

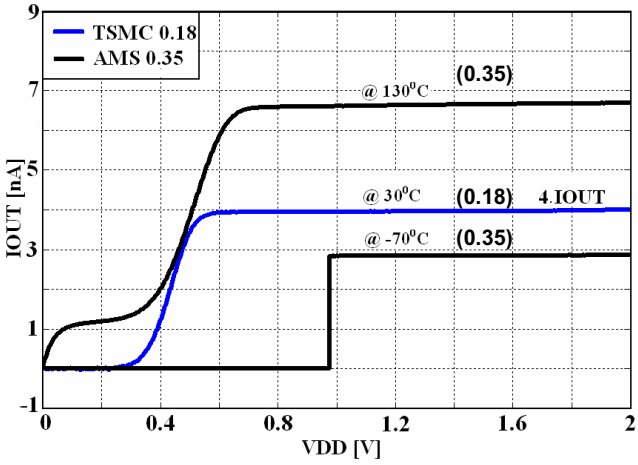


**Fig. 4.** Iout for AMS 0.35µm vs. VDD at several temperatures.

The experimental results (Fig. 4) show that the sensitivity of the reference current to the supply is quite low (0.2%/V) and very appropriate for most applications. These results validate the design and show that the current source can operate at voltages down to the value resulting from (7), in the AMS 0.35µm(TSMC 0.18µm) technology used for the current reference, $V_{TP}$= -0.65V(-0.4V) and $V_{TN}$ = 0.5V(0.4V).

As can be observed in Fig. 5, the variation of the reference current over a temperature range of 100ºC is approximately 30%, showing an approximately PTAT behavior with sub-1V operation from -70ºC to 130 ºC.

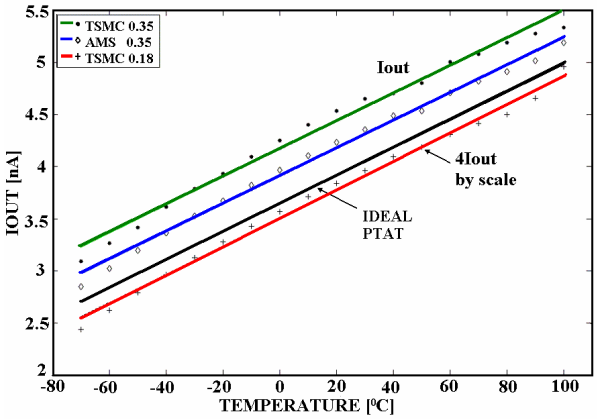


**Fig. 5.** Output current for several technologies vs. temperature.

The average current reference obtained from two sets of 15 (0.35µm with an area of 0.02mm$^2$, Fig 7) and 40 (0.18µm with an area of 0.01mm$^2$) samples is 4.2nA and 900pA, respectively, with a 3σ deviation of ±8% at 1.0V supply, see Fig. 6.

For temperatures close to 110ºC or higher, the leakage currents through both the protection diode of the current pad and the SBCS circuit become of the order of the reference current and, thus, the current measured is higher than expected.

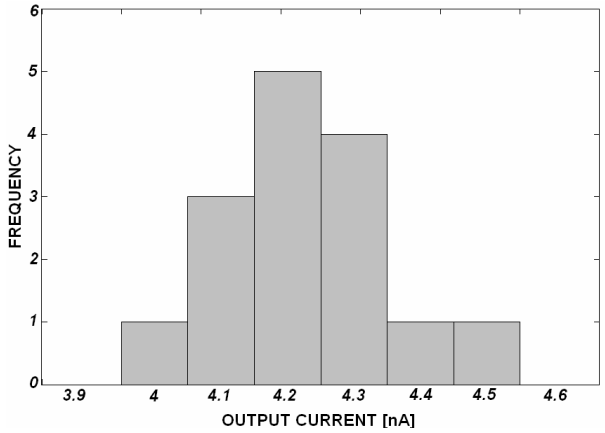


**Fig. 6.** Histogram of Iout for AMS 0.35µm.

## VII. CONCLUSIONS

A low-voltage low-power self-biased current source with start-up circuit has been presented. A graphic design procedure based on the ACM model has been provided. Experimental results have shown that the SBCS provides ultra-low power operation, low sensitivity to changes in the supply voltage, small silicon area and can operate at power supply voltages down to 1.0 V in a 0.35µm technology and from 650mV in a 0.18µm technology. The SBCS circuits presented an approximately PTAT behavior. The SBCS was shown to be particularly suited to very-low power low-voltage applications, due to operation of all transistors in either moderate or weak inversion.

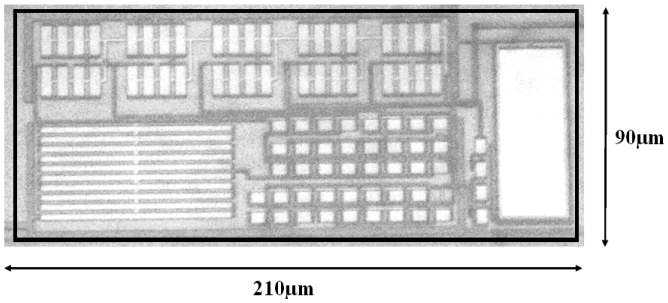


**Fig. 7.** Micrograph of SBCS for AMS 0.35µm.

## ACKNOWLEDGEMENTS

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