A Simple Modeling of the Early Voltage of MOSFETs in Weak and Moderate Inversion

R. L. Radin, G. L. Moreira, C. Galup-Montoro, M. C. Schneider
Electrical Engineering Department - Federal University of Santa Catarina
Florianópolis, SC, Brazil
marcio@eel.ufsc.br

Abstract – **This paper presents a simple model of the Early voltage for the MOS transistor operating in weak and moderate inversion. The model is based on a decomposition of the transistor channel into a region where the gradual-channel approximation holds and a region that is modeled as a reverse-biased juntion. Measurements of the characteristics of both n- and p-channel transistors with different channel lengths in a 0.35 μm technology demonstrate the feasibility of the proposed model.**

I. INTRODUCTION

In the design of CMOS analog circuits, the Early voltage (or the output conductance) of a transistor in saturation is a fundamental parameter since it affects, for example, the accuracy of current mirrors and the gain of voltage amplifiers. The output conductance in saturation is difficult to determine due to the need for modeling the short-channel effects. The simplest approach to model the saturation region assumes the Early voltage to be a constant, which is inadequate for either simulation or even first-order hand calculations. An improved model of the Early voltage considers it to be proportional to the channel length and independent of both current level and drain voltage [1], but it can deviate too much from the true Early voltage. For more accurate calculations of the Early voltage, two approaches are usually employed. One of them is to solve the two-dimensional Poisson's equation either numerically or using approximate solutions [2]-[5]. However, this procedure is too complicated to be used for circuit simulation or hand calculations. Another approach, the one used in this work, describes separately each short-channel phenomenon that affects the output conductance and superimposes the effects of them all. The short-channel phenomena to be presented here are the channel-length modulation (CLM) [6]-[9] and the drain-induced barrier lowering (DIBL) [8]-[13]. Here we show that an earlier approach [7] to model the output conductance of MOSFETs can give accurate results for transistors operating in weak and moderate inversion. In effect, using the continuity of the electric field between the channel and the saturation regions along with an all-regions transistor model allows a simple but accurate calculation of the channel length shortening. Weak avalanche (WA) was removed in our measurements by measuring the source current rather than the drain current. Restricting our analysis to moderate/low inversion levels introduces a great simplification for solving the electrostatics since the carrier charge can be neglected and the results thus obtained can be applied to a large class of circuits that operate at low/moderate inversion levels. The goal of this work is to arrive at both a simple and satisfactorily accurate model of the Early voltage for hand calculations as in [14]-[16].

Concepts of the long-channel MOSFET theory are reviewed in Section II. The modeling of the short-channel effects is introduced in Section III. The experimental results together with a set of fitting curves are presented in Section IV. Conclusions are drawn in Section V.

II. LONG-CHANNEL THEORY

The MOSFET model hereinafter is strongly based on two physical features of the MOSFET structure, namely the charge-sheet model and the incrementally linear relationship between the inversion charge density Q'_I and the surface potential ϕ_S

$$dQ'_I = nC'_{ox}d\phi_S\,, \qquad n = 1 + C'_b / C'_{ox} \tag{1}$$

In (1), C'_{ox} and C'_b are the oxide and bulk capacitances, respectively. n is the slope factor, which is slightly dependent on the gate voltage. $C'_b=-dQ'_B/d\phi_S$ is calculated from the potential balance equation

$$V_G = V_{FB} + \phi_S - \frac{Q'_B + Q'_I}{C'_{ox}} \tag{2}$$

assuming $Q'_I=0$. The charge-sheet approximation allows writing the bulk charge for an n-channel MOSFET as

$$Q'_B = -\gamma C'_{ox}\sqrt{\phi_S - \phi_t}\,, \tag{3}$$

where γ is the body effect coefficient and ϕ_t is the thermal voltage. The surface potential ϕ_{Sa} at which the inversion charge density equals zero can be readily obtained from (2) and (3) with $Q'_I=0$:

$$\phi_{Sa} - \phi_t = \left(\sqrt{V_G - V_{FB} - \phi_t + \frac{1}{4}\gamma^2} - \frac{1}{2}\gamma\right)^2 . \tag{4}$$

The relationship between the inversion charge density and the applied voltages is given by the unified charge control model (UCCM) [8]-[9], which can be written as

$$\phi_{Sa} - 2\phi_F - V_C = \phi_t \left[\frac{Q'_I}{Q'_{IP}} + \ln\left(\frac{Q'_I}{Q'_{IP}} \right) \right], \qquad (5)$$

where $Q'_{IP}=-nC'_{ox}\phi_t$ is the thermal charge, ϕ_F is the Fermi potential for holes, and V_C is the channel voltage.

For the calculation of the drain current, we use the Pao-Sah equation [17]

$$I_D = -\mu W Q'_I \frac{dV_C}{dy} \qquad (6)$$

In order to simplify the notation we make use of the following normalized variables

$$q'_I = \frac{Q'_I}{Q'_{IP}}, \qquad i_d = \frac{I_D}{I_S}$$

where $I_S=\mu C'_{ox} n \phi_t^2 W/2L$ is the normalization current. Using (5) for the calculation of the derivative of the channel voltage in terms of the derivative of the inversion charge density and inserting the result in (6), gives the relationship between the normalized current and the variation of the normalized inversion charge density along the channel as

$$i_d = -2L\left(q'_I + 1\right)\frac{dq'_I}{dy}. \qquad (7)$$

For CLM modeling, we calculate the longitudinal field of the transistor along the channel as

$$F_y(y) = -\frac{d\phi_S}{dy} = \phi_t \frac{dq'_I}{dy} = -\frac{i_d}{q'_I + 1}\frac{\phi_t}{2L}. \qquad (8)$$

Note that (1) has been used in (8) to substitute the variation of the inversion charge density for the variation of the surface potential.

III. SHORT-CHANNEL EFFECTS IN WEAK AND MODERATE INVERSION

Reverse bias of the drain junction creates a field pattern that can lower the potential separating the source from the drain, resulting in increased injection of carriers by the source [8], [11]. This phenomenon is referred to as drain-induced barrier lowering (DIBL). The modeling of DIBL is a difficult task owing to the intrinsic two-dimensional nature of the effect [8], [10], [11]. The inclusion of the DIBL effect in MOSFET models is generally through a modification in the threshold voltage [8]. An analytical model of the dependence of the threshold voltage V_T on technological parameters and bias is shown in [12] and rewritten in a modified form in [8] as

$$V_T \cong V_{Tlc} - \sigma\left[\left(\phi_{bi} + V_{SB}\right) + \left(\phi_{bi} + V_{DB}\right)\right] \qquad (9)$$

to emphasize the source-drain symmetry. In (9), V_{Tlc} is the threshold voltage of the long-channel device whereas σ is DIBL factor, which depends on technology and channel length [12]. Expression (9) is the one used in this work to model the DIBL.

Since the analysis of the output conductance in this work is limited to weak and moderate inversion, we can neglect the carrier charge in comparison with the bulk charge in order to solve Poisson's equation. Also, we assume that the normalized inversion charge density at the drain end of the channel in saturation is less than unity (see the Appendix for details).

The CLM model we derive next is a modified version of the model developed in [7]. Since we have limited our analysis to weak and moderate inversion, we have used the long-channel equations of the previous section to derive the so-called channel length modulation.

As V_D increases, the depletion region of drain-channel junction widens, thus shortening the effective channel length. For a MOSFET operating in saturation, the gradual channel approximation (GCA) used to derive the long-channel equations becomes less valid, especially in the vicinity of the drain junction. The usual approach employed to find an analytical formulation for the saturation region divides the channel into two sections, as shown in Fig. 1. In one of them, closer to the source, the GCA is valid while in the other one, closer to the drain, the two-dimensional nature of the space-charge region must be accounted for [8]. Using this formulation, the current can be calculated using the expression derived under the GCA but considering the effective channel length of the device to be reduced by the length Y_D of the drain section. A similar channel length shortening close to the source end can also be calculated, even though its value is of minor importance for calculating the dependence of the current on the drain voltage.

To derive the model for CLM in weak and moderate inversion we make the following hypotheses: (i) the transistor can be divided into two regions, I and II , the former closer to the source and the latter closer to the drain, as shown in Fig. 1 (a) (ii) in region I, the GCA is valid, *i.e.*, expressions (1) through (8) hold; (iii) in region II, Poisson's equation is solved assuming that both the contribution of the carriers to the charge density and the transversal component of the electric field are negligible; (iv) the drain junction is an N^+P-step junction. Under these assumptions, the solution of Poisson's equation gives for Y_D

$$Y_D = \sqrt{\left(\frac{F_L}{2a}\right)^2 + \frac{V_{bi} + V_{DB} - \phi_{SL}}{a}} - \frac{F_L}{2a}, \qquad (10)$$

where

$$F_L = F_y(y = L - Y_D) = -\frac{i_d}{1 + q'_{ID}}\frac{\phi_t}{2L} \cong -i_d \frac{\phi_t}{2L}, \qquad (11)$$

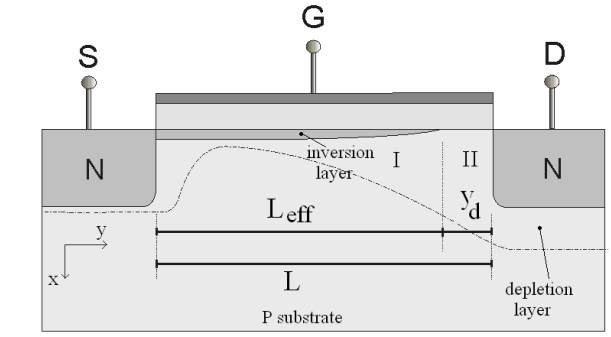
$$\phi_{SL} = \phi_S(y = L - Y_D) = \phi_{Sa} - \phi_t q'_{ID}, \qquad (12)$$

with $q'_{ID}=q'_I(y=L-Y_D)$. V_{bi} is the built-in potential and $a=qN_A/2\varepsilon_S$.

Assuming that the Early voltage is dominated by DIBL and CLM, we find, from (9) and (10) that

$$\frac{1}{V_A} = \frac{1}{I_D}\frac{dI_D}{dV_D} = \frac{1}{V_{ADIBL}} + \frac{1}{V_{ACLM}}, \qquad (13)$$

$$V_{ADIBL} \approx \frac{n\phi_t}{2\sigma}\left(\sqrt{1+i_{dsat}}+1\right) \qquad V_{ACLM} \cong 2aL_{eff}(Y_D+\frac{F_L}{2a}). \quad (14)$$



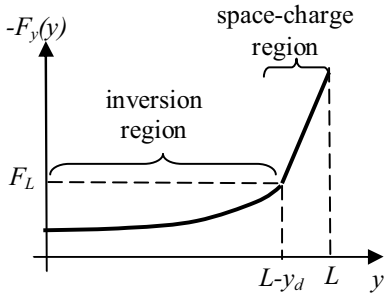


Fig. 1. (a) Charge distribution in the n-MOS transistor in saturation; (b) Electric field along the channel (x=0) [7].

In our simplified model, the DIBL component of the Early voltage depends on the inversion level according to (14) but is nearly independent of V_{DS} while the CLM component is proportional to the square root of V_D.

IV. EXPERIMENTAL RESULTS

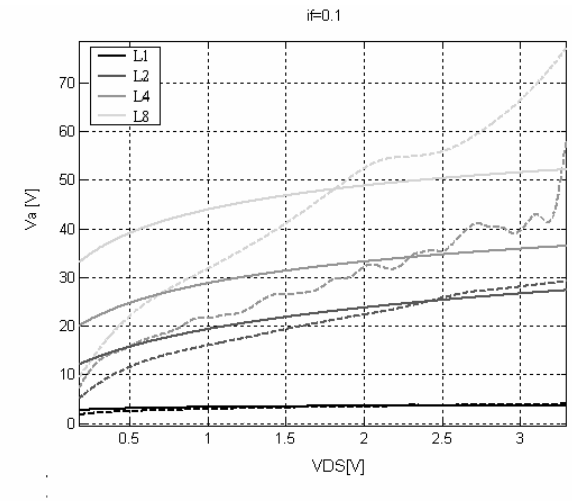


Fig. 2. Experimental (dashed lines) and fitted (solid lines) Early voltages of n-channel transistors for i_f=0.1.

Plots of experimental and fitted Early voltages of n-channel devices for inversion levels at the source equal to 0.1 and 100 are shown in Fig. 2. and Fig. 3. , respectively. These set of curves are representative of the data for operation below i_f= 100. In fact, the characteristics for i_f<1 are quite similar and, as a first order approximation, the Early voltage is not sensitive to the inversion level in weak inversion (i_f<1). For inversion levels greater than unity, the Early voltage increases very slowly with increasing inversion levels (please, compare Fig. 2 with Fig. 3). Fig. 4 displays the experimental and fitted Early voltages for the minimum-length n-MOS transistor. Table I presents the fitting parameters for L1=L_{min} (minimum channel length), L2=2 L_{min}, L4=4 L_{min}, and L8= 8 L_{min}. The DIBL factor was extracted for each channel length. For the 0.35 µm technology of the fabricated the devices, the nominal substrate doping is 2.2 10^{17} cm^{-3}, which gives a= 1.67 10^{14} V/m^2, a value relatively close to the one extracted from the Early voltage.

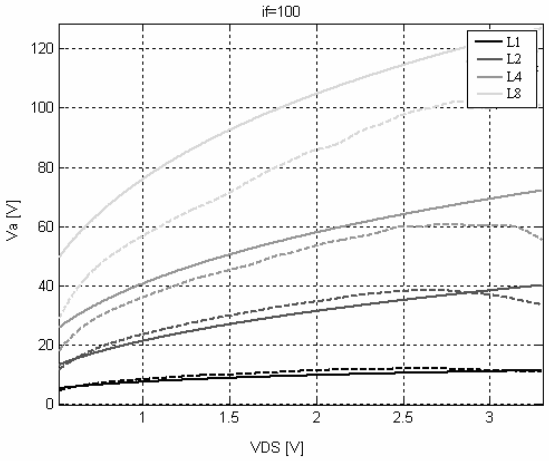


Fig. 3. Experimental (dashed lines) and fitted (solid lines) Early voltages of n-channel transistors for i_f=100.

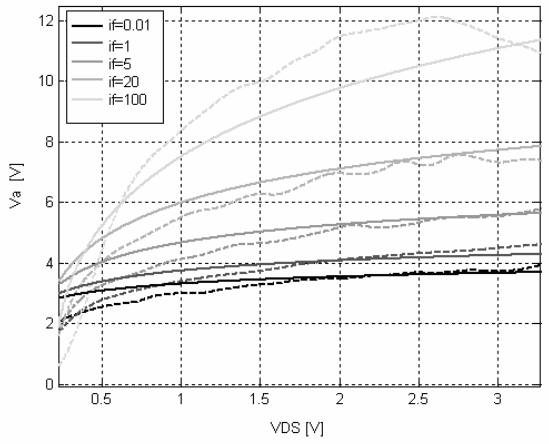


Fig. 4. Experimental (dashed lines) and fitted (solid lines) Early voltages of minimum-length n-channel transistor.

Fig. 5. displays the experimental and fitted Early voltages for the minimum-length p-MOS transistor.

TABLE I. FITTING PARAMETERS FOR THE N-CHANNEL TRANSISTORS IN 0.35 µm TECHNOLGY.

Transistor	σ [mV/V]	a [V/m^2]	$\phi_{bi} - 2\phi_F$ [V]
L1	7	2.5 10^{14}	0.1
L2	0.8	2.5 10^{14}	0.1
L4	0.6	2.5 10^{14}	0.1
L8	0.45	2.5 10^{14}	0.1

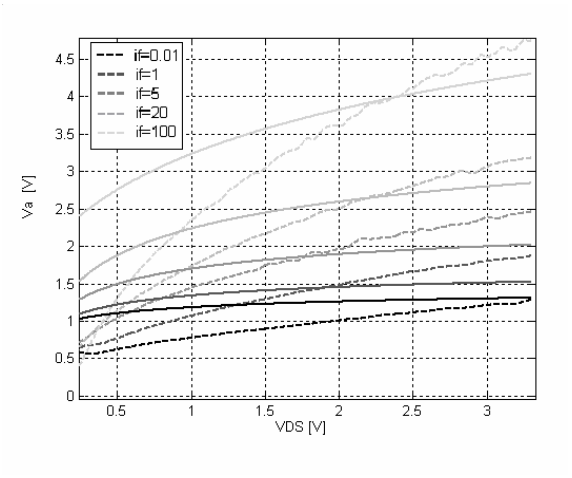


Fig. 5. Experimental (dashed lines) and fitted (solid lines) Early voltages of minimum-length p-channel transistor.

V. CONCLUSIONS

We presented a very simple model of the Early voltage in MOS transistors operating in weak and moderate inversion. The measurements taken from a set of n- and p-channel devices in 0.35 µm technology demonstrated that the very simple model of the Early voltage we have developed correlates very well with experimental data. The model we derived here is useful for hand calculations, simulation, and parameter extraction.

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APPENDIX

The maximum current that can flow in the channel is limited by the maximum carrier velocity [8],[14]. When electrons at the drain end of the channel reach the saturation velocity, the drain current is expressed as

$$I_{Dsat} = -W v_{sat} Q'_{IDsat} . \qquad \text{(A1)}$$

In (A1), Q'_{IDsat} is the inversion charge density at the drain end of the channel. Normalizing both the charge and the current in (A1) yields

$$i_{dsat} = \frac{I_{Dsat}}{I_S} = \frac{2}{\zeta} q'_{IDsat} , \qquad \text{(A2)}$$

with $\zeta = \phi_t \mu_o / L v_{sat}$. Typical values for zero-field mobility and saturation velocity in the 0.35 µm CMOS technology are μ_o=420 cm^2/Vs and v_{sat}= 1.5x 10^7 cm/s. For the minimum channel length L=0.35 µm, we have ζ=0.02. For the maximum normalized current i_d=100, (A2) gives $q'_{IDsat} = 1$