Design-oriented Model for Nonlinearities in MOSFETs

P.D. da Silva, C. Galup-Montoro and M.C. Schneider
Department of Electrical Engineering
UFSC-Federal University of Santa Catarina
88040-900 Florianopolis SC, Brazil
Email:pablo, carlos, marcio@eel.ufsc.br

F. Rangel de Sousa
Department of Electrical Engineering
Federal University of Rio Grande do Norte
59072-970 Natal RN Brazil
Email: frangel@dee.ufrn.br

***Abstract*—In this paper we propose a design-oriented model for nonlinearities in short channel MOS transistors. We show that it is possible to achieve a fair accuracy in the third derivative of the drain current for short channel devices, taking into account the velocity saturation effect.**

I. Introduction

The growing demand for developing wireless communicating systems has driven CMOS technology to be applied in radio-frequency (RF) circuits, mainly in low-power battery driven portable products. Ultra-low-power CMOS circuits can be designed with MOSFETs biased in weak inversion, however, at the expense of reduced linearity. An intermediate alternative is to bias the devices in moderate inversion, a region with a good trade-off between low-power consumption, high transition frequency and high linearity [1], nevertheless, an accurate transistor model is necessary.

Distortion in short channel MOSFETs is mainly due to the current-voltage nonlinear behavior, and less due to inversion charge dynamics [2]. So, by evaluating the MOSFET nonlinear transconductance and its derivatives, it is possible to have an estimate of the distortion even for high operating frequencies. In [1], [3]–[5] expressions for MOSFET drain current and its derivatives were presented, showing that there is a linearity peak called Sweet Spot in moderate inversion. Despite their reasonable accuracy, these equations are very complex for analog and RF design.

The aim of this study is to present a set of simple and accurate equations for the nonlinear analysis of MOSFET amplifiers, particularly for operation in weak and moderate inversion. We will show that the simple model here developed gives a good approximation for the actual behavior of the drain current derivatives. The validity of the proposed model was verified by observing the distortion in common-source short channel and long channel MOSFET based amplifiers and comparing the results against measurements and SPICE simulations.

The rest of this paper is organized as follows: we show in Section II a description of the proposed model. In Section III, we provide comparisons between results obtained from measurements, from SPICE simulations and from the new model. Conclusions are finally drawn in Section IV.

II. Short-Channel Mosfet Model

Due to the continuous channel length reduction in CMOS technology, several effects related to high electrical fields are becoming more prominent and must be included in device modeling. The carrier velocity saturation is a very important effect and will be taken into account here to develop the nonlinear model. In the ACM model [6], the channel of the saturated transistor is split into two parts. One is the source side where the long-channel approximation is still valid, and the other is the drain side where the current is proportional to the charge density near the drain, given by:

$$I_{DSAT} = -W v_{lim} Q'_{IDSAT} \tag{1}$$

where I_{DSAT} is the drain current when the carrier velocity at the drain side is equal to the saturation velocity v_{lim}, W is the channel width and Q'_{IDSAT} is the charge density at the drain side. Normalizing (1) results in:

$$i_{dSAT} = \frac{2}{\zeta} q'_{IDSAT} \tag{2}$$

where $i_{dSAT} = \frac{I_{DSAT}}{I_S}$, $I_S = \frac{\mu_0 n C'_{ox} \phi_t^2 W}{2L}$ is the current normalization factor called specific current, $q'_{IDSAT} = \frac{Q'_{IDSAT}}{Q'_{IP}}$, $Q'_{IP} = -nC'_{ox}\phi_t$ is the charge density normalization factor and $\zeta = \frac{\mu_0 \phi_t}{L v_{lim}} = \frac{\phi_t}{U_{CRIT} L}$ is the velocity saturation coefficient [6]. This coefficient is the ratio of the charge velocity at the source (minimum velocity) to the velocity saturation (maximum velocity) where $U_{CRIT} = \frac{v_{lim}}{\mu_0}$. The relationship between the charge density in the drain side and the charge density in the source side is given by [6]:

$$\frac{q_{IDSAT}}{q'_{IS}} = 1 + \frac{\zeta + 1}{\zeta q'_{IS}} \left(1 - \sqrt{1 + \frac{2\zeta q'_{IS}}{(\zeta + 1)^2}} \right) \tag{3}$$

After some mathematical manipulation, (3) can be rewritten as:

$$\frac{q_{IDSAT}}{q'_{IS}} = \frac{2\zeta \left(1 + \frac{q'_{IS}}{2} \right)}{1 + \zeta(q'_{IS} + 1) + \sqrt{1 + 2\zeta(q'_{IS} + 1) + \zeta^2}} \tag{4}$$

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Given that generally $\zeta << 1$, we can simplify (4) without compromising the accuracy in weak and moderate inversion ($q'_{IS} < 10$), resulting in the following approximation [7]:

$$\frac{q_{IDSAT}}{q'_{IS}} = \frac{2\zeta\left(1+\frac{q'_{IS}}{2}\right)}{2+\zeta(q'_{IS}+1)} \tag{5}$$

From (2), (5) and from the Unified Charge Control Model (UCCM) [8], we can calculate gate transconductance for the weak and moderate operating regime by [7]:

$$g_{mg} = \frac{dI'_{DSAT}}{dV_G} = \frac{2I_S}{n\phi_t}\frac{q'_{IS}}{2+\zeta q'_{IS}}\left(\frac{4+\zeta q'_{IS}}{2+\zeta q'_{IS}}\right) \tag{6}$$

The first and second gate trasconductance derivatives calculated from (6) are respectivelly:

$$g'_{mg} = \frac{16I_S}{(n\phi_t)^2}\frac{q'_{IS}}{q'_{IS}+1}\frac{1}{(2+\zeta q'_{IS})^3} \tag{7}$$

and

$$g''_{mg} = \frac{16I_S}{(n\phi_t)^3}\frac{q'_{IS}}{(q'_{IS}+1)^3}\frac{2-2\zeta q'_{IS}-3\zeta q'^2_{IS}}{(2+\zeta q'_{IS})^4} \tag{8}$$

Notice that (6), (7) and (8) can be used to predict some figures of merit related to nonlinearities in analog circuits, such as third order intermodulation product (IP3), second order intermodulation product (IP2), and harmonic distortion.

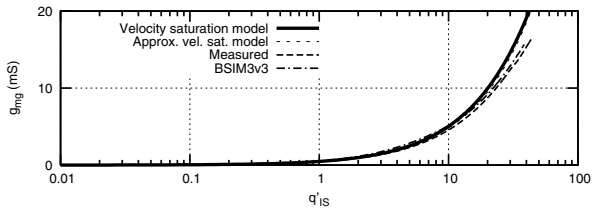
III. Results and Discussion

In order to validate the model described in the previous section, we compared the values of first, second and third drain current derivatives obtained from (6), (7), (8) with the corresponding values obtained from the exact ACM velocity saturation model equations [7] and with simulations results using BSIM3v3 MOSFET model. In addition, we measured the DC $I_D \times V_G$ characteristics of six different transistors as indicated in Table I using the high precision semiconductor analyzer Agilent 4156C. Then, we obtained the corresponding transconductance and its derivatives by numerical differentiation for comparison purposes.

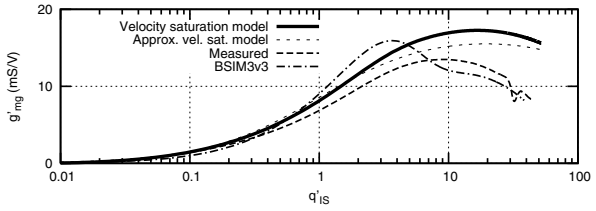
TABLE I
Dimensions, gate voltage range, and critical field of tested transistors

	Sample	L (μm)	W (μm)	V_G (V)	U_{CRIT} ($V/\mu m$)	V_{DS} ($V/\mu m$)
$0.18\mu m$	M1	0.2	2.0	$0 < V_G < 1.2$	3,86	6,00
	M2	0.4	4.0	$0 < V_G < 1.2$	3,86	3,00
	M3	2.0	20.0	$0 < V_G < 1.2$	3,86	0,60
$0.35\mu m$	M4	0.4	4.0	$0 < V_G < 2.0$	3,80	5,00
	M5	0.8	8.0	$0 < V_G < 2.0$	3,80	2,50
	M6	4.0	40.0	$0 < V_G < 2.0$	3,80	0,50

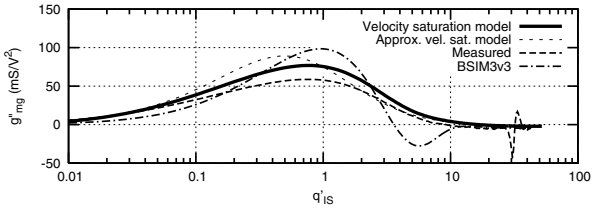
In Table I, parameter U_{CRIT} represents the electric longitudinal field for which the carrier velocity is half of v_{lim}. We have measured the transconductances and their derivatives for both long-channel and a short-channel devices. The comparison between the average electrical field and U_{CRIT} shows that the velocity saturation effect is not significant for the long-channel devices (L= 2 μm and 4 μm), but is extremely important for the short-channel transistors (L=0.2 μm and 0.4 μm). A comparison between results from measures, from the proposed model, from the original ACM velocity saturated drain current equation and from SPICE simulations is shown in Figures 1, 2, 3 and 4.



(a) g_{mg} - gate transconductance



(b) g'_{mg} - gate transconductance first derivative

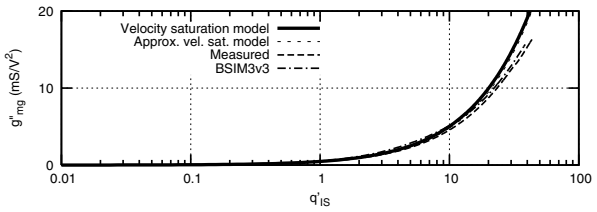


(c) $g"_{mg}$ - gate transconductance second derivative

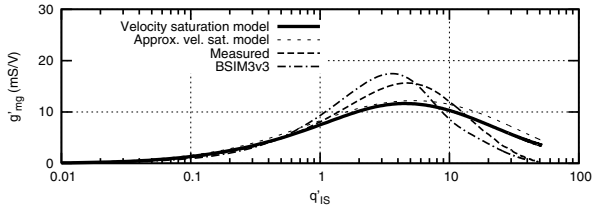
Fig. 1. Predicted, Measured and simulated transconductance and derivatives of M6

One can notice in Figures 1(a), 2(a), 3(a) and 4(a) that, for both technologies and for all transistors tested, the g_{mg} curves from the four models compare well. However, to predict nonlinearities in analog circuits, the models must give a reliable approximation for the 2^{nd} and 3^{rd} derivatives of the drain current as well. In Figures 1(b) and 3(b) one can verify that for long-channel devices (M6 and M3), the proposed model and the ACM model fits well the experimental results. In 1(b) and 4(b) for short-channel devices (M4 and M1), one can verify a consistent behavior of the proposed model and the ACM model with respect to the experimental results. On the other hand, the BSIM3v3 model exhibits for all devices, in the moderate inversion region, an abrupt change in the trend of the derivative, which is inconsistent with the experimental data.

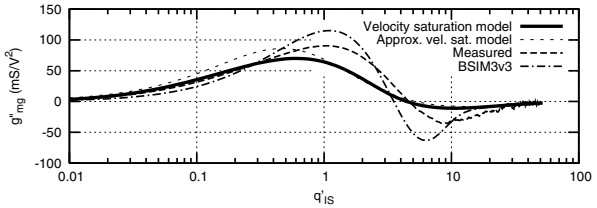
Figures 1(c), 2(c), 3(c) and 4(c) show a comparison between experimental results, the proposed model, the original ACM



(a) g_{mg} - gate transconductance

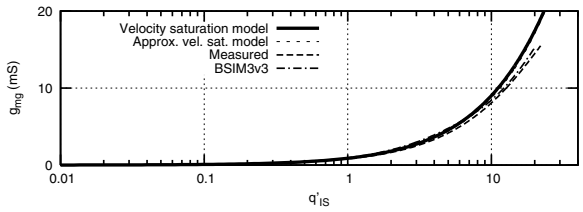


(b) g'_{mg} - gate transconductance first derivative

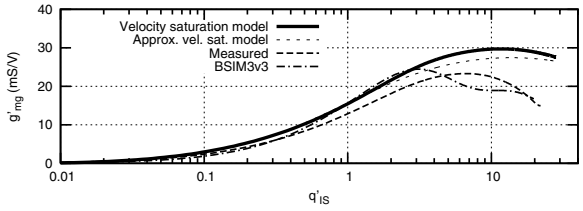


(c) $g"_{mg}$ - gate transconductance second derivative

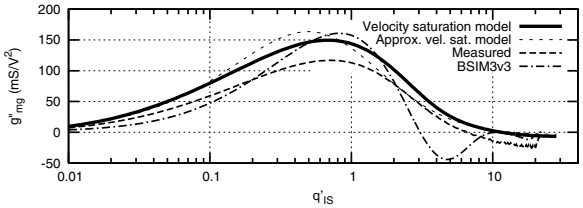
Fig. 2. Predicted, Measured and simulated M4 transconductance and derivatives



(a) g_{mg} - gate transconductance



(b) g'_{mg} - gate transconductance first derivative



(c) $g"_{mg}$ - gate transconductance second derivative

Fig. 3. Predicted, Measured and simulated M3 transconductance and its derivatives

velocity saturated equation of drain current and the BSIM3v3 model for $g"_{mg}$. Important information is contained in the zero crossing of the $g"_{mg}$ curve. This point is the so-called Sweet Spot [5]. For long-channel transistors (M3 and M6), in Figures 1(c) and 3(c), the measured results, ACM model and (8) are really close despite the fact that there is no zero crossing for the developed model, which is a consequence of neglecting second-order effects other than velocity saturation. On the other hand, the BSIM3v3 curve has a zero crossing far away from that obtained from experimental data and a much larger value for the negative peak of when compared to the experimental results.

Examining the results in Figures 2(c) and 4(c), one can observe that the proposed model, as well as the ACM model, predict with acceptably accuracy the Sweet Spot despite the fact that there is a difference between the measured results and the proposed model around the zero crossing point. It is important to recall that the developed model, as well as the ACM model, take into account the carrier velocity saturation as the only mechanism of current degradation and the measured results are sensitive to the influence of other effects such as channel length modulation and mobility degradation due to the transversal field. In order to show that the proposed model can predict with fair accuracy a nonlinearity figure of merit for RF amplifiers we chose the input-referred third-order intercept point (V_{IIP3}), which is defined as the input voltage in a two-tone test at which the extrapolated magnitude of the fundamental component of the output is equal to the extrapolated magnitude of the third-order intermodulation products of the output.

Figure 5 shows the comparison between M2 e M4. In Figure 5 it is clear that the physics based model proposed here and the measurement results corroborate with the statement made about the sweet spot above. In addition, the comparison made in Figure 5 shows the consistency of the approach used to develop the equations.

IV. Conclusion

A compact physics based model for nonlinearities in MOSFETs, including the carrier velocity saturation effect, has been presented. This model gives results consistent with the experimental data in the whole range of the applied bias. Moreover, this model shows an acceptable accuracy for predicting the Sweet Spot. The comparison with experimental results demonstrates that the principal second order effect related with the sweet spot phenomenon is the carrier velocity saturation. This statement is proved by the comparison between identical transistors built on different technologies.

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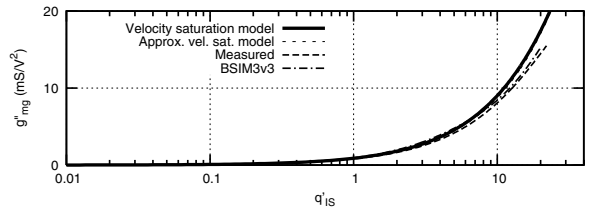
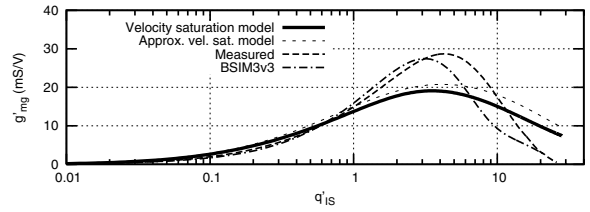
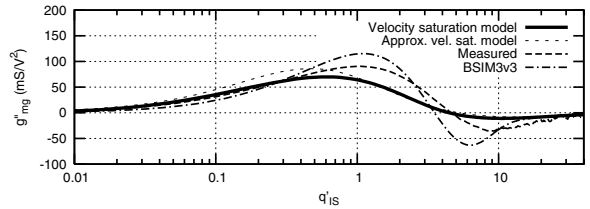


(a) g_{mg} gate transconductance



(b) g'_{mg} gate transconductance first derivative



(c) $g"_{mg}$ gate transconductance second derivative

Fig. 4. Predicted, Measured and simulated M1 transconductance and its derivatives

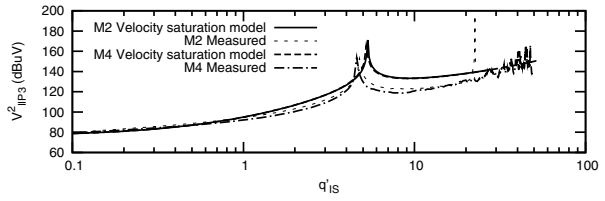


Fig. 5. V^2_{IIP3} as function of normalized source charge density for two identical short-channel transistors built on different technologies

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