A D/A converter based on a transistor-only R-2R ladder network

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Abstract - A transistor-only D/A converter based on an R-2R ladder network is presented. This type of converter can be implemented on a standard CMOS digital process and is particularly adequate to gate array implementation.

I - Introduction

With the ever increasing trend towards digital and mixed analog-digital systems, D/A and A/D converters are indispensable to interface the environment with the silicon chip. Digital-to-analog converters require some type of accurate scaling circuitry in order to provide an analog output that is a scaled version of some voltage or current reference. The scaling circuitry is commonly accomplished by the use of passive components or scaled transistors acting as current sources [1].

This paper presents a simple technique to implement digital-to-analog converters (DACs) using MOS transistors to perform both the roles of resistors [2] and switches of the conventional R-2R ladder network. This technique does not require neither passive components nor scaled transistors leading to a simple design of a compact circuit that can be realized in a CMOS digital process and, particularly, in a gate array.

II - Analysis of Series Connected Transistors

Assuming the gradual channel approximation is valid, the drain current I_D of an MOS transistor in the triode region is given [3] by

$$I_D = \frac{W}{L}[g(V_G, V_S) - g(V_G, V_D)] \qquad (1)$$

where all voltages are referred to the substrate, emphasizing the symmetry between drain and source. According to eqn. (1), two transistors with the same aspect ratio have the same DC characteristics in the triode region.

From eqn. (1), the following expression is derived for the drain current in a series association (fig. 1(a)) of two transistors [2]:

$$I_D = \frac{\left(\frac{W}{L}\right)_1 \left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1 + \left(\frac{W}{L}\right)_2} [g(V_G, V_S) - g(V_G, V_D)] \qquad (2)$$

Expression (2) shows that a series connection of two unit transistors is equivalent to a transistor that is twice longer than a unit transistor. Therefore, the drain current of two series-connected transistors is equal to one half the drain current of a single unit device with the same bias voltage. In a parallel connection of two unit transistors it is easy to verify that the drain current will be twice larger than that of a unit transistor. Hence, the parallel connection of two unit transistors is equivalent to a transistor whose aspect ratio is 2W/L. The DC characteristics of a unit transistor, two series-connected and two parallel-connected unit transistors are shown in fig. 1(b), ratifying the result presented in eqn. (2).

III - Transistor-Only R-2R Ladder Network

One of the most popular techniques to implement a D/A converter employs an R-2R ladder network, containing only two resistance values. The objective of the R-2R network is to provide a binary scale of currents.

The R-2R ladder network can be implemented with transistors performing both the roles of resistors and switches. Consider, for instance, the circuit shown in fig. 2(b), where all the transistors are identical. The basic principles presented in section II are easily applied to this network. The current entering node 4 is equally split in the two vertical branches connected to it, providing a division by two. The current entering node 3 is also divided in two equal currents by the two "equivalent" branches seen from node 3. Hence, the currents flowing into the vertical branches produce a binary scale of currents.

Therefore, the well-known R-2R ladder network [1] can be implemented with single MOS transistors without the need for linear resistors. Moreover, the current scaling of the MOSFET network does not depend on body effect and transversal mobility degradation [4].

IV - The D/A Converter

In order to validate the method presented here a 4-bit N-channel discrete prototype has been built. Fig. 2 shows the DAC scheme with linear voltage-to-current and current-to-voltage converters at the input and output. The DAC operation is very simple - a current injected at the input transistor is successively divided by two at nodes 1, 2, 3 and 4. The input word controls the MOS switches that inject the binary weighted currents in either the op amp inverting input or in the dump-line. As we can see in fig. 2, the switches also act as components of the scaling circuit, resulting in silicon area savings.

We have decided to operate the DAC in the triode region to take advantage of the better linearity in the current division [4]. All the gates are connected at V_{DD}, since the best precision in current division is obtained at high gate voltages [5]. Moreover, the high level for the CMOS logic is V_{DD}.

Compensation for thermal drifts could be achieved if the feedback transistor in the V-I converter and the linear resistors of the V-I and I-V converters were included on the chip.

V - Experimental Results and Discussion

The static characteristic of the discrete prototype built with C4007 N-channel transistors is shown in fig. 3. The converter speed will be dictated by the operational amplifier employed in the I-V converter.

The resolution of this network is limited by transistor matching, which is much better in a fully integrated implementation than in a discrete prototype. 8-bit DACs have been designed using different layout strategies and transistor sizes in order to obtain the desired matching [5].

The DAC proposed in this paper is going to be implemented in the CMOS process available in the Brazilian multiproject chip using different layout strategies.

These technique results in a very compact converter, where the number of transistors is proportional to the number of bits. Moreover, the design of the converters is simple and it can be realized in any digital CMOS process.

References

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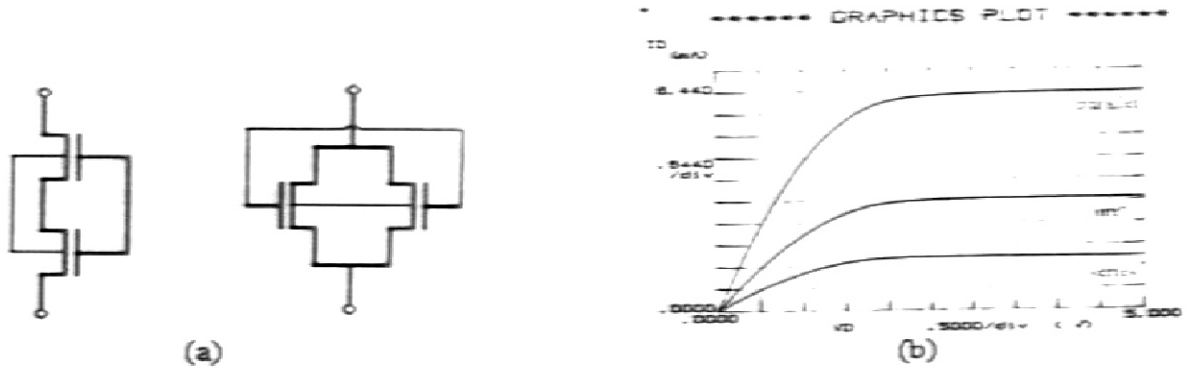

Fig. 1 - (a) series and parallel-connected transistors.
(b) DC characteristics of unit transistor, series and parallel-connected transistors.

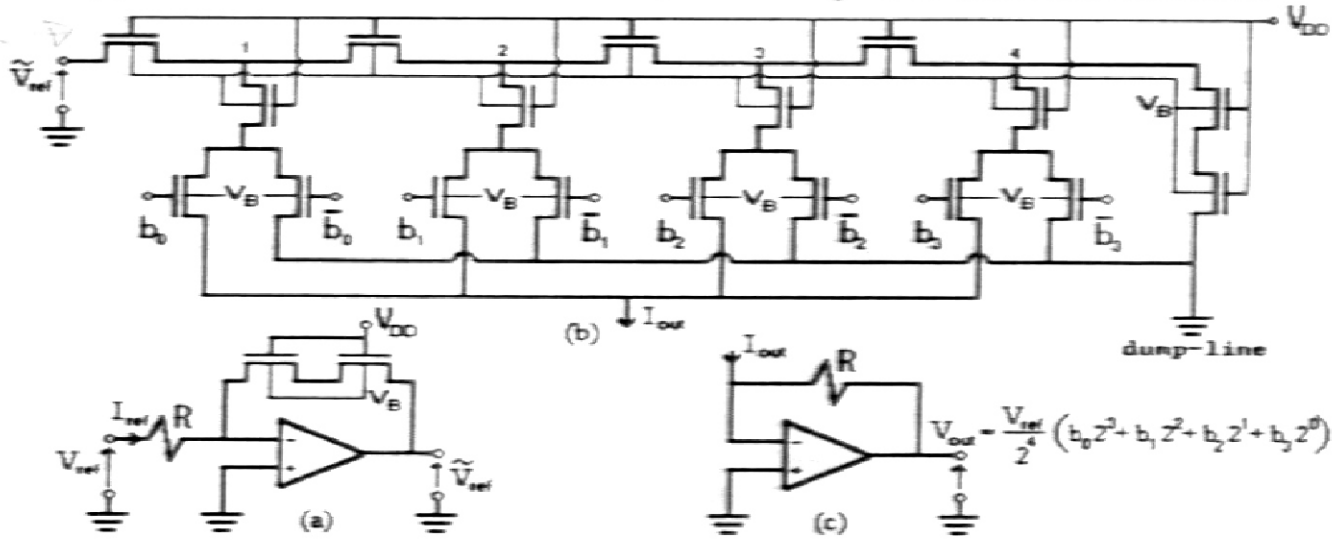

Fig. 2 - A 4-bit D/A converter using MOS current dividers.
(a) Linear input V-I converter.
(b) Current scaling network.
(c) Linear output I-V converter.

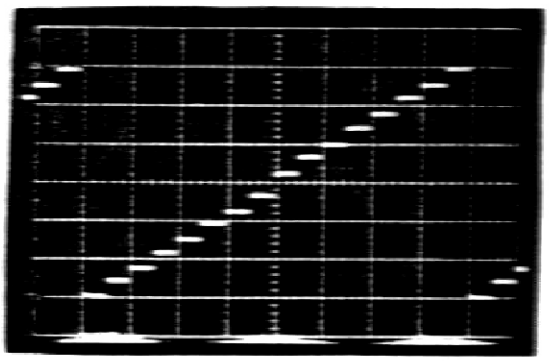

Fig. 3 - Static characteristic of the 4-bit discrete prototype.
vertical scale 0.1 V/div.