Analysis and Design of Ultra-Low-Voltage Inductive Ring Oscillators for Energy-Harvesting Applications

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***Abstract*— This paper presents inductive ring oscillators that operate from supply voltages of around two times the thermal voltage ($2kT/q$), for energy-harvesting applications. Expressions for the oscillation frequency as well as the minimum transistor gain and supply voltage required for the start-up oscillations are derived. The ring oscillators were built with zero-VT transistors due to their high drive capability at low voltages. Measurement results obtained in a ring oscillator prototype integrated in a 130 nm technology confirmed operation of the oscillator with 53 mV of supply voltage.**

***Index Terms* — MOSFET analog circuits, ultra-low-voltage, energy harvesting, zero-VT transistor, ring oscillator.**

I. INTRODUCTION

Emerging applications such as wireless sensor networks and wearable devices used for medical, lifestyle or entertainment purposes require energy autonomy. Harvesting power from the environment using a thermoelectric generator (TEG) and photovoltaic cells is an important way to address these recent applications and is suitable for body-environment applications. Body-worn TEGs typically generate voltages as low as 50 mV whereas a photovoltaic cell provides voltages of around 100 mV in dark rooms [1]. Another interesting voltage source is provided by trees, which can generate voltages ranging from 50 mV to 200 mV [2]. In general, all these power sources need a boost converter for the proper operation of electronic circuits.

In a recent study, DC-DC boost topologies [1], [3], [4], such as that shown in Fig. 1, have been used to increase the very small voltage level from low-voltage sources. A major design challenge due to the extremely low-voltage supply is to generate oscillations to turn on and off the MOS switch. Some start-up solutions have recently been proposed, such as the use of previously charged capacitors or batteries [3], the use of mechanical switches [4], or the use of an oscillator tuned after fabrication which operates from voltages above 90 mV [1]. However, a fully-integrated solution which can start up from around 50 mV is not yet available.

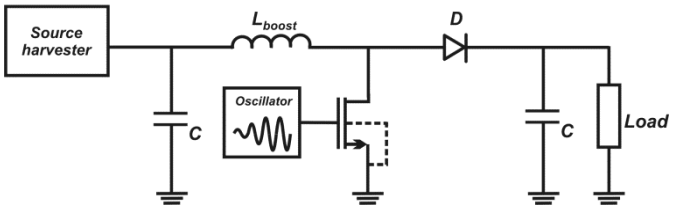

Figure 1. Boost DC-DC converter topology used in energy harvesting applications.

In this study we developed an ultra-low-voltage (ULV) oscillator in order to control the operation of DC-DC boost converters. The analysis and design of inductive oscillators based on the ring topology were carried out. Experimental results using a 130 nm technology proved that the oscillator can operate with supply voltages of 53 mV.

Zero-threshold voltage (zero-VT) MOS transistors were employed as the active devices of the oscillators. This transistor, which is suitable for ULV analog circuits due its high drive capability and sufficient voltage gain at low voltages, provides the necessary gain for oscillation from a very low supply voltage.

This paper is organized as follows. The inductive ring oscillator topology is presented in Section II. Analysis considering the oscillation frequency and minimal voltage supply is given in Section III. Experimental results for an integrated seven-stage oscillator are reported in section IV. Section V concludes the paper.

II. THE INDUCTIVE RING OSCILLATOR TOPOLOGY

Starting up a conventional ring oscillator with a power supply $V_{DD,min}$ below 100 mV is extremely difficult [5]. The magnitude of the $V_{DD,min}$ is usually limited by the imbalance of the threshold voltage V_T of PMOS/NMOS transistors of the logic inverter caused by within-die and die-to-die variations [5]. In order to reduce the $V_{DD,min}$ of the conventional ring oscillator, one can use the inductive ring oscillator topology shown in Fig. 2 [9]. This topology, which replaces the active load PMOS of the logic inverters with an inductor, can not only reduce the $V_{DD,min}$ but may also boost the oscillation amplitude beyond the supply rail.

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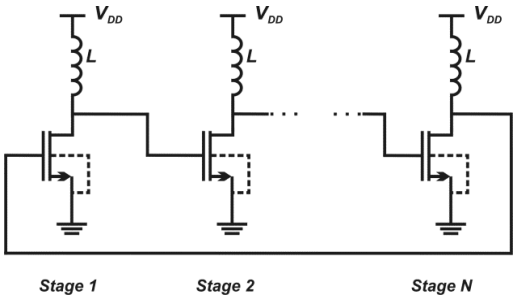

Figure 2. Schematic diagram of an N stage inductive ring oscillator [9].

III. ANALYSIS

The circuit of a single stage of the inductive ring oscillator as well as its small-signal model is shown in Fig. 3 where g_m and g_{md} represent the gate and drain transconductances, respectively, C_{gd} is the gate-drain capacitance, C is the sum of all capacitances between the drain node and the ac ground, and G_P models the inductor loss.

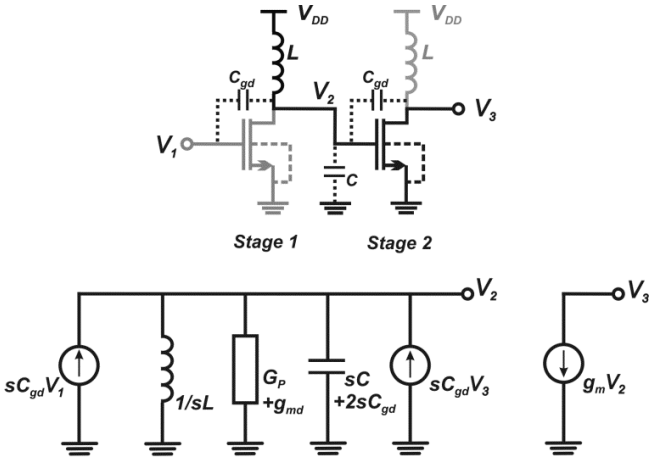

Figure 3. Single stage of the inductive ring oscillator and its corresponding small signal model.

When the ring structure is oscillating, the phase shift ϕ between two adjacent stages is given by $\phi=2k\pi/N$. N is the number of stages and k is an integer number.

Considering that the voltage nodes in Fig. 3 are related in the form $V_2=V_1e^{j\phi}$ and $V_3=V_2e^{j\phi}$, we can redraw the small-signal circuit of Fig. 3 as shown in Fig. 4. The transfer function of the single stage is given by

$$\frac{I_{out}}{I_{in}}(s)=-\frac{g_m}{g_{md}+G_P+\frac{1}{sL}+sC_T} \tag{1}$$

where $C_T=C+2C_{gd}(1+cos\ \phi)$. It is possible to show that, except for N=2 and 4, more than one value of the phase shift for the transfer function given by (1) satisfies the phase condition required for oscillation. However, as explained in [6], the circuit will oscillate at the frequency for which the gain stage is higher. In the case of an even number of stages we have $\phi=\pi$, while for the case of an odd number of stages $\phi=(N-1)\pi/N$.

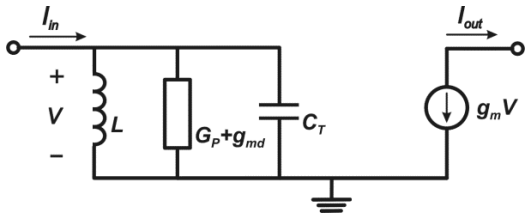

Figure 4. Small-signal model equivalent to a single stage of the inductive ring oscillator.

A. Frequency of oscillation

Once the number of stages of the oscillator is determined, the phase-shift between two adjacent stages is known; therefore, from (1), we can calculate the oscillation frequency ω as

$$\frac{\omega}{\omega_o}=\sqrt{1+\frac{(\tan\phi)^2}{4Q^2}}-\frac{\tan\phi}{2Q} \tag{2}$$

where $\omega_o=1/\sqrt{LC_T}$, is the equivalent LC resonant frequency of a single stage, and Q is the quality factor, $Q=1/(g_{md}+G_P)\omega_0L$. Note that when the condition $\phi=\pi$ holds, which is the case for an even number of stages, ω equals ω_0.

The dispersion relation of a stage, which shows the dependence of ω/ω_0 on ϕ, is shown in Fig. 5. It is clear that, for $Q>100$, we have $\omega/\omega_0\cong1$.

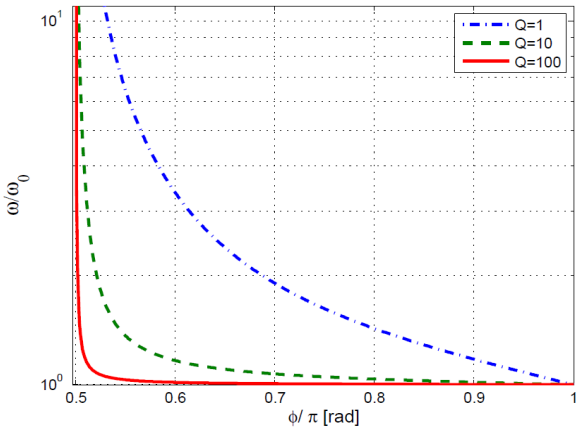

Figure 5. The dispersion relation of one stage of the inductive ring oscillator for different quality factors. ω normalized by ω_0 and ϕ normalized by π.

B. Minimum transistor gain required for oscillation start-up

In order to oscillate, the minimum loop gain of the N stage oscillator can be obtained from (1) as

$$\left(-\frac{g_m}{g_{md}+G_P}\right)^N\frac{1}{(1-j\tan\phi)^N}=1 \tag{3}$$

Since the relation between source, drain, and gate transconductances, g_{ms}, g_{md}, and g_m, respectively, is $g_m=(g_{ms}-g_{md})/n$ [7], where n is the transistor slope factor, the minimum transistor gain g_{ms}/g_{md} required for oscillation is obtained from (3) as

$$\left.\frac{g_{ms}}{g_{md}}\right|_{\min} = 1 + n\sqrt{1+(\tan\phi)^2}\left(1+\frac{G_P}{g_{md}}\right) \quad (4)$$

C. Minimum supply voltage required for oscillation start-up

From the MOSFET model described in [7] and the condition given by (4), it is possible to calculate the minimum supply voltage required to start up the oscillator. Thus, considering the expression for the drain-source voltage (V_{DS}), as [7]

$$V_{DS} = \frac{\phi_t^2}{2I_S}\left(g_{ms} - g_{md}\right) + \ln\frac{g_{ms}}{g_{md}} \quad (5)$$

and noting that for each transistor of Fig. 2 we have the following dc values V_S=V_B and V_G=V_D=V_{DD}, from (4) the minimum supply voltage required to start up the oscillator can be written as

$$\begin{aligned} V_{DD}\big|_{\min} &= \frac{\phi_t^2}{2I_S} n\left(g_{md}+G_P\right)\sqrt{1+(\tan\phi)^2} \\ &+\phi_t \ln\left[1+n\sqrt{1+(\tan\phi)^2}\left(1+\frac{G_P}{g_{md}}\right)\right] \end{aligned} \quad (6)$$

Assuming that the transistor operates in weak inversion and that the inductor losses are negligible, the voltage supply limit of (6) is given by

$$V_{DD}\big|_{\lim} = \phi_t \ln(1+n) \quad (7)$$

for the case of an even number of stages. Assuming that n=1, the limit given by (7) is around 18 mV at room temperature. This limit shows that the circuit can theoretically operate with one half the value of the Meindl limit [8] of digital circuits, which for a CMOS inverter under the same conditions is 36 mV. This result was to be expected since the condition required for oscillation of a ring oscillator with an even number of stages (loaded with an infinite-Q tank) is that the gain of the transistor equals unity. The unity gain of a transistor operating in weak inversion is obtained for a power supply of 18 mV at room temperature.

D. Verification of the analysis

Figure 6 shows the simulated (for sustained oscillations) and calculated (for oscillation start-up) minimum supply voltage in terms of the number of stages for the oscillator in Fig. 2, using a 130 nm technology. The oscillators were built with zero-VT transistors (W/L=250 µm/0.42 µm) and inductors for which L≈100 nH and Q≈8 @ 500 MHz. The calculated results were obtained from (6).

IV. Experimental Results

We designed a seven-stage inductive ring oscillator using zero-VT transistors. The micrograph of the circuit implemented in a 130 nm technology is shown in Fig. 7. In order to obtain some idea of the practical behavior of the zero-VT transistor designed the source and drain transconductances were experimentally determined for V_{DD} ranging from 0 to 100 mV, as shown in Fig. 8. The bias condition was V_S=V_B=0 and V_G=V_D=V_{DD}.

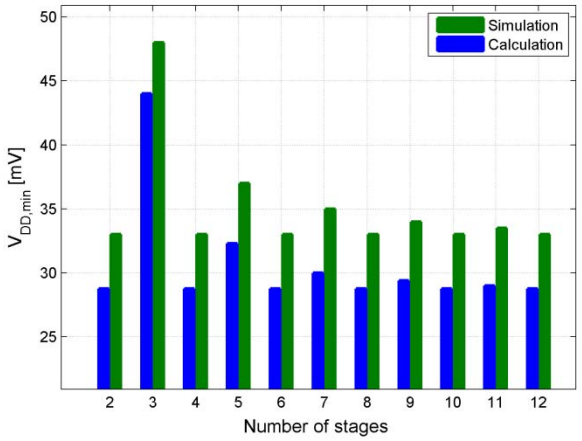

Figure 6. Calculated and simulated $V_{DD,min}$ vs. number of stages N of the oscillator in Fig. 2 using a 130 nm technology.

Figure 7. Micrograph of the seven-stage inductive ring oscillator in a 130 nm technology.

A summary of the characteristics of the zero-VT transistor (W/L=150 µm/0.48 µm) and the inductor used in the oscillator is given in Table I. The inductor was chosen so that the G_P value was as low as possible within the expected frequency range (500 to 800 MHz).

Table I. Main characteristics of the inductor (@ 550 MHz) and transistor (V_{DD}=40 mV) used in the integrated inductive ring oscillator.

Transistor		Inductor
g_{md}^{*} = 2.3 mA/V	C = 130 pF	L = 100 nH
V_T^{*} = 22 mV	C_{gd} = 70 pF	G_P = 0.3 mA/V

* Value obtained experimentally

Using the values shown in Table I, the oscillation frequency calculated from (2) is around 1 GHz, against 730 MHz obtained using the simulator. In fact, the parasitic capacitances introduced by a poor layout contributed to reducing the oscillation frequency to 550 MHz, as the experimental spectral diagram in Fig. 9 shows.

The minimum voltage required to start up the oscillator obtained with the experimental prototype was around 53 mV, against 50 mV calculated using (6) and the values of Table I. The minimum V_{DD} for sustained oscillations of the seven-stage oscillator, 53 mV, is considerably higher than the value of 20 mV in reference [10], but it is worth noting that the Colpitts oscillator in [10] uses high-quality off-the-shelf components whereas the oscillator presented here is fully integrated.

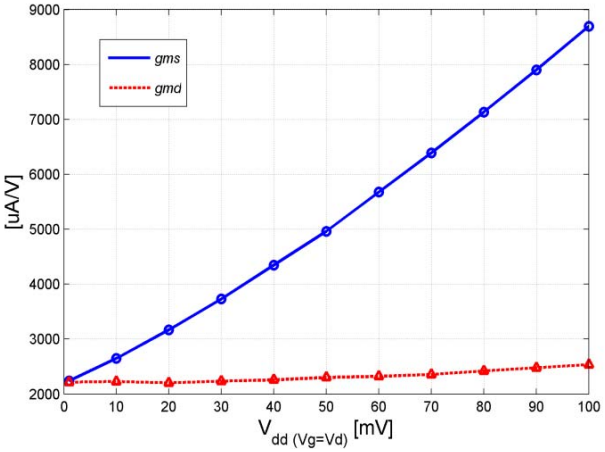

Figure 8. Experimental drain and source transconductances of the zero-VT transistor (W/L=150 µm/0.48 µm) for V_S=V_B=0 and V_G=V_D=V_{DD}.

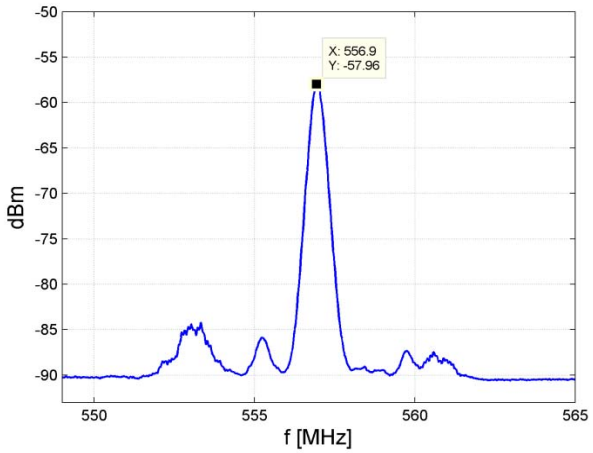

Figure 9. Spectral diagram of the seven-stage inductive ring oscillator, obtained experimentally for V_{DD}=70 mV.

The variation in the output voltage magnitude with the supply voltage variation is shown in Fig. 10, for both experimental and simulation results. Note that the output voltage is normalized to its value at a supply voltage of 100 mV.

V. CONCLUSIONS

In this paper we have presented an ultra-low-voltage inductive ring oscillator topology. Analysis considering the start-up conditions and the fundamental voltage supply limit shows that the topology is suitable for energy harvesting applications such as DC-DC converters operating from very low voltages. The topology functionality was verified through experimental results for a 130 nm CMOS seven-stage oscillator that can operate with supply voltages as low as two thermal voltages ($2kT/q$).

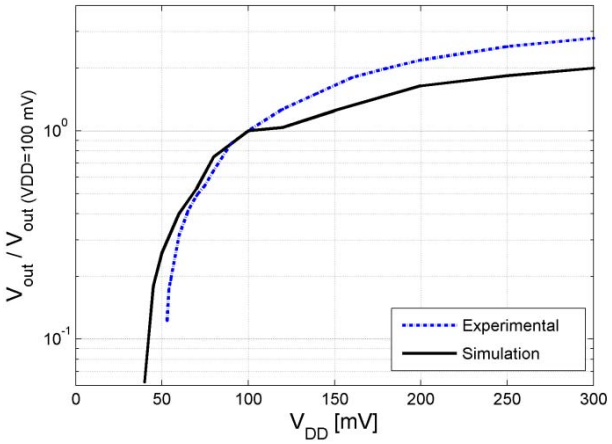

Figure 10. Normalized output voltage of the 7 stage inductive oscillator vs. supply voltage.

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