A MOSFET MODEL FOR LOW POWER ANALOG IC DESIGN

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Abstract

The subject of this paper is a MOSFET model that is valid from weak to strong inversion. Simple and continuous expressions have been derived from basic MOSFET equations. The key variable of the model is the current. Simple expressions for both the transconductance-to-current ratio, the saturation voltage and the cutoff frequency in terms of the inversion level have been included in the paper. A design of a common source amplifier is presented to illustrate the application of the model.

Introduction

Power consumption is currently the main issue for battery-operated systems such as electronic watches, implanted biomedical devices and other small size portable instruments [1]. Typical current consumption is below the μA range for a voltage operation between 1V and 3 V. At these current levels the MOS transistors generally operate in the weak and moderate inversion regions. Therefore, a MOSFET model which extends from low to high current levels is needed for analysis and design of high performance integrated circuits (IC). The desirable properties of this MOSFET model [2,3] can be summarized as follows: (i) it should be physics-based; (ii) it should consist of single-piece, continuous and accurate expressions; (iii) it should have as few parameters as possible; (iv) it should preserve the source-drain symmetry of the transistor. Particularly, analog IC designers need simple expressions to compute transistor dimensions for any current level. The model introduced in [4] satisfies the above mentioned properties. This paper extends the results of [4] and provides a set of accurate and universal expressions for analysis and design of ICs. These expressions can be employed for any process, bias voltages or transistor dimensions. In these expressions, the current is the key variable and a normalization current is the main parameter to be determined.

Drain current to transconductance ratio

The fundamental approximation presented in [4] is the linearization of the inversion charge density Q_I' with respect to the surface potential ϕ_S:

$$dQ_I' = (C_{ox}' + C_b')d\phi_S = nC_{ox}'d\phi_S \tag{1}$$

In (1) n is the slope factor, between 1 and 2, which is slightly dependent on the gate voltage. C_{ox}' and C_b' are the oxide and bulk capacitances per unit area. The drain current is obtained by substituting (1) into the following expression [5, p. 109]:

$$I_D = \mu W\left(-Q_I'\frac{d\phi_S}{dx} + \phi_t\frac{dQ_I'}{dx}\right) \tag{2}$$

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where the first term in the right hand side is the drif current and the second one is the diffusion current. Integrating along the channel length results in

$$I_D = I_F - I_R \tag{3a}$$

$$I_{F(R)} = \frac{\mu W}{C'_{ox} L}\left(\frac{Q'^2_{IS(D)}}{2n} - C'_{ox}\phi_t Q'_{IS(D)}\right) \tag{3b}$$

The drain current has been decomposed into a forward current I_F and a reverse current I_R [3]. These currents depend on the inversion charge densities Q'_{IS} and Q'_{ID} at the source and drain ends of the channel. In saturation, $I_F >> I_R$ and $I_D \cong I_F$. In the triode region both components of the drain current should be taken into account.

Combining (3b) and the definition of the source transconductance [3,4],

$$g_{ms} = -\mu Q'_{IS} W / L \tag{4}$$

leads to an expression for the current to source transconductance ratio:

$$\frac{I_F}{\phi_t g_{ms}} = \frac{1+\sqrt{1+i_f}}{2} \tag{5a}$$

where

$$i_f = \frac{I_F}{I_S} \quad (5b) \qquad \text{and} \qquad I_S = \mu \frac{W}{L} n C'_{ox} \frac{\phi_t^2}{2} \quad (5c)$$

i_f is the forward normalized current or inversion coefficient [3], and I_S is the normalization current or specific current, which depends on technology ($\mu n C'_{ox}$), geometry (W/L), gate voltage (μ, n)and temperature (ϕ_t, μ).

Eqn. (5a) is a universal characteristic of MOSFETs that is independent of technology, geometry, gate voltage and temperature. Thus, plots of (5a) should coincide for all MOSFETs as long as the normalization current is correctly determined.

Figs. 1 to 3 show the plots of the current to transconductance ratios for N and P-channel transistors, transistors with different geometries and different gate voltages. The measurements confirm the theoretical expression (5a).

Let us compare now the difference between a bipolar design and an MOS design. Recall that for the bipolar transistor $I_C/g_m\phi_t=1$. Thus, the collector current is determined as long as the transconductance is specified. On the other hand, for MOSFETs, we can choose either the inversion coefficient or the drain current, according to (5a), to meet the design requirements for g_{ms}.

The intrinsic cutoff frequency

The intrinsic cutoff frequency ω_T is defined as the unit current gain frequency of the common source configuration [5]. For the intrinsic transistor in saturation ω_T is given by:

$$\omega_T = \frac{g_{mg}}{C_{gs} + C_{gb}} \tag{6}$$

An expression for ω_T can be readily obtained from the results in Appendix A and recalling that, in saturation, $g_{mg}=g_{ms}/n$ [3,4]:

$$\omega_T = \frac{g_{mg}}{C_{gs}+C_{gb}} = \frac{\mu\phi_t}{L^2}\frac{n i_f\left(1+\sqrt{1+i_f}\right)}{(n-1)\left(1+\sqrt{1+i_f}\right)^2+\frac{2}{3}\left(i_f+\sqrt{1+i_f}-1\right)} \tag{7}$$

Plots of ω_T vs. i_f are shown in Fig. 4. Note that the sensitivity of ω_T to n is low, specially in the moderate and strong inversion regions (i_f>1).

The saturation voltage

Let us define the drain saturation voltage V_{DSAT} in the long-channel transistor as the voltage for which the ratio of the reverse current to the forward current $I_R/I_F=\varepsilon<<1$, say, $\varepsilon=0.01$. Assuming the inversion charge density is given by (B3) in Appendix B and using (3b) we have the following expression for V_{DSAT}:

$$V_{DSAT} = V_S + \phi_t \ln\left(\frac{exp\left(\sqrt{1+i_f}-1\right)-1}{exp\left(\sqrt{1+\varepsilon i_f}-1\right)-1}\right) \tag{8}$$

Fig. 5 shows the plot of the drain saturation voltage vs the inversion coefficient. Note that for weak inversion $V_{DSAT}=V_S+\phi_t ln(1/\varepsilon)$ and for strong inversion $V_{DSAT}\propto\sqrt{i_f}$.

Design of a common source amplifier

In the common source amplifier shown in Fig. 6 the current source is assumed to be ideal. C is the load capacitance, g_d is the output conductance and g_{mg} is the gate transconductance. Replacing the output conductance by the ratio I_D/V_A (V_A is the Early voltage), the voltage gain and the gain-bandwidth product are given by $A_V=-(g_{ms}/nI_D)V_A$ and $GBW=g_{mg}/2\pi C$, respectively. Note that the voltage gain is proportional to the ratio g_{ms}/I_D. Moreover, this ratio indicates the conversion efficiency from current (power) to transconductance. Since a compromise between power consumption, silicon area and low frequency gain is usually desirable, this voltage gain expression is useful for design.

As a design example, assume GBW and C are known. Therefore, the bias current and the transistor aspect ratio have to be determined. The minimum value of the inversion coefficient, i_{fmin}, can be readily determined from (7) for $f_{Tmin}=3GBW$ [6]. For each value of $i_f \geq i_{fmin}$ the bias current I_F is computed from (5a) while the aspect ratio is computed from:

$$\frac{W}{L} = \frac{g_{ms}}{\mu n C'_{ox}\phi_t}\frac{1}{\sqrt{1+i_f}-1} \tag{9}$$

As an example, consider the same specifications as in ref. [7]: GBW=10 MHz, C=10pF, $\mu C'_{ox}$=80μA/V^2. Aditionally, assume n=1.35, μ=500 cm^2/Vs and L=2μm. From (7), i_{fmin}=0.4. From (5a), I_{Fmin}=24 μA and $(W/L)_{max}$=1650, according to eqn. (9). Table 1 shows the results obtained using the new model and those from [7, 8]. It can be readily noticed that our analytic formulation leads to results that almost coincide with those obtained in [7, 8].

Conclusions

A physics-based law for the I/g_m ratio in MOSFETs has been derived and experimentally verified. An expression for the drain saturation voltage for any inversion level has been

included here. Finally, we presented a simple methodology for the design of basic analog stages based on the dependences of ω_T and $1/gm$ on the inversion coefficient i_f.

References

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APPENDIX A

A general expression for C_{gs} is given in ref. [4]:

$$C_{gs} = \frac{2}{3}\frac{WL}{n}\left(1 - \frac{Q_R'^2}{\left(Q_F' + Q_R'\right)^2}\right)D_F' \tag{A1}$$

where

$$Q_{F(R)}' = Q_{IS(D)}' - nC_{ox}'\phi_t \tag{A2}$$

and

$$D_F' = \left.\frac{\partial Q_{IS}'}{\partial V_S}\right|_{V_G} \tag{A3}$$

The differentiation of eqn. (3b) with respect to V_S together with eqn. (4) results in:

$$D_F' = nC_{ox}'\frac{Q_{IS}'}{Q_{IS}' - nC_{ox}'\phi_t} \tag{A4}$$

Recall that in saturation $I_F >> I_R$. The substitution of eqn. (A4) into eqn. (A1) and eqn. (3b) allow us writing the gate-to-source capacitance in saturation:

$$C_{gs-sat} = \frac{2}{3}C_{ox}\frac{i_f + \sqrt{1+i_f} - 1}{\left(1+\sqrt{1+i_f}\right)^2} \tag{A5}$$

The gate-to-bulk capacitance is calculated from [4]

$$C_{gb-sat} = \frac{n-1}{n}\left(C_{ox} - C_{gs-sat}\right) \tag{A6}$$

APPENDIX B

From the gate charge conservation equation [5, p. 79] it is easy to prove that for constant gate to bulk potential V_{GB}:

$$\left.\frac{d\phi_S}{dV_{CB}}\right|_{V_{GB}} = \frac{C_i^{'}}{C_i^{'} + C_{ox}^{'} + C_b^{'}} \tag{B1}$$

where ϕ_S is the surface potential, V_{CB} is the channel voltage, and $C_i^{'}$, $C_{ox}^{'}$ and $C_b^{'}$ are the inversion, oxide and depletion capacitances per unit area, respectively [4].

From (1) and (B1) we obtain:

$$\frac{dQ_I^{'}}{dV_{CB}} = \frac{\left(C_{ox}^{'} + C_b^{'}\right)C_i^{'}}{C_{ox}^{'} + C_b^{'} + C_i^{'}} = n\frac{C_i^{'}}{1 + C_i^{'}/C_{ox}^{'}} \tag{B2a}$$

where $C_C^{'} = C_b^{'} + C_i^{'}$ is the so-called semiconductor capacitance per unit area.

Eqn. (1), (B1), (B2a) are equivalent to the small signal model shown in Fig. B1.

Assuming that the expressions for $C_b^{'}$ and $C_i^{'}$ are

$$C_b^{'} = (n-1)C_{ox}^{'} \quad \text{(B2b)} \qquad \text{and} \qquad C_i^{'} = C_{ox}^{'}(n-1)e^{\frac{V_P - V_{CB}}{\phi_t}} \quad \text{(B2c)}$$

the integration of (B2a) leads to

$$Q_I^{'} = -nC_{ox}^{'}\phi_t\, ln\left(1 + \frac{n-1}{n}e^{\frac{V_P - V_{CB}}{\phi_t}}\right) \tag{B3}$$

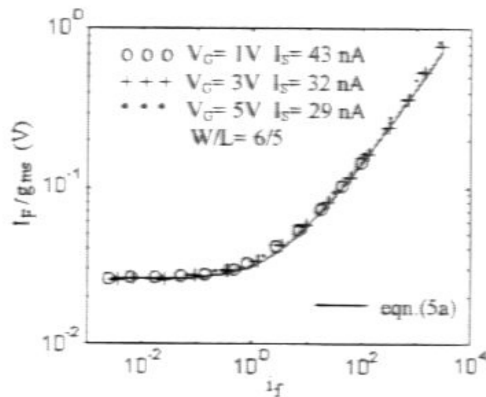

Figure 1- Drain current/transconductance vs inversion coefficient for different gate voltages.

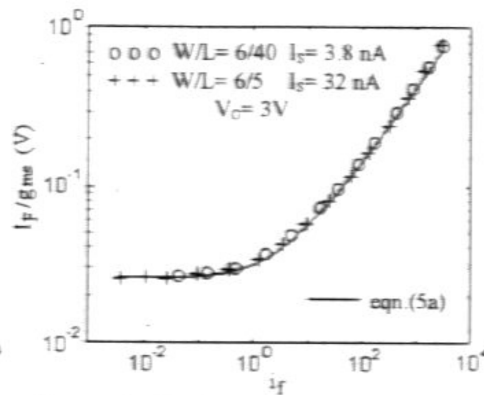

Figure 2- Drain current/transconductance vs. inversion coefficient for different aspect ratios.

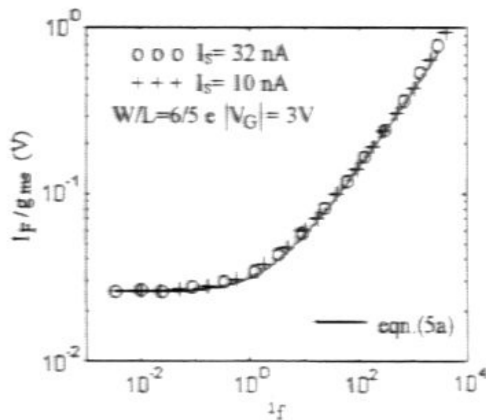

Figure 3- Drain current/transconductance vs. inversion coefficient for N (ooo) and P (+++) channel transistors.

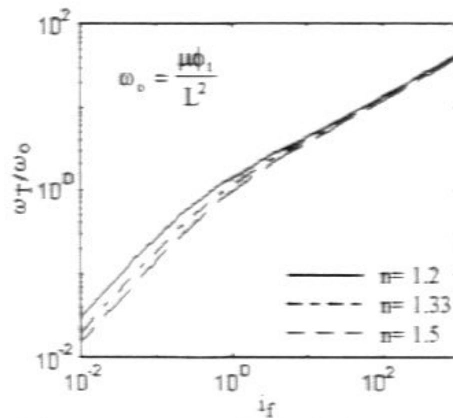

Figure 4- Normalized intrinsic cutoff frequency vs. inversion coefficient.

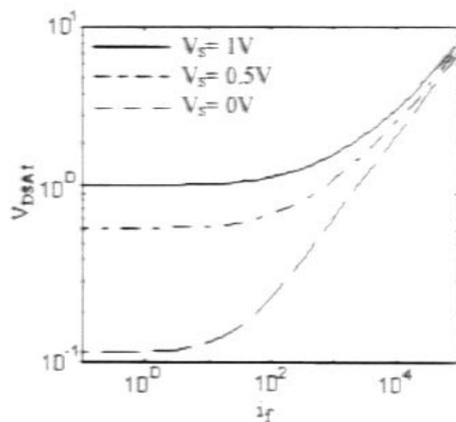

Figure 5- Drain saturation voltage (ε=0.01) vs. inversion coefficient.

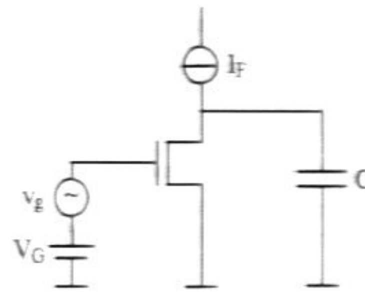

Figure 6- Common source amplifier.

W/L	i_f [eqn.(9)]	I_F (μA) [eqn.(5a)]	I_F (μA) [7, 8]
500	1.57	29	30
200	5.30	39	41
100	15.2	55	58
50	48.6	88	91
20	258	188	190

Table I- Drain current and aspect ratio vs inversion coefficient.

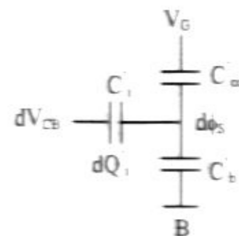

Figure B1 - Small-signal model for the three terminal MOSFET.