A Programmable Low Voltage Switched-Current FIR Filter for Disk Drive Equalization

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Abstract

In this paper we describe a 20MHz sample rate switched-current Finite Impulse Response (FIR) filter, suitable for equalizer architectures. The basic cell of the FIR filter is the switched-current (SI) sample-and-hold (S/H) circuit proposed in [1], appropriate for low voltage operation. The programmability of the FIR filter structure is achieved via Mosfet Only Current Dividers (MOCD) [2]. The FIR filter has been designed using the AMS 0.8u CMOS process parameters. The power consumption per tap is 12mW at 3V power supply.

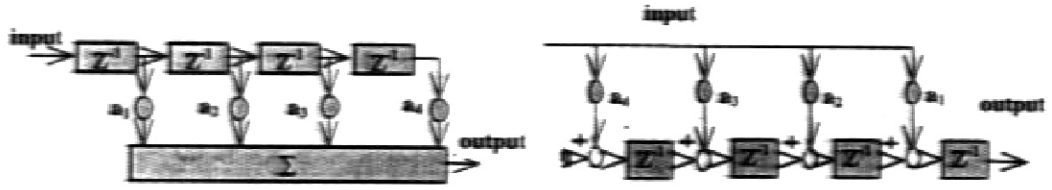
I - *Introduction*

Generally, in the disk-drive Partial Response signaling with Maximum Likelihood detection (PRML) [3, 4], the forward equalizer and the feedback equalizer are used to eliminate the Intersymbol Interference (ISI) before and after each symbol, respectively. The ISI limits the speed of many communication systems and the density of many storage systems. In all equalizer circuits, the FIR filter is used to compensate the interface error. This paper presents a programmable switched-current FIR filter which is suitable for low voltage operation. The FIR filter is based on a circular delay line architecture [5]. This paper is divided into three parts. Section II is a revision of the FIR filter realizations: direct, transposed and circulating structures. The switched-current realization and simulation of the FIR filter structure are presented in section III. Section IV summarizes the conclusions about this paper.

II - *FIR filter structures*

Traditional designs of analog FIR filters use a direct form structure due to its simplicity (Fig. (1.a)). The main problem in this structure is the multiple input summer which limits the operating speed. To overcome this problem, the transposed form (Fig. (1.b)) has been proposed [6]. As shown in this figure, the output summation block of the direct form was replaced by two-input summers at the input of each delay cell. The overall transfer function of the transposed form is exactly the same as of the direct form, and is given by

$$H(Z) = a_1 Z^{-1} + a_2 Z^{-2} + a_3 Z^{-3} + a_4 Z^{-4} \qquad (1)$$



(a) Block diagram of a direct-form FIR filter. *(b) Block diagram of a transposed FIR filter.*

Fig. 1- The different block diagrams of the FIR filter realization.

The disadvantage of this structure is that the input drives N multipliers (number of taps) and, consequently, the input (master) S/H amplifier must drive a large load. To avoid this problem, the transposed structure can be modified, as shown in [6].

In the traditional forms (direct or transposed forms) of the FIR filter structure, the signal is moved from one memory cell to the next on each clock cycle, resulting in an analog delay line. In the analog delay line

structure, errors such as noise and offset are accumulated up to the ultimate tap. To avoid this drawback of the analog delay line, the circular FIR structure [5] has been proposed (Fig. 2). The signal flow through the FIR filter is described as follows :

- During the first clock cycle, the sampled value (sample- hold 1) is the input to multiplier "a_1", which corresponds to the first coefficient in equation 1.
- In the second clock cycle, the stored value is NOT moved to next delay cell (sample-hold 2), but is the input to the second multiplier, "a_2" (a_2Z^{-2}), as shown in Fig 2 .

Therefore, the FIR filter can be constructed with delay elements connected in parallel. Fig. 2 can be extended to an N tap circulating FIR filter. The multiplexing process continues on each clock cycle thus cycling the input data through all the tap weight multipliers. This process simulates a tapped delay line without passing the sampled value into series delay elements on each clock cycle. Consequently, this structure has the advantage of avoiding the propagation of offset voltage and noise from each cell to the following.

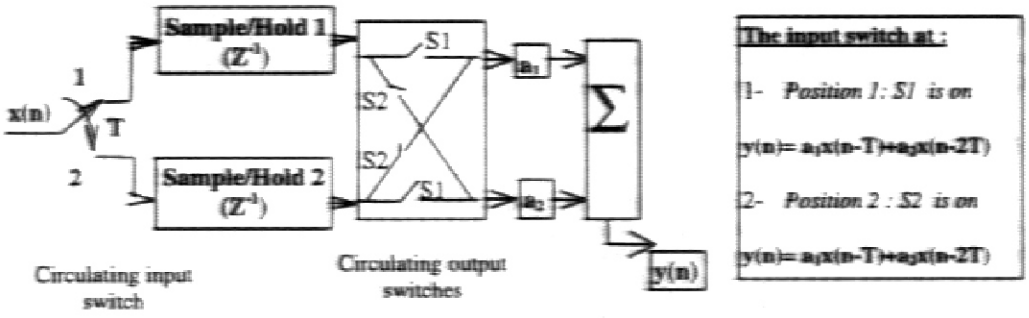


Fig. 2- Second order circular FIR filter structure.

III- *The Switched-Current Realization of the Circular FIR Filter*

(III-1) The sample-and-hold circuit

The sample-and-hold circuit can be built as a switched-capacitor (SC) integrator with zero initial condition at each clock cycle. In the SC technique, the op amp design is relatively complicated due to the change of the load capacitance in each clock phase. Programmable SC circuits (S/H, integrator and filters) require capacitor arrays, which occupy a large active area compared with the binary weighted transistor array and the MOCD structures in the SI technique. Moreover, in the switched-current technique [1, 7], the complete delay element is realized as a cascade of two half delay cells, as shown in Fig. 3.

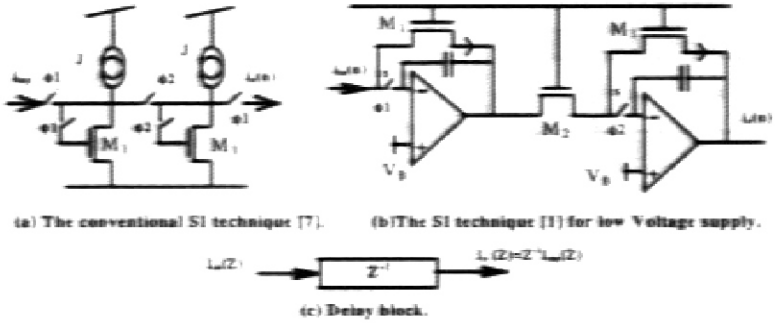


Fig. 3- Delay implementation in SI technique.

Therefore, for the SI implementation of both the direct and transposed realizations, two half delay cells must be used. So, for an N-tap FIR filter, 2N op amps (two current sources in the conventional SI technique)

have to be used. However, in the circular FIR filter realization form, we can use only one half delay cell to implement a complete delay element which means that the total power consumption and total active area will be reduced by about 50% with respect to direct and transposed SI implementations. Also, the circular structure has only one tap connected to the input S/H (master S/H) at each clock cycle, thus avoiding multiple loads at the input. The circulating structure needs a multiple-input summer, as shown in Fig. 2. But generally, in current mode process, the summation is performed by tying all terminals (summer inputs) together.

In this work, the technique for switched-current (SI) circuits proposed in [1, 8] will be used. This SI technique avoids the conduction gap [9] by properly biasing the switches. Therefore, it is more suitable for low voltage applications than the conventional SI technique [7]. In this switched-current method, the current is processed in two steps, as can be readily observed from Fig. (3.b):

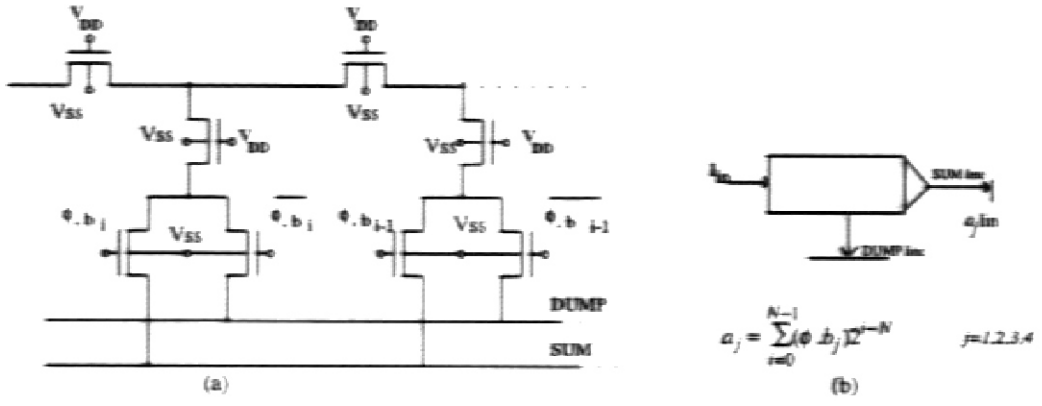
- Track mode : the input current is fed to the cell when switch "s" (ϕ_1) is closed. The current is memorized as a voltage across the holding capacitor. It should be emphasized that linear capacitors are NOT needed to store the data.
- Sampled mode: when switch "s" opens, the voltage is held on the capacitor. This voltage is used to keep the same current through the output transistor M_2 ($(W/L)_{M1} = (W/L)_{M2}$).

In the SI structure shown in Fig. (3.b), all the switches operate at a constant DC voltage, equal to V_b, thus giving rise to a signal independent charge injection.

(III-2) The MOCD as a programmable structure

In the conventional SI technique [7], binary weighted transistors are used as programmable elements. The binary weight technique needs binary weighted current sources [10] to realize a complete programmable element, which means more power consumption with respect to the MOCD structure [1, 2]. In the SI technique, proposed here, the MOCD structure is used as the digitally programmable element. The MOCD, whose scheme is shown in Fig. (4.a), has an input impedance independent of both the digital word and the clock phase, thus providing a constant load impedance to the op amps. The MOCD is switched by "ANDing" the digital word and the switched phase. Without trimming techniques, the MOCD achieves 6-bit resolution, which is sufficient for disk drive circuits [6, 11].

Generally, the output circulating switches (Fig. 2) are implemented by using a rotating switch matrix as in [4]. In this work, the FIR coefficients are controlled by MOCD structures and the rotating switch is simulated by rotating the digital word (b_i, i=0,1,2,...5) of the MOCD. The FIR filter coefficients are circulated through the MOCDs as shown in Table 1. This multiplexing process is achieved via a digital time-multiplexed circuit such as the one shown in Fig. (5.a).



$$a_j = \sum_{i=0}^{N-1} (\phi \cdot b_j) 2^{i-N} \qquad j=1,2,3,4$$

Fig. 4- The MOCD scheme and its symbol.

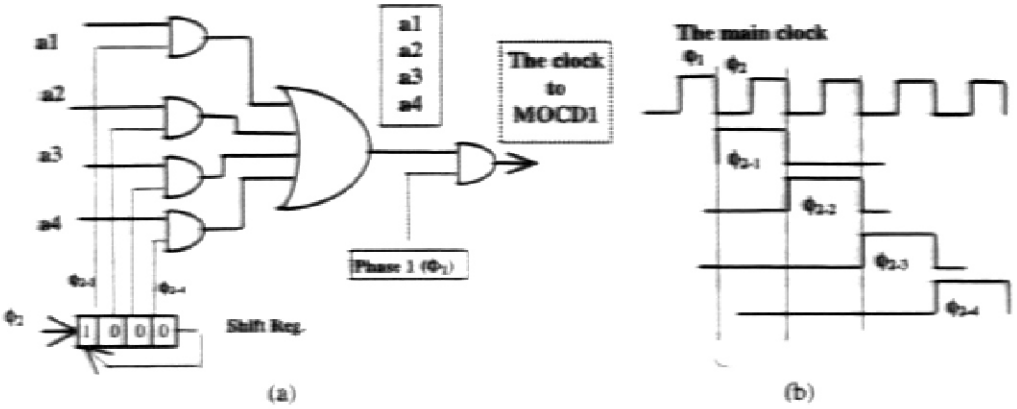


Fig. 5- The time multiplexing digital circuit and the timing diagram.

(III-3) The complete FIR architecture

Each of the S/H circuits and the MOCD programmable structure are used for the complete SI implementation of a 4-tap circular FIR filter, as shown in Fig. 6. The input circulating switch "S1" is realized by using transistor M_2 for each delay cell. In the sample mode of each cell, both "S1" and "S2" of the corresponding cell must be closed together (Φ_{2-1} for the first delay cell, for example). After this time slot, "S2" has to be opened for the hold mode of the sample/hold circuit and "S1" must be opened to avoid the outputs of the cells in the hold mode to be fed to the sampled cell. The control pulses for the input circulating switches "S1" and "S2" of each tap are generated by a shift register circuit, as shown in Fig. (5.a). The clock diagram is shown in Fig. (5.b).

In Fig. 6, the input switch is a large MOS transistor (M_2). Thus, a significant amount of charge can be transferred to the holding capacitor due to both the channel charge and the capacitive coupling between gate and source. Figure (7.a) shows details about the switching methodology of the FIR filter structure shown in Fig. 6 at different clock cycles. Generally, the injected charge due to the switch "S2" is minimized by using a transmission gate structure or dummy transistor technique. Here, we propose a new clock scheme to limit the injected charge into the holding capacitor due to the large transistor M_2. The new scheme is shown in Fig. (7.b). In this clock diagram, switch "S2" in Fig. (7.a) has to open before M_2 turns off to avoid the charge injected by M_2 to be stored into the holding capacitor.

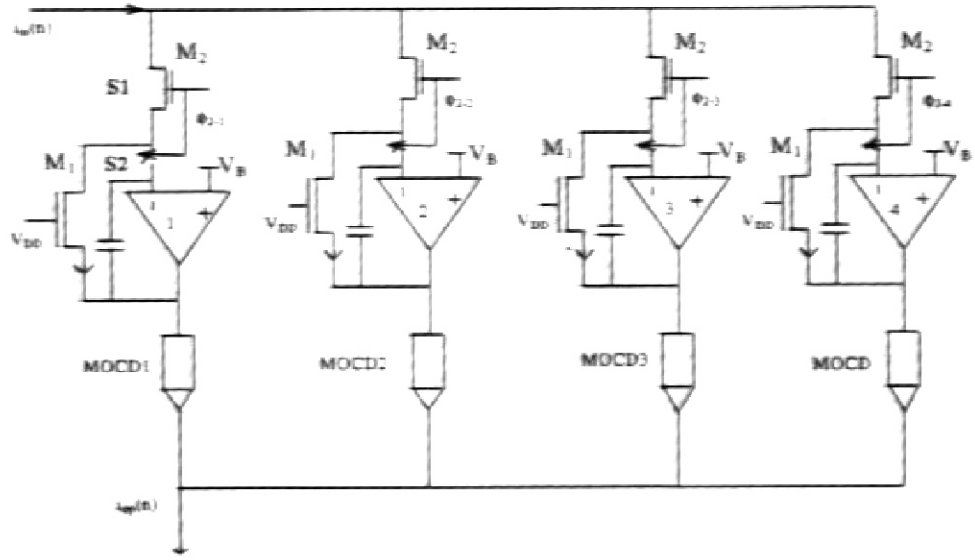
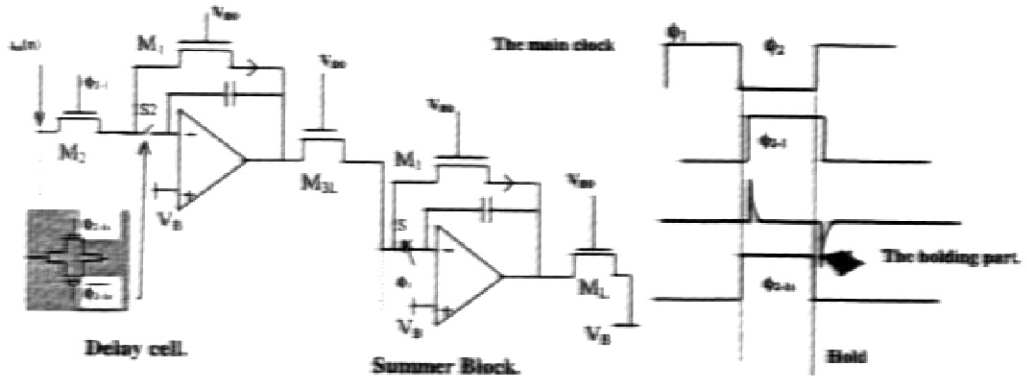


Fig. 6- The SI 4-tap FIR realization in circulating form.

To validate our analysis, the circuit shown in Fig. (7.a) has been simulated with SMASH [12] for a 10μA input current and using switches whose aspect ratio are 2μm/0.8μm and 4μm/0.8μm for the n-channel and p-channel transistors, respectively. The ACM model has been used for the transistors. M_2, M_1, M_L and M_{3L} have aspect ratios equal to 6μm/5μm. A 0.5 pF holding capacitor has been used. The two-stage CMOS op amp has been designed using the methodology described in [13].



(a) The Basic cell. *(b) Proposed clock scheme.*

Fig.7- The basic cell construction of the circulating FIR and its clock scheme.

The bias voltage (V_B) has been generated using the voltage divider scheme proposed in [1]. Transistor M_{3L} (Fig. (7.a)) is equivalent to an MOCD in Fig. 6. The simulation results with and without clock shifting are shown in Fig. 8. The delay time is around 0.4n sec, corresponding to the delay of two cascaded CMOS inverters. In Fig. 8, the DC offset current in the output current $I_D(M_L)$ is due to the charge injected into the holding capacitor. This problem is attenuated by using the clock scheme in Fig. (7.b). The corresponding simulated result is shown in Fig. 8, ($I_D(M_L)$ SHIFT). Finally, the overall switched current FIR filter shown in Fig. 6 has been simulated. The output current measured at the 4th tap is shown in Fig. 9. The delay time is around 200n sec.

IV- *Conclusion*

A programmable switched current CMOS FIR filter has been proposed using the circulating tap technique. The problem of low voltage switches has been overcome by using the SI technique described in [1, 8]. Thus the FIR filter structure is suitable for low voltage disk drive application. The FIR filter structure saves 50% of the total power consumption and active area with respect to traditional FIR realizations in SI technique. A 4-tap FIR filter has been realized and simulated. The total power dissipation is 48mW from a 3V power supply.

ACKNOWLEDGMENTS

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Table 1- The sequence of 4- tap FIR coefficients in the MOCDs at different clock cycles.

Clock cycles	Clock phase	MOCD1	MOCD 2	MOCD3	MOCD4	H(z)
1	ϕ_{2-1}	*a1*	*****	*****	***	a_1Z^{-1}
2	ϕ_{2-2}	a2	*a1*	*****	***	$a_1Z^{-1}+a_2Z^{-2}$
3	ϕ_{2-3}	a3	a2	*a1*	***	$a_1Z^{-1}+a_2Z^{-2}+a_3Z^{-3}$
4	ϕ_{2-4}	a4	a3	a2	a1	$a_1Z^{-1}+a_2Z^{-2}+a_3Z^{-3}+a_4Z^{-4}$
5	ϕ_{2-1}	a1	a4	a3	a2	$a_1Z^{-1}+a_2Z^{-2}+a_3Z^{-3}+a_4Z^{-4}$
6	ϕ_{2-2}	a2	a1	a4	a3	$a_1Z^{-1}+a_2Z^{-2}+a_3Z^{-3}+a_4Z^{-4}$
7	ϕ_{2-3}	a3	a2	a1	a4	$a_1Z^{-1}+a_2Z^{-2}+a_3Z^{-3}+a_4Z^{-4}$

V - *References*

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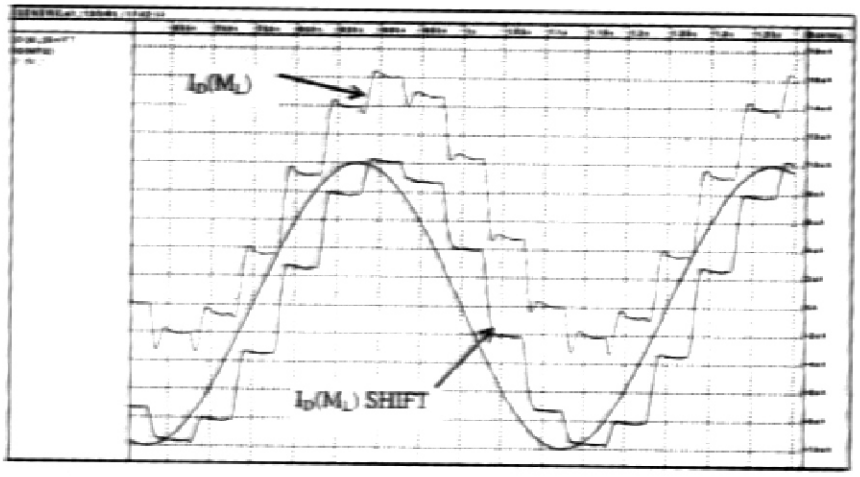

Fig. 8- Simulation results for the circuit of Fig. (7.a).

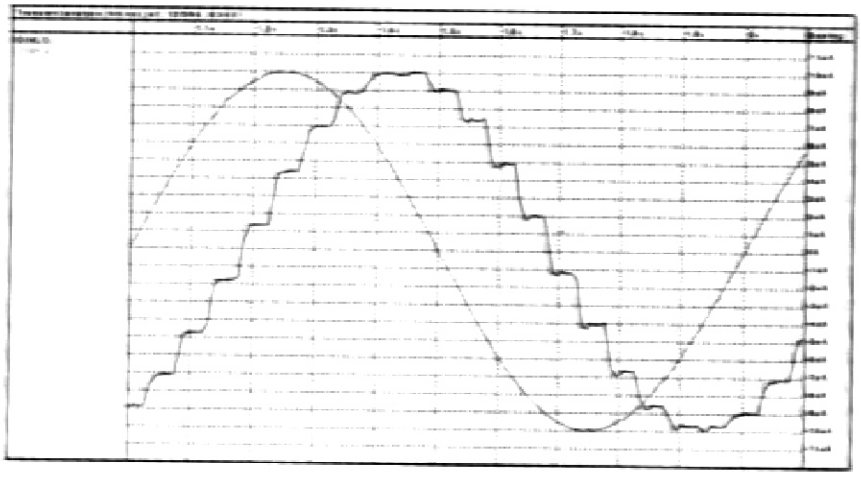

Fig. 9- Input and output current measured at the 4th tap .