A Fully Balanced Switched-Current Sample-Hold Amplifier for Low-Voltage Applications

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ABSTRACT

In this paper, we propose a CMOS fully balanced switched-current (SI) sample-hold amplifier for 20 MHz sampling rate applications. The proposed circuit is based on the switched-current technique described in [1,2], which is appropriate for low voltage operation. The programmability of the sample-hold circuit is achieved via the MOSFET Only Current Division (MOCD) technique [3]. We present a new method for sign bit realization using the two output currents of the MOCD. The programmable S/H circuit is designed to be fabricated in 0.8μm CMOS technology from AMS.

1. Introduction

The switched-current (SI) technique has been considered as a practical way for the implementation of analog sampled data system in digital CMOS technology [4]. Unfortunately, the conventional SI technique presents the same limitation of SC circuits with respect to the conduction gap of the switches when operated at low supply voltages [5]. To overcome the conduction gap of the switches, the SI technique proposed in [1] has been developed. In this SI circuit strategy, the constant voltage switching of the sample-hold is well suited to low voltage applications, since it avoids the conduction gap of the switches as well as the signal dependent charge injection. Based on this method, a fully balanced SI sample-hold is proposed in this work.

Fully Balanced Circuit Architectures (FBCAs) are widely used in analog-signal-processing applications, because an FBCA ensures high power supply rejection, improves linearity and increases the dynamic range. Also, in sampled data circuit (switched capacitor or switched-current) FBCA reduce the effects clock feedthrough and charge injection. The proposed S/H has an FBCA to achieve high accuracy in low voltage application. The proposed S/H is described in section 2. The binary weight controlled MOCD is illustrated in section 3. Section 4 includes a simulation result of the proposed S/H circuit.

2. Fully Balanced SI Sample-Hold Circuit

The general block diagram of a sampled current-mode signal processing is depicted in Fig. 1. The input and output blocks are interfaces between the core section (current-mode) and the surrounding voltage-mode circuits. Moreover, the single to balanced and balanced to single ended sections are necessary to interface a balanced circuit to a single ended one.

Fig. 1. General block of current-mode processing.

A fully balanced switched-current block is designed using the same thoughtway of methodology as in [1,2]. The proposed fully balanced (FB) sample-hold is shown in Fig. 2. In this circuit, the currents (I and -I) are processed in two steps:

- Track mode : the input currents are fed to the cell when both switches are closed. The currents are memorized as voltages across the holding capacitors. It should be emphasized that linear capacitors are not needed to store the data.
- Hold mode: when the switches open, the voltages are held on the capacitors. These voltages cause the output currents to be equal and opposite to the input currents as long as M_1 and M_2 have the same aspect ratios.

In the SI structure shown in Fig. 2, all the switches operate at a constant DC voltage, equal to V_{CM}, thus causing both the charge injection and switch opening time [6] to be signal independent. The "conduction gap", a key limitation of the switches in conventional SI and SC techniques at low voltage supply is avoided with the technique shown in Fig.2. The switches work at a constant DC level out of this gap. In this technique, CMOS switch becomes pointless. In our design NMOS

switches have been used due to their higher conductance compared with the PMOS switches. Our proposed circuit, avoids the switch gap by adjusting V_{CM} using the bias circuit shown in [1,2].

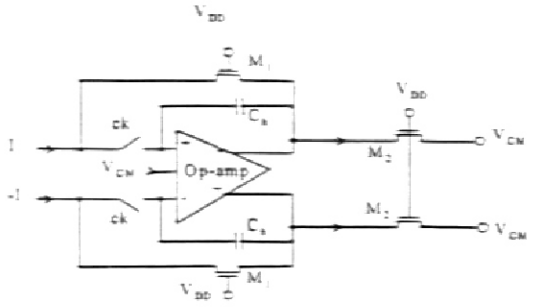

Fig. 2. Proposed switched-current fully balanced sample-hold circuit.

The fully balanced (FB) differential op-amp to be used in the S/H circuit, has been designed according to the methodology in [7]. The FB op-amp schematic is in appendix A. The proposed S/H has been designed for 20MHz sampling rate and using the MOST parameters of the 0.8μm CMOS technology from AMS.

3. MOCD Circuit Architecture and Sign Bit Realization

(3.a) The MOCD schematic

The MOCD ladder circuit is based on the current division technique reported in [3].The schematic of the MOCD together with its symbol are shown in Fig. 3. The output currents at the SUM and DUMP lines are digitally controlled fractions of the input current. This fraction is related to the digital control word as

$$a = \sum_{i=0}^{N-1} b_i 2^{(i-N)} \qquad (1)$$

where N is the number of the MOCD's bits.

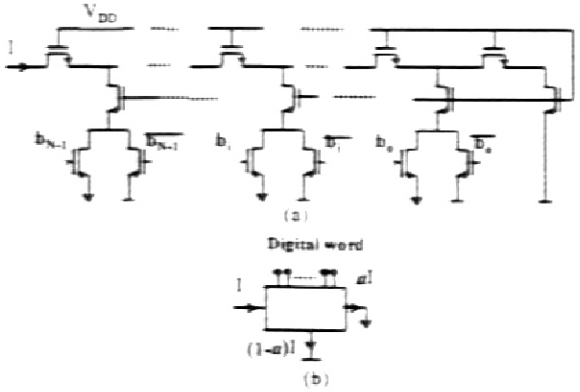

Fig. 3. The MOCD circuit scheme and its symbol.

(3.b) The negative coefficient Implementation.

Programmable (sign and value) taps are necessary for fully programmable filters. The MOCD attenuation factor is changed by using the digital word, Eqn. 1. The sign bit (negative coefficient) control can be achieved by adding an extra transistor with the first section of the MOCD (extra input transistor) as in [8]. The method described in [8] to invert the output currents of the MOCD's is relatively slow due to the need to invert the current of the MOCD's, thus requiring the internal nodes of the MOCD's to be charged to a new set of voltages.

Here, we propose a new method for the sign bit realization. This method is suitable for a fully balanced circuit. It uses the two output currents of the MOCD by adding the SUM current of one MOCD to the DUMP current of the other one, as shown in Fig. 4.a. The positive output current I_{o+} is

$$I_{o+} = (2a-1)I = \beta I \qquad (2)$$

The MOCD fraction factor (a) changes from zero to one when the digital word (<bi>) is changed from 00 to FF (8 bit's MOCD). The variation of the coefficient β against the control digital word is illustrated in Fig. 4.b. This method avoids the need to invert the current of the MOCD's, thus keeping the node voltages of the MOCD's at fixed values. Therefore, the approach proposed here to realize the sign bit is much faster than the one in [8].

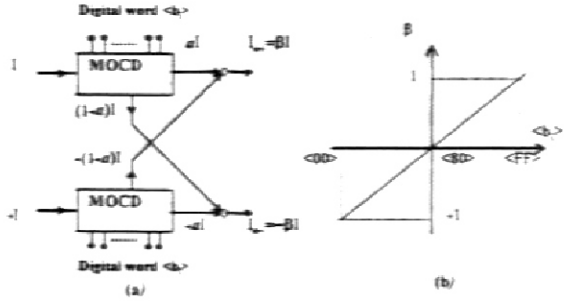

Fig. 4. Proposed method for sign bit realization.

4. The Sample-Hold Simulation

Using the circuits in sections 2 and 3, the fully programmable balanced SI sample-hold circuit has been implemented. 8-bit MOCD's have been used. The complete circuit has been simulated with 3μm/0.8μm NMOS switches, the aspect ratios of M_1 and M_2 equal to 6μm/5μm (6μm/2.5μm MOCD unite transistor) and 0.5pF holding capacitors. The strategy of sign bit realization has been tested as shown in Fig. 5. The top figure of Fig.5 exhibits the most significant bit (sign-bit) variation while the other bits are 1000000 (<40>). Thus, the MOCD fraction factor was ±0.5 as shown from the two bottom curves.

5. Conclusions

A fully programmable balanced SI sample-hold amplifier has been proposed and designed. The proposed S/H circuit achieves high accuracy due to the reduction of the effects of charge injection. The programmability of the S/H is implemented using the MOSFET current divider technique. The new method for sign-bit realization has been analyzed and tested. The S/H occupies 0.8mm^2 silicon area and dissipates 6mW from a 3V supply. The S/H amplifiers proposed here can be used to implement programmable switched-current IIR and FIR filters at low-voltage power supply.

References

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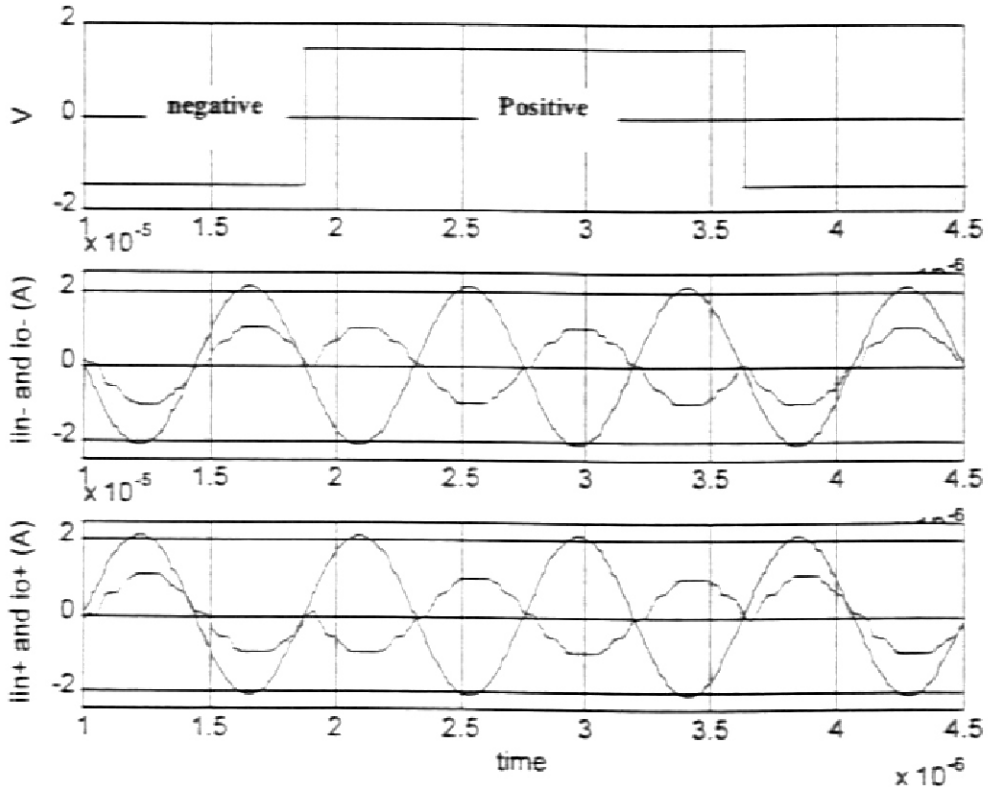

Fig. 5. The time response of the programmable SI S/H circuit.

Appendix A

The complete fully balanced op-amp schematic used in this work is depicted in Fig. A-1.(a). Because the signals are no longer referred to ground, as in single-ended circuit, the operating point of the amplifier cannot be stabilized. A Common Mode Feedback Loop (CMFB) block has to be added to overcome this problem. In our design, a MOSFET network M_{5c} and M_{6c}, instead of a resistive network, is employed to "sense " the common mode voltage. The network composed of M_{5c} and M_{6c} is identical to the network employed to generate the common mode voltage as shown in Fig. A-1(b). The op-amp design methodology in [7] has been used to define transistor geometry. The design method results are shown in table A-1.

Table A-1. (L=2μm).

Op-amp parameter	
C_L (pF)	2
I_B (μA)	120
I_{total}(mA)	2.0
$W_{1,2,1c,2c}$ (μm)	150
$W_{3,4}$(μm)	30
W_8 (μm)	30
$W_{7,7c}$(μm)	30
$W_{3c,4c}$ (μm)	30
$W_{5,9}$ (μm)	200
$W_{6,10}$ (μm)	400
$W_{5c,\ 6c}$ (μm)/L(μm)	5/5
A_o (dB)	62
GB (M Hz)	99
Phase margin	54°
C_c	0.5pF

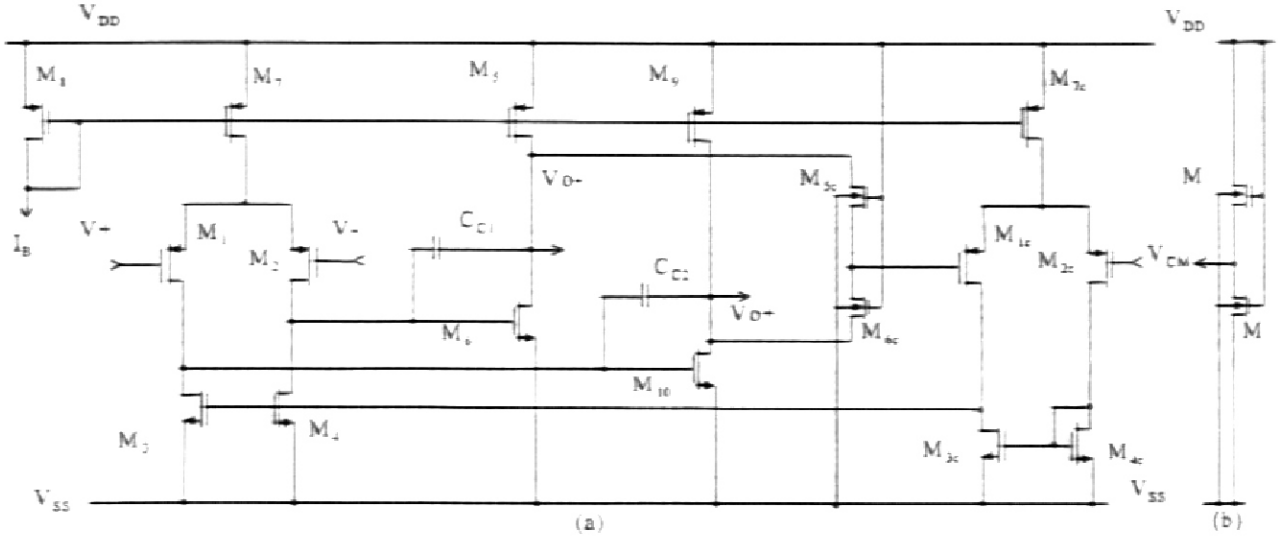

Fig. A-1. Fully balanced differential op-amp schematic and V_{CM} generated circuit.