AN MOS TRANSISTOR MODEL FOR ANALOG CIRCUIT DESIGN

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Abstract

This paper presents a physically based model for the MOS transistor suitable for analysis and design of analog integrated circuits. Static and dynamic characteristics of the MOSFET are accurately described by single-piece functions of two saturation currents in all regions of operation. Simple expressions for the transconductance-to-current ratio, the drain-to-source saturation voltage and the cutoff frequency in terms of the inversion level are given.

1. Introduction

MOSFET models for analog IC design should consist of simple, continuous and accurate single-piece expressions, valid in the whole inversion regime of operation [1]. These models should verify fundamental properties, such as charge conservation [2] and the MOSFET source-to-drain intrinsic symmetry [3]. Moreover, they have to be technology independent and correctly represent not only the strong and inversion regions but also the moderate inversion region, where the MOSFET often operates [4]. Ideally, only a few parameters should be required to describe the model and a simple and consistent characterization procedure should be devised. Finally, analog IC designers need simple expressions to compute transistor dimensions for any current level.

In this work the model of [5], which satisfies all the above mentioned requirements, is entirely rewritten in terms of two components of the transistor current, one associated with the source and the other with the drain. In this reformulation, all the static and dynamic characteristics are expressed as functions of these two components of the drain current. Therefore, hand calculations for circuit design can be substantially simplified.

Our model uses the same basic physical variables as the EKV model [3], but avoids the use of non-physical interpolating curves to bridge the gap between weak and strong inversion. As a consequence, our model allows the calculation of the non-reciprocal capacitances and is charge-conserving.

The model presented here does not include short-channel effects or the dependence of the mobility on the transversal field. The inclusion of such effects leads to complicated expressions that are not suitable for discussion in this paper. A computer-implemented version of our MOSFET model that includes short-channel and field-dependent mobility already exists and can be found elsewhere [9].

The basic principles used to derive our MOSFET model are presented in [5, 13]. The expression for the drain current, based on the model of [5], is presented in order to emphasize its decomposition into two components. The remaining expressions of the MOSFET static and dynamic characteristics in terms of the two components of the drain current are also given. Simulated and measured characteristics are compared. The expressions presented here are a powerful tool for designing analog circuits where the MOSFETs can operate under any inversion level.

2. Fundamentals

The MOSFET model hereinafter is strongly based on two physical features of the MOSFET structure: the charge-sheet model [2, 10] and the incrementally linear relationship between the inversion charge density and the surface potential [5, 6]. Combined, these two approximations allow deriving a MOSFET model entirely formulated in terms of two components of the drain current [3, 11].

Two basic parameters of our model are n, the slope factor:

$$n = 1 + \frac{\gamma}{2\sqrt{\phi_0 + V_P}} \qquad (1.a)$$

where γ is the body effect factor, ϕ_0 is a potential whose value is a few ϕ_t (thermal voltage) above twice the Fermi potential for holes [3] and V_P, the "pinch-off" voltage [3, 5], given by:

$$V_P = \left[\sqrt{V_G - V_{T0} + \left(\sqrt{\phi_0} + \gamma/2\right)^2} - \gamma/2\right]^2 - \phi_0 \cong \frac{V_G - V_{T0}}{n} \qquad (1.b)$$

In (1.b) V_{T0} is the threshold voltage in equilibrium, corresponding to the value of V_G for which V_P is equal to zero. In our model, all voltages are referred to the local substrate, as in [3].

The drain current in a long-channel transistor is given [3,11,12] by:

$$I_D = I_F - I_R \tag{2.a}$$

$$I_{F(R)} = I(V_G, V_{S(D)}) = \mu n C'_{ox} \frac{W}{L} \frac{\phi_t^2}{2} \left[\left(\frac{Q'_{IS(D)}}{nC'_{ox}\phi_t} \right)^2 - \frac{2Q'_{IS(D)}}{nC'_{ox}\phi_t} \right] \tag{2.b}$$

where $I_{F(R)}$ is the forward (reverse) saturation current and $Q'_{IS(D)}$ is the inversion charge density evaluated at the source (drain) end. Therefore, the forward (reverse) saturation component of the current is associated with the source (drain) inversion charge density by a one-to-one relationship. In (2.b), μ is the carrier mobility, W is the channel width, L is the channel length and C'_{ox} is the gate oxide capacitance per unit area..

Equations (2) emphasize the source-drain symmetry of the MOSFET. In order to exploit the intrinsic symmetry of the device, voltages are referred to the substrate [3] (Fig.1). Let us now explain how to determine the forward and reverse components of the drain current from the transistor output characteristic, as the one shown in Fig.1 for a long-channel MOSFET. Note that there is a region, usually called saturation region, where the drain current is almost independent of V_D. This means that in this region $I(V_G, V_D) \ll I(V_G, V_S)$. Therefore, $I(V_G, V_S)$ can be interpreted as the drain current in forward saturation. Similarly, in reverse saturation, I_D is independent of the source voltage. Since the long-channel MOSFET is a symmetric device, the knowledge of the saturation current $I(V_G, V_S)$ for any V_G, V_S allows computing the drain current for any combination of source, drain and gate voltages.

3.Model Formulation

In this Section we show how to derive continuous, single-piece expressions for the large and small signal characteristics of the MOSFET in terms of the forward and reverse saturation currents. These expressions are very accurate in weak, moderate and strong inversion.

A. Current Normalization

Expression (2.b) can be rewritten in the form:

$$-\frac{Q'_{IS(D)}}{nC'_{ox}\phi_t} = \sqrt{1 + i_{f(r)}} - 1 \tag{3.a}$$

where

$$i_{f(r)} = \frac{I_{F(R)}}{I_S} = \frac{I(V_G, V_{S(D)})}{I_S} \tag{3.b}$$

is the forward (reverse) normalized current [3] and

$$I_S = \mu n C'_{ox} \frac{\phi_t^2}{2} \frac{W}{L} \tag{3.c}$$

is the normalization current, which is four times smaller than the homonym presented in [3]. The factor $\mu n C'_{ox} \phi_t^2/2$, which is herein denominated the sheet normalization current I_S, is a technological parameter slightly dependent on V_G, through μ and n.

In [3] the forward normalized current i_f is also properly referred to as the inversion coefficient since it indicates the inversion level of the device, which depends on both the gate and source voltages. As a rule of thumb, values of i_f greater than 100 characterize strong inversion. The transistor operates in weak inversion up to $i_f = 1$. Intermediate values of i_f, from 1 to 100, indicate moderate inversion.

The source (drain) transconductance, defined as the derivative of the drain current with respect to the source (drain) voltage, can be obtained either by differentiating (2):

$$g_{ms(d)} = -(+)\frac{\partial I_D}{\partial V_{S(D)}} = -\mu \frac{W}{L} \phi_t \frac{\partial Q'_{IS(D)}}{\partial V_{S(D)}} \left(\frac{Q'_{IS(D)}}{nC'_{ox}\phi_t} - 1 \right) \tag{4.a}$$

or from the general expression [3, 5]:

$$g_{ms(d)} = -\mu \frac{W}{L} Q'_{IS(D)} \tag{4.b}$$

The combination of (3.a), (4.a) and (4.b) allows one to express the derivative of the source (drain) inversion charge density with respect to the source (drain) voltage as a function of the forward (reverse) normalized current:

$$\frac{\partial Q'_{IS(D)}}{\partial V_{S(D)}} = nC'_{ox} \frac{\sqrt{1 + i_{f(r)}} - 1}{\sqrt{1 + i_{f(r)}}} \tag{4.c}$$

In the model of [5] all the static (drain current and total charges) and dynamic (three transconductances and nine independent (trans)capacitances) characteristics of the long-channel MOS transistor are expressed as functions of the source and drain inversion charge densities and their derivatives with respect to the source and drain voltages. Expressions (3.a) and (4.c) allow rewriting the charge model of [5] in terms of the normalized saturation currents i_f and i_r, as shown in Table I.

Table I synthesizes the overall behavior of a large and long-channel device from weak to strong inversion. It is remarkable that only three parameters (I_S, C_{ox} and n) are enough to characterize the small-signal parameters of the MOSFET. Short and narrow channel effects can be modeled as in [3]. The current-based expressions in Table I are useful for analysis and design of current-biased circuits, as is the case of almost all the analog circuits.

B. Current-to-Transconductance Ratio

An important design parameter required in analog circuits is the current-to-transconductance ratio [4]. In the following we will demonstrate that this design parameter can be expressed in terms of a normalized saturation current.

The substitution of (3.a) into (4.b) allows one to derive the equation for the source (drain) transconductance in Table I. Therefore, the ratio of the drain current in forward (reverse) saturation to the source(drain)-transconductance is given by

$$\frac{I_{F(R)}}{\phi_t \cdot g_{ms(d)}} = \frac{\sqrt{1 + i_{f(r)}} + 1}{2} \tag{5}$$

Expression (5) is independent of gate voltage, transistor dimensions, technology and temperature. Therefore, (5) is a universal expression for MOS transistors as well as the transconductance-to-current ratio is for bipolar transistors. Expression (5) is a very powerful tool for circuit design since it allows designers to compute the available transconductance-to-current ratio in terms of the inversion level i_f. Moreover, (5) provides a straightforward procedure for extracting the value of the normalization current, as shown in [11, 12].

The universality of the law in (5) is confirmed in Fig. 2 where measured and simulated current-to-transconductance ratios are plotted for different gate voltages, technologies and channel lengths. The accuracy of (5) is excellent for any of these cases.

C. Output Characteristics

Since the source (drain) transconductance $g_{ms(d)}$ is the derivative of $-(+)I_{F(R)}$ with respect to $V_{S(D)}$, the relationship between source (drain) voltage and forward (reverse) normalized current (last expression in Table I) is determined by integrating (5). In the last expression of Table I, $V_{S(D)} = V_P$ implies that $i_{f(r)} = i_P$; thus, the assigned value of parameter i_P defines V_P and should be chosen in the transition from weak to strong inversion. In this work we have adopted $i_P = 3$, which corresponds to the condition $Q'_{IS(D)} = -nC'_{ox}\phi_t$ at $V_{S(D)} = V_P$ [11, 12].

Fig. 3 shows the measured and simulated "common-gate" characteristics for a saturated ($V_D = V_G$) NMOS transistor of a 0.75 μm technology (oxide thickness of 280 Å) with L = W = 25 μm. The simulated curves have been determined from the first and last expressions in Table I (assuming that, in saturation, i_r is equal to zero) and the definitions of i_f and I_S in (3.b-c). An excellent matching between the experimental results and the proposed model is observed in all regions of operation.

The MOSFET output characteristics described by the universal relationship:

$$\frac{V_{DS}}{\phi_t} = \sqrt{1+i_f} - \sqrt{1+i_r} + \ln\left(\frac{\sqrt{1+i_f}-1}{\sqrt{1+i_r}-1}\right) \qquad (6)$$

are readily derived from the last expression in Table I. Expression (6) demonstrates that the normalized output characteristics of a long-channel MOSFET are independent of technology and transistor dimensions, corroborating again the universality and consistency of our model. In Fig.4 we compare the measured output characteristics, for several gate voltages, and the ones simulated by (6).

The theoretical drain-to-source saturation voltage, V_{DSSAT}, is defined here as the value of V_{DS} for which the ratio $Q'_{ID}/Q'_{IS} = \varepsilon$, where ε is an arbitrary number much smaller than one. Therefore, from (3.a) and (6),

$$V_{DSSAT} = \phi_t\left[\ln\left(\frac{1}{\varepsilon}\right) + \sqrt{1+i_f} - 1\right] \qquad (7)$$

The definition in (8) is extremely useful for circuit design since it gives the boundary between the triode and saturation regions in terms of the inversion level. Note that in weak inversion V_{DSSAT} is independent of the inversion level while in strong inversion V_{DSSAT} is proportional to the square root of the inversion level. The saturation voltage is around 120 mV (ε=0.01) in weak inversion [8] and around 350 mV if i_f=100. Our definition of saturation is arbitrary but provides designers with a very good first order approximation to the minimum V_{DS} required to keep the MOSFET in the "constant current region".

D. Small Signal Parameters

Table I shows the expressions for the source (g_{ms}), drain (g_{md}) and gate (g_{mg}) transconductances, defined in [3, 5] as the partial derivatives of $I_D(V_S, V_D, V_G)$ with respect to the source, drain and gate voltages, respectively. Fig.5 compares the measured and simulated values of the gate transconductance, for the same device of Fig. 3, thus demonstrating the satisfactory precision of the proposed model.

The expressions for the ten intrinsic (trans)capacitances listed on Table I are obtained from the differentiation of the inversion (Q_I), depletion (Q_B), source (Q_S) and drain (Q_D) total charges with respect to the terminal voltages. One should recall that only nine of the sixteen possible (trans)capacitances are independent [2]. In Fig.6 we compare some of the intrinsic transcapacitances calculated from the expressions presented in Table I and from the charge-sheet ϕ_S-formulated model of [7], which is already known to fit experiments very well.

It can be noticed that all the small-signal parameters in Table I approximate to their well-known asymptotic values in weak and strong inversion [3]. For instance, deep in weak inversion, that is, for $i_f \ll 1$, $\sqrt{1+i_f}$ can be approximated by $1+i_f/2$. Therefore, g_{ms} (Table I) tends to its expected value, I_F/ϕ_t. On the other hand, in very strong inversion, g_{ms} is proportional to $\sqrt{I_F}$ since i_f is much greater than one.

The small-signal parameters in Table I describe the MOSFET behavior in quasi-static operation, being suitable for low and medium frequency analysis. The frequency limits of validity for this quasi-static approach are discussed in [11, 12], where a nonquasi-static model of the MOSFET is presented.

4. Transistor cutoff frequency

Analog circuit designers need to determine bias current and transistor dimensions in order to satisfy design specifications such as gain and cutoff frequency.

Even though it is possible to choose the inversion level, the designer should be aware of the frequency capability of the transistor, which is most often specified in practice by the intrinsic cutoff frequency f_T. The intrinsic cutoff frequency of an MOS transistor is defined as the frequency value for which the short-circuit current gain in the common-source configuration drops to 1 [2]. The intrinsic cutoff frequency of a MOSFET in saturation is [2] given by:

$$f_T = \frac{g_{mg}}{2\pi(C_{gs}+C_{gb})} = \frac{g_{ms}}{2\pi n(C_{gs}+C_{gb})} \qquad (8.a)$$

From the expressions of g_{ms}, C_{gs} and C_{gb} presented in Table I, f_T can be readily written in terms of the inversion coefficient as:

$$f_T = \frac{\mu n \phi_t}{2\pi L^2} \frac{i_f\left(\sqrt{1+i_f}+1\right)}{(n-1)\left(\sqrt{1+i_f}+1\right)^2 + \frac{2}{3}\left(i_f+\sqrt{1+i_f}-1\right)} \qquad (8.b)$$

The first term in the right-hand side of (8.b) shows the dependence of f_T on the channel length and on the slope factor and mobility, both slightly dependent on technology and on gate voltage. The second term represents the dependence of the cutoff frequency on the inversion level. Usually, due to the lack of adequate models, designers employ transistors whose f_T is much higher than that required for a specific application, thus leading to an unnecessary increase in power consumption.

Assuming the slope factor n in the denominator of (8.b) to be equal to 4/3, a typical value, f_T can be roughly approximated to:

$$f_T \equiv \frac{\mu \phi_t}{2\pi L^2} 2\left(\sqrt{1+i_f}-1\right) \qquad (8.c)$$

for any inversion level.

Fig.7 shows the intrinsic cutoff frequency calculated from (8.b), for n = 4/3 and n = 5/3, and from (8.c), for a large range of the inversion coefficient.

5. Conclusions

An accurate MOSFET model valid in weak, moderate and strong inversion has been presented. All the device characteristics are expressed as single-piece functions of the saturation components of the drain current. A physics-based law for the current-to-transconductance ratio in the MOSFET has been derived and experimentally verified. The model presented here is a powerful tool that can be used for both hand calculations as well as computer-assisted analysis and design of MOSFET integrated circuits.

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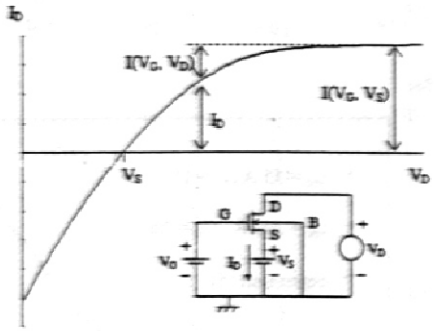

Fig.1. Output characteristic of a long-channel NMOS transistor for constant V_S and V_G. All voltages are referred to the bulk terminal.

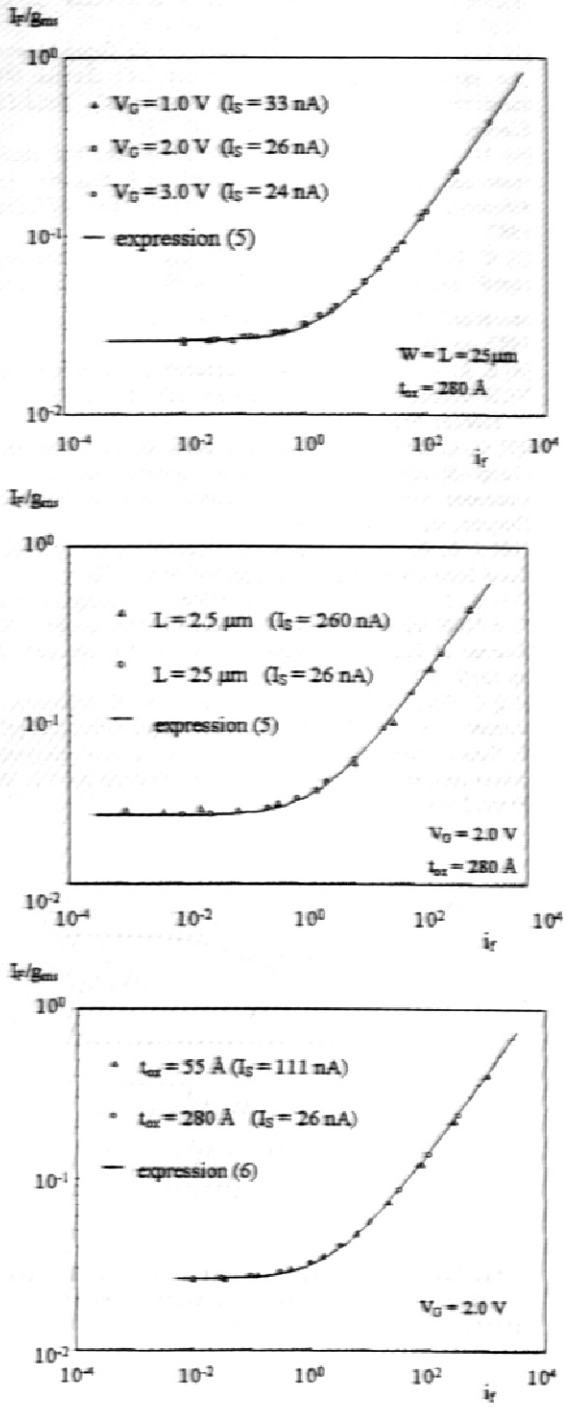

Fig.2. Forward current-to-transconductance ratio (I_F/g_{ms}) vs. inversion coefficient of NMOS transistors: (a) biased at different gate voltages; (b) with different channel lengths; (c) from different technologies.

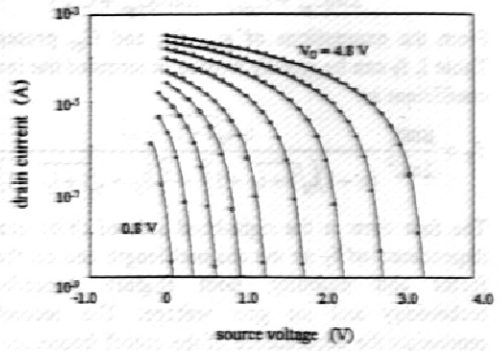

Fig.3. Common-gate characteristics of an NMOS transistor in saturation, with t_{ox} = 280 Å and W = L = 25 μm (V_G = 0.8, 1.2, 1.6, 2.0, 2.4, 3.0, 3.6, 4.2 and 4.8 V): (——) simulated curves calculated from Table I; (o) measured curves.

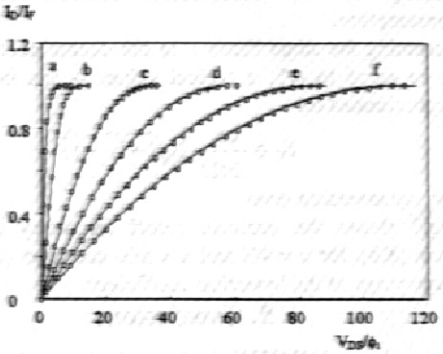

Fig.4. Normalized output characteristics (NMOS transistor, t_{ox} = 280 Å and W = L = 25 μm). $I_F = I_D$ @ $V_D = V_G$ and $V_S = 0$.

O measured data —— calculated from (6)

(a) $i_f = 4.5 \times 10^{-2}$ (V_G = 0.7 V) (b) i_f = 65 (V_G = 1.2 V)
(c) $i_f = 9.5 \times 10^{2}$ (V_G = 2.0 V) (d) $i_f = 3.1 \times 10^{3}$ (V_G = 2.8 V)
(d) $i_f = 6.8 \times 10^{3}$ (V_G = 3.6 V) (f) $i_f = 1.2 \times 10^{4}$ (V_G = 4.4 V)

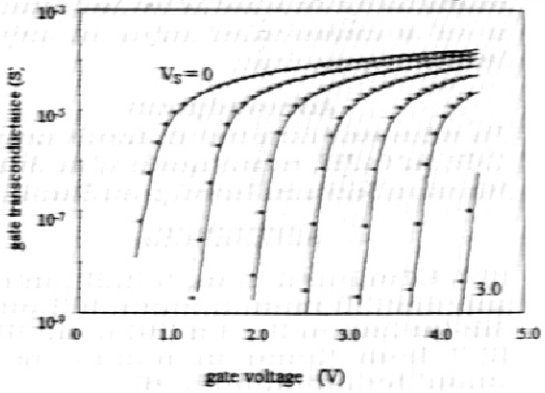

Fig.5. Gate transconductance (V_S = 0, 0.5, 1.0, 1.5, 2.0, 2.5 and 3.0 V) of an NMOS transistor with t_{ox} = 280 Å and W = L = 25 μm: (——) simulated curves calculated from Table I; (o) measured curves.

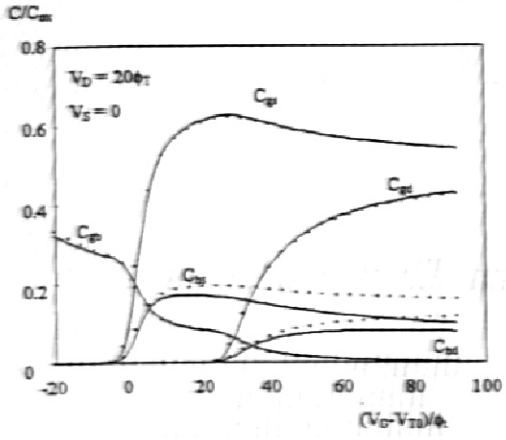

Fig.6. Intrinsic capacitances simulated from: (——) our quasi-static model described in Table I; (o) the ϕ_S-formulated model of [7].(NMOS transistor with t_{ox} = 250 Å, $N_A = 2 \times 10^{22}$ m^{-3} and $V_{T0} = 0.7$ V)

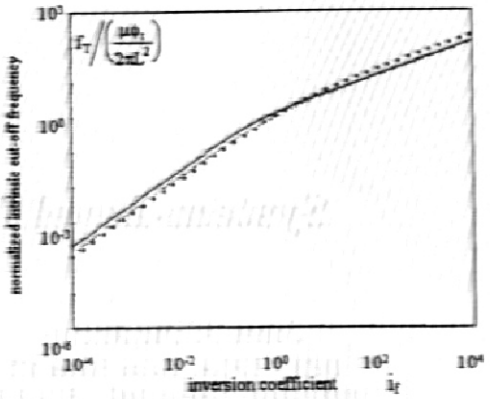

Fig.7. Normalized intrinsic cutoff frequency: (——) eqn.(8.b) with n = 4/3; (----) eqn.(8.b) with n = 5/3; (o) eqn.(8.c).

Table I - Expressions for the MOSFET Static and Dynamic Characteristics

Variable	Expression
I_D	$I_S\,(i_f - i_r)$
Q_I	$-C_{ox} n \phi_t \left[\frac{2}{3} \left(\sqrt{1+i_f} + \sqrt{1+i_r} - \frac{\sqrt{1+i_f}\sqrt{1+i_r}}{\sqrt{1+i_f} + \sqrt{1+i_r}} \right) - 1 \right]$
Q_B	$-\frac{n-1}{n} Q_I - C_{ox} \frac{\gamma^2}{2(n-1)}$
Q_S	$-C_{ox} n \phi_t \left[\frac{2}{15} \left(\frac{3\left(\sqrt{1+i_f}\right)^3 + 6(1+i_f)\sqrt{1+i_r} + 4\sqrt{1+i_f}(1+i_r) + 2\left(\sqrt{1+i_r}\right)^3}{\left(\sqrt{1+i_f} + \sqrt{1+i_r}\right)^2} \right) - \frac{1}{2} \right]$
Q_D	$Q_I - Q_S$
$g_{ms(d)}$	$\frac{2I_S}{\phi_t} \left(\sqrt{1+i_{f(r)}} - 1 \right)$
g_{mg}	$(g_{ms} - g_{md})/n$
$C_{gs(d)}$	$C_{ox} \frac{2}{3} \left(1 - \frac{1}{\sqrt{1+i_{f(r)}}} \right) \left[1 - \frac{1+i_{r(f)}}{\left(\sqrt{1+i_f} + \sqrt{1+i_r}\right)^2} \right]$
$C_{gb} = C_{bg}$	$[(n-1)/n](C_{ox} - C_{gs} - C_{gd})$
$C_{bs(d)}$	$(n-1)C_{gs(d)}$
C_{ss}	$C_{ox} \frac{2}{15} n \left(\sqrt{1+i_f} - 1 \right) \frac{3(1+i_f) + 9\sqrt{1+i_f}\sqrt{1+i_r} + 8(1+i_r)}{\left(\sqrt{1+i_f} + \sqrt{1+i_r}\right)^3}$
C_{sd}	$-C_{ox} \frac{4}{15} n \left(\sqrt{1+i_r} - 1 \right) \frac{2 + i_f + 3\sqrt{1+i_f}\sqrt{1+i_r} + i_r}{\left(\sqrt{1+i_f} + \sqrt{1+i_r}\right)^3}$
C_{sg}	$(C_{ss} - C_{sd})/n$
C_{sb}	$(n-1)C_{sg}$
$V_P - V_{S(D)}$	$\phi_t \left[\sqrt{1+i_{f(r)}} - \sqrt{1+i_P} + \ln \left(\frac{\sqrt{1+i_{f(r)}} - 1}{\sqrt{1+i_P} - 1} \right) \right]$

$C_{ox} = C'_{ox} WL$; $i_P = 3$