# DESIGN TRADEOFFS OF CMOS CURRENT MIRRORS USING ONE-EQUATION FOR ALL-REGION MODEL

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## ABSTRACT

The design of current mirror involves different conflicting design specifications (noise, bandwidth, input and output resistances, power dissipation, accuracy, THD, etc..), while only three design transistor parameters are available (DC current, width, length). In this paper, we address the effect of such parameters on the current mirror performance. For each specification, an expression is derived which is valid for any inversion level based on the one-equation for all-region MOS model [1]. Experimental results from a current mirror fabricated in 0.5μm AMI CMOS process are found in good agreement with the theoretical ones.

## 1. INTRODUCTION

Current mirrors have been taking part in almost all analog integrated circuits. In most cases, the performance of these circuits is limited by the non-idealities of the current mirror. In this paper, the one-equation model derived in [1] for MOS transistor is used to analyze the performance of the simple current mirror shown in Fig. 1, where $A_I$ is the required current gain, W/L and $A_I$W/L are the aspect ratios of the input and output transistors, respectively. The output transistor $M_2$ is assumed to operate in saturation. The model equations for the saturation region are listed below for convenience.

$$V_p = \left[\sqrt{V_G - V_{T0} + (\sqrt{\phi_0} + \gamma/2)^2} - \gamma/2\right]^2 - \phi_0 \cong \frac{V_G - V_{T0}}{n} \quad (1)$$

where:

$$n = 1 + \frac{\gamma}{2\sqrt{\phi_o + V_p}} \qquad \phi_o = 2\phi_F \quad (2)$$

$$I_S = 0.5 n \mu C_{ox} \varphi_t^2 \frac{W}{L} = normalization\ current \quad (3)$$

$$i_f = \frac{I}{I_S} = \frac{I(V_G, V_S)}{I_S} \quad (4)$$

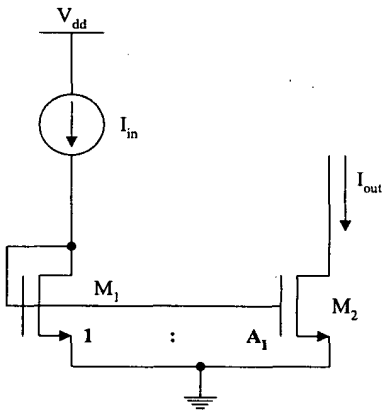


Fig. 1 Simple current mirror

$$\frac{V_p - V_{S(D)}}{\varphi_t} = \sqrt{1 + i_f} - 2 + \ln(\sqrt{1 + i_f} - 1) \quad (5)$$

where:

$V_p$ is the pinch-off voltage [1].

$V_{T0}$ is the threshold voltage in equilibrium.

$\gamma$ is the body effect factor.

$\phi_F$ is the Fermi potential for holes.

$i_f$ is the forward current inversion level.

I is the drain current.

$\mu$ is the low field mobility.

$C_{ox}$ is the gate oxide capacitance/unit area.

$\varphi_t$ is the thermal voltage.

n is the sub-threshold slope factor [1], slightly dependent on $V_G$, greater than one and usually less than two. In this paper, n = 4/3 is used to simplify the analyses.

## 2. ANALYSIS OF THE CURRENT MIRROR

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In each of the following subsections, simulation results using version 3.1 BSIM models will be compared with the theoretical results. Measurement results, from a current mirror fabricated in 0.5μm CMOS process, will also be presented. Unless otherwise stated, all simulations and measurements are done with W = 120μm, L =1.2μm, and $A_I$ = 1. Note that, since $V_{GS1} = V_{GS2}$, M1 and M2 will have the same inversion level ($i_f$).

### 2.1. Output and input resistances

In the saturation region, channel length modulation and drain-induced barrier lowering (DIBL) are the main factors limiting the output resistance of an MOS transistor. To take into account these two effects, the following empirical formula can be used:

$$R_{out} = \frac{LV_A}{A_I I_{S1} i_f^{\alpha}} \tag{6}$$

where $V_A$ is the Early voltage / unit length, $I_{S1}$ is the normalization current of the input transistor, and α is a parameter usually assumed to be equal to one. However, in order to have a better fit of equations (6) with the measurement results, α is chosen slightly smaller than one. (about 0.9 in 0.5μm AMI CMOS technology). Fig. 2 shows the simulated and measured output resistance together with the expected output resistance for α = 1 and α = 0.91. It was found that the maximum deviation error in the expected $R_{out}$ is 18% for α = 0.91 and 50% for α = 1.

The input resistance of the simple current mirror is given by:

$$R_{in} = \frac{\partial V_{in}}{\partial I_{in}} = \frac{\partial V_{GS}}{I_{S1}\partial i_f} = \frac{n\varphi_t}{2I_{S1}}\left(\frac{1}{\sqrt{1+i_f}-1}\right) \tag{7}$$

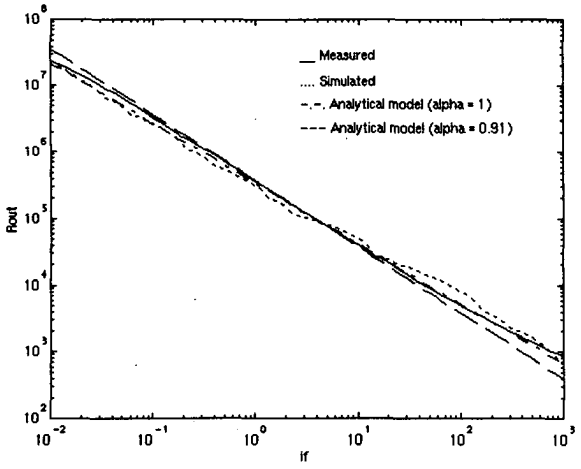


Fig. 2 Output resistance of the current mirror

### 2.2. Current gain errors

Accuracy of the current mirror is mainly limited by three parameters, namely, $V_{T0}$ mismatch, β mismatch, and the finite output resistance of the transistor. The current gain error (CGE) due to $V_{T0}$ mismatch can be derived from (5):

$$CGE|_{V_T} = \frac{\Delta I}{I} = -2\frac{\sqrt{1+i_f}-1}{i_f}\frac{\Delta V_{T0}}{n\varphi_t} = \begin{cases} -\dfrac{\Delta V_{T0}}{n\varphi_t} & i_f >> 1 \\ -\dfrac{2}{\sqrt{i_f}}\dfrac{\Delta V_{T0}}{n\varphi_t} & i_f >> 1 \end{cases} \tag{8}$$

where $\Delta V_{T0} = V_{T2} - V_{T1}$ and $\Delta I = I_2 - I_1$. The above equation shows that the CGE due to $V_{T0}$ mismatch increases when $i_f$ is decreased. However, this error becomes less dependent on $i_f$ in the weak inversion region ($i_f < 1$). Note the equation reduces to the well-known CGE at the weak and strong inversion regions. The CGE is independent of $i_f$ in the weak inversion region because of the exponential IV characteristic. The simulated and theoretical errors of a current mirror in 0.5μm technology are shown in Fig. 3, for $\Delta V_{T0}$= -10mV. Since it is not possible to control the $V_{T0}$ mismatch between the transistors M1 and M2, the mismatch is artificially imposed by offsetting the gate voltage of M2 by 10mV with respect to that of M1. A well-matched current mirror ($\Delta V_{T0}$ < 1mV) is chosen for this measurement to ensure that the total effective mismatch is close to 10mV. The theoretical and simulated CGEs match well in the strong and weak inversion regions. However, the difference reaches its maximum value (about 40%) at $i_f$ = 1. In the same figure, the measured CGE is shown to be well matched with the theoretical curve in the whole inversion regime with maximum error of only 10%. This shows the superior accuracy of the all-region model over BSIM model. The figure also shows that the sensitivity to $V_{T0}$ mismatch increases at weak inversion.

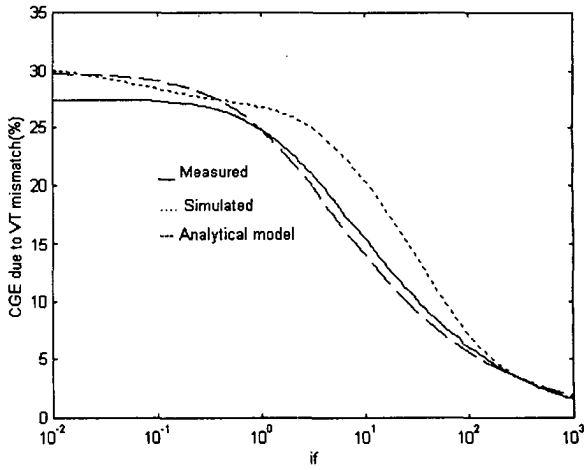


Fig. 3 The CGE due to $V_{T0}$ mismatch

The second factor that determines the accuracy of the current mirror is the mismatch in the transconductance parameter (β). Since the output current of the transistor is linearly proportional to β, then:

$$CGE|_{\beta mismatch} = \frac{\Delta\beta}{\beta} \tag{9}$$

where β is defined as:

$$\beta = \mu C_{ox} \frac{W}{L} \tag{10}$$

Note that, as expected, β mismatch leads to a CGE that is independent of the inversion level ($i_f$).

The third factor that affects the CGE is the output resistance of the transistor. The CGE due to output resistance depends on the load resistance of the current mirror. It's a common practice to evaluate this type of error when the current mirror is loaded with a similar current mirror. In other words, we will calculate the CGE due to output resistance when the load resistance is the same as the input resistance of the current mirror. In this case, the CGE is expressed as:

$$CGE|_{Rout} = -\frac{R_{in2}}{R_{out}} = -\frac{n\varphi_t}{2LV_A}\left(\frac{i_f^{\alpha}}{\sqrt{1+i_f}-1}\right) \tag{11}$$

where $R_{in2}$ is the input resistance of the next stage, which is assumed to be a current mirror with the same aspect ratio as M2 and the same inversion level. This is illustrated in Fig. 4, in which it is shown that the CGE magnitude exhibits a minimum of about 2.5% at $i_f = 0.072$ in the theoretical model, which is close enough to the measured minimum value 2.44% at $i_f = 0.05$. The CGE starts to increase in the moderate and strong inversion regions. Note also that, from (11), the CGE can be reduced by increasing the length of the transistor. Unfortunately, this will reduce the bandwidth and increase the area of the current mirror.

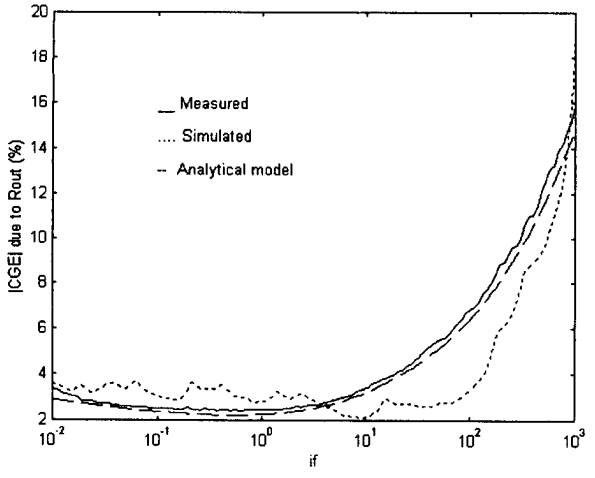


Fig. 4 The CGE due to output resistance

**2.3. Noise**

The input referred thermal noise current can be expressed as:

$$\overline{i_{ni}^2} = \overline{i_{n1}^2} + \frac{1}{A_I^2}\overline{i_{n2}^2} \tag{12}$$

From [2], for an MOS transistor, the input referred noise is given by:

$$\overline{i_n^2} = -4kT\frac{\mu}{L^2}Q_I\Delta f \tag{13}$$

where $Q_I$ is the total inversion layer charge. It can be calculated by integrating the inversion charge density over the transistor area:

$$Q_I = W\int_0^L Q_I'(x)dx \tag{14}$$

From [1]:

$$I_D = \mu W\left(\frac{-Q_I'(x)}{nC_{ox}} + \varphi_t\right)\frac{dQ_I'(x)}{dx} \tag{15}$$

From equations (14) and (15):

$$Q_I = \frac{\mu W}{I_D}\left(\frac{-(Q_{ID}'^{\,3} - Q_{IS}'^{\,3})}{3nC_{ox}} + \varphi_t\frac{Q_{ID}'^{\,2} - Q_{IS}'^{\,2}}{2}\right) \tag{16}$$

where $Q'_{ID}$ and $Q'_{IS}$ are the inversion charge densities at the drain and source, respectively, and can be expressed in terms of the inversion level as follows [1]:

$$Q_{IS(D)}' = -nC_{ox}\varphi_t\left(\sqrt{1+i_{f(r)}}-1\right) \tag{17}$$

Substituting in (16) and noting that the reverse inversion level ($i_r$) is zero for a saturated transistor, then:

$$Q_I = \frac{\mu W\varphi_t(nC_{ox}\varphi_t)^2}{I}\left(\frac{1}{3}(1+i_f)^{\frac{3}{2}} - \frac{1}{2}(1+i_f) + \frac{1}{6}\right) \tag{18}$$

Using (3), (4), (12), (13), and (18), we obtain:

$$\overline{i_{ni}^2} = 16qI_{S1}\left(1+\frac{1}{A_I}\right)\left(\frac{\frac{1}{3}(1+i_f)^{\frac{3}{2}} - \frac{1}{2}(1+i_f) + \frac{1}{6}}{i_f}\right)\Delta f \tag{19}$$

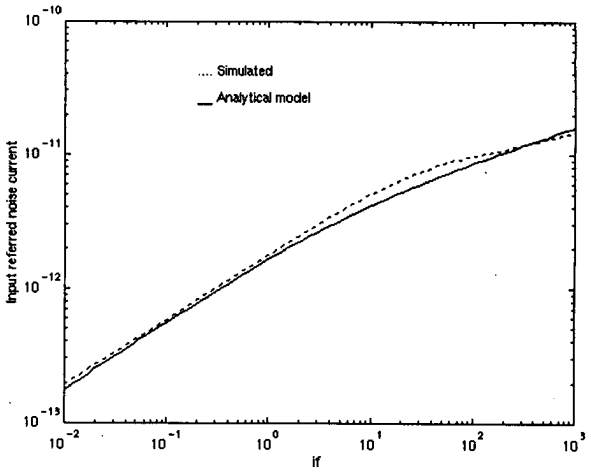


Fig. 5 The input referred noise current

Fig. 5 shows the theoretical and simulated input referred noise current densities in $A/\sqrt{Hz}$ for unity current gain. The two curves are fairly close to each other in the weak and strong inversion regions. In moderate inversion, the simulated curve deviates from the theoretical equation (19). The deviation error is less than 20%, which may be acceptable for noise calculations.

### 2.4. The bandwidth

The bandwidth of the current mirror is often dominated by the input time constant, which can be expressed as:

$$BW = \frac{g_{in}}{2\pi C_{in}} = \frac{g_{m1}}{2\pi(C_{gb1} + C_{gb2} + C_{gs1} + C_{gs2})} \quad (20)$$

which can roughly be approximated as:

$$BW \cong \frac{\mu n \varphi_t}{(1+A_I)\pi L^2}\left(\sqrt{1+i_f} - 1\right) \quad (21)$$

The bandwidth is directly proportional to the transconductance $g_m$ since the sum of the capacitances in the denominator of (20) is almost independent of $i_f$. Indeed, the denominator of (20) can be written as approximately $C_{ox}WL/2(1+A_I)$ and (21) results as a consequence of this approximation. Although this expression does not take into account the effect of drain and source overlap capacitances, these capacitances can be easily added to the denominator of (20). Neglecting this effect has led to a slight error in the theoretical bandwidth.

### 2.5. Input and Output Voltages

The minimum power supply is limited by the required input gate to source voltage. This voltage can be directly derived from (5):

$$V_{\mathrm{Im}in} = V_T + n\varphi_t\left(\sqrt{1+i_f} - 2 + \ln\left(\sqrt{1+i_f} - 1\right)\right) \quad (22)$$

For the weak inversion region ($i_f < 1$), the current mirror can operate properly from a supply voltage as low as 1V while having sufficient room for the signal swing. Accordingly, the weak inversion region is more appropriate for very low voltage applications. However, the bandwidth is reduced as $i_f$ decreases. This limits the use of this region to low frequency applications. In contrast, for the strong inversion region, the input voltage increases rapidly with $i_f$. The corresponding increase in the bandwidth is not as much. For most applications, with modest bandwidth and power supply specifications, the moderate inversion region may be sufficient.

### 2.5. The total harmonic distortion (THD)

The total harmonic distortion of the current mirror is dominated by $V_{T0}$ mismatch. We assume that the total input current is given by:

$$I_1 = I_{bias} + \Delta I_1 \quad (23)$$

where $I_{bias}$ is the bias current and $\Delta I_1$ is the signal current. From Taylor series expansion around $\Delta V_{T0} = 0$, the inversion level in the output transistor M2 is given by:

$$i_{f2} \cong i_{f1} - \frac{2}{n\varphi_t}\left(\sqrt{1+i_{f1}} - 1\right)\Delta V_T \quad (24)$$

where $\Delta V_T = V_{T2} - V_{T1}$.

Now, if $I_1$ is a sinusoidal current with amplitude $\Delta I_{1m}$, then the second and third order harmonics in the output current can be calculated. Let $i_{f1} = i_{fbias} + \Delta i_{f1}$, then by expanding (24) around $\Delta i_{f1} = 0$, it can be shown that the second and third order harmonics due to $V_{T0}$ mismatch are approximated by:

$$HD_2 = \frac{\Delta V_T}{8n\varphi_t}\frac{i_{f1}}{\left(1+i_{f1}\right)^{\frac{3}{2}}}\frac{\Delta I_{1m}}{I_{S1} i_{f1}} \quad (25)$$

$$HD_3 = \frac{\Delta V_T}{32n\varphi_t}\frac{i_{f1}^2}{\left(1+i_{f1}\right)^{\frac{5}{2}}}\left(\frac{\Delta I_{1m}}{I_{S1} i_{f1}}\right)^2 \quad (26)$$

## 3. CONCLUSION

The basic CMOS current mirror has been analyzed using the all-region model. Expressions for design specifications of current mirrors as function of the inversion level were provided. Measurement results showed the model accuracy despite its relative simplicity. At least in the CGE prediction, the all-region model gives better accuracy than the more complicated BSIM models.


## 4. ACKNOWLEDGEMENT

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