MOSVIEW: A Graphical Tool for MOS Analog Design

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Abstract

This paper presents MOSVIEW, a graphical tool for transistor-level design of analog MOS circuits. MOSVIEW allows students to visualize and explore the design space in order to size and bias the transistor for a given set of specifications.

1. Introduction

In the present digital age, there is growing need for analog designers. Because of the increasing complexity of the chips and the trend to include sensors and communication interfaces inside them, most ICs will have analog components in the near future [1]. The multiplicity of performance specifications, the dependence of circuit behavior on technology variations, the diversity of element sizes and shapes make the analog design problem difficult. Only recently have analog designers received some help from electronic design automation (EDA) software [1], and much of their work continues to be done empirically, using repeatedly time-consuming simulations. The natural difficulties of analog design are worsened by the lack of good device models implemented in circuit simulators and by the fact that modern electrical engineering curricula do not provide adequate preparation for analog design.

In this paper we present MOSVIEW, a graphical tool for transistor-level design that allows rapid exploration of the design space. With MOSVIEW the students can easily analyze design tradeoffs and develop an intuition on transistor sizing for analog circuits. The graphical tool uses MATLAB and is based on the ACM model of the MOS transistor [2], which covers all transistor operating regions and has fewer parameters than other models.

2. ACM model for analog design [2]

The ACM model was developed considering the needs of analog designers. The fundamental parameter of the ACM model is the normalization current I_S, which contains the basic information on the device, namely geometry, technology, and temperature. In ACM, the large and small signal parameters of the saturated MOSFET are simple rational functions of i_f and of transistor parameters I_S, C_{ox} and n, being C_{ox} the total oxide capacitance and n the slope factor. $i_f = I_D/I_S$, the normalized drain current of a saturated MOSFET, indicates the inversion degree at the source end of the channel.

3. MOSVIEW

The current version of MOSVIEW accepts four usual specifications for the problem of analog transistor sizing. In all cases the design space is represented using the normalized channel length as the abscissa and the normalized intrinsic gain as the ordinate (Figs. 1 - 4). In more traditional design approaches, the design space is not fully explored because the channel length and the inversion level are often fixed (e. g.: channel length L=2 or 3 L_{min}, gate voltage overdrive V_{GS}-V_{TH}=200mV).

In the figures shown, the straight lines represent the linear dependence of the voltage gain on the channel length for constant values of i_f (here, i_f = 2, 8, 32, 128, 512). The curves represent constant cutoff frequency transistors. In any case, the shaded area represents the design space. All graphics were plotted using the same technological parameters, $L_{min} = 1\mu m$, $C'_{ox} = 2fF/\mu m^2$, n = 1.25, $\mu_0 = 500 \cdot 10^8 \mu m^2/Vs$, and $V_E = 5V/\mu m$. V_E is the Early voltage per unit length and Ut= 25.9mV. Amplifiers I and II described below are common source amplifiers.

Amplifier I: The specifications are a fixed transconductance (g_m), a range of intrinsic cutoff frequencies (f_{Tmin}, f_{Tmax}) and a minimum value for the voltage gain (A_{Vmin}). In Fig. 1, $g_m = 4\mu A/V$, f_{Tmin} = 1MHz, f_{Tmax} = 10MHz, and A_{Vmin} = 1000.

Amplifier II: The specs are a fixed transconductance (g_m), a range of frequencies (f_{Tmin}, f_{Tmax}) and a minimum value for the drain current (I_{Dmin}). Fig. 2 shows the design area for a transistor operating with $g_m = 4\mu A/V$, f_{Tmin} = 1MHz, f_{Tmax} = 10MHz and I_{Dmin} = 200nA. Here, the straight bold line represents I_{Dmin}.

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Transconductor: The specifications given are a fixed transconductance (g_m), a minimum value of the cutoff frequency (f_{Tmin}) and a range of inversion levels (i_{fmin}, i_{fmax}). In Fig. 3 $g_m = 4\mu A/V$, $f_{Tmin} = 1MHz$, $i_{fmin} = 8$ and $i_{fmax} = 100$. The straight bold lines represent i_{fmin} and i_{fmax}.

Current Mirror: The specs are drain current (I_D), minimum cutoff frequency (f_{Tmin}), and a maximum value for the inversion level (i_{fmax}). The design space for I_D = 300nA, f_{Tmin} = 1MHz and i_{fmax} = 200 is shown in Fig. 4, where the solid line represents i_{fmax}.

Because the ACM model includes noise, future versions of MOSVIEW will include noise specifications.

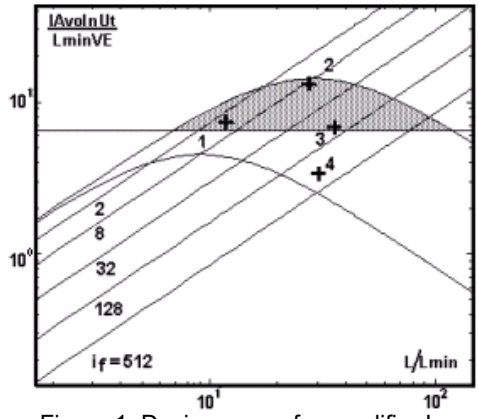

Figure 1. Design space for amplifier I.

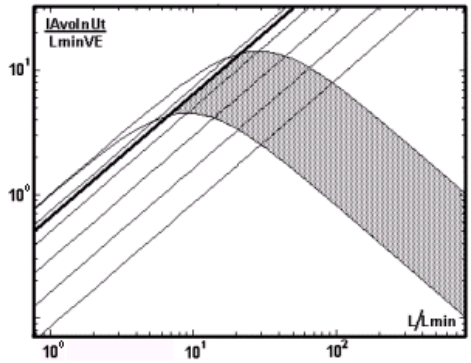

Figure 2. Design space for amplifier II.

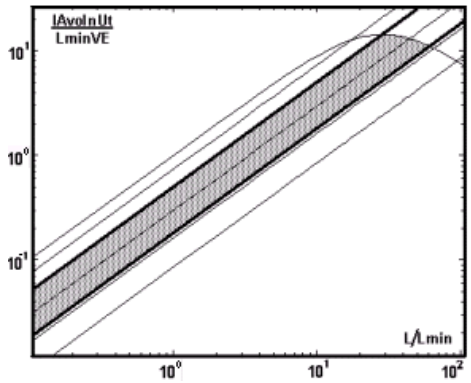

Figure 3. Design space for the transconductor.

4. Simulation Results

For Fig. 1, some points in the design space were selected. Table I shows the characteristics of the transistors represented for each point (point 4 doesn't meet the gain spec). The maximum intrinsic gain of the transistor is for the transistor with the lowest transition frequency f_T. On the other hand, the minimum area is associated with the maximum cutoff frequency. Finally, the minimum current consumption transistor is achieved with the lowest inversion level.

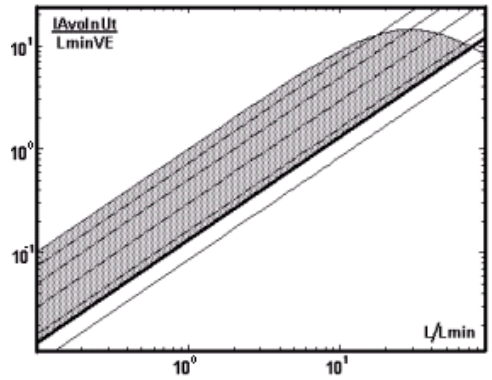

Figure 4. Design space for the current mirror.

Table I. Parameters of the amplifier of Fig. 01.

	1	2	3	4
i_f	4.2	8.05	70.01	*308.36*
g_m/I_D [1/V]	18.9087	15.4655	6.6044	*3.30092*
g_m [uA/V]	4	4	4	*4*
I_D [nA]	211.54	258.64	605.65	*1208.76*
V_{DSsat} [V]	0.1365	0.1553	0.2954	*0.53224*
A_{VO}	1283.2	2107.6	1014.4	*514.4*
f_T [MHz]	2.85	1.11	3.2	*7.15*
L [um]	13.6	27.3	30.9	*30.9*
W [um]	16.4	21	6.4	*2.9*
WL [um^2]	223.04	573.3	197.76	*89.61*

5. Conclusions

MOSVIEW, a graphical tool to size analog MOS transistors, has been developed. With MOSVIEW the designer can rapidly analyze design tradeoffs and develop an intuition on MOS transistor sizing and biasing for analog circuits.

6. References

[1] B. Martin, "Automation comes to analog", IEEE Spectrum, vol. 39, no. 6, pp.70-75, June 2001.

[2] A. I. A. Cunha, M. C. Schneider and C. Galup-Montoro, "An MOS transistor model for analog circuit design", IEEE JSSC, vol. 33, no. 10, pp. 1510-1519, October 1998.