The Advanced Compact MOSFET (ACM) Model for Circuit Analysis and Design

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Abstract- Most of the new generation compact models for the MOSFET have many commonalities since they are based on the same main approximations: gradual channel, charge-sheet, and depletion charge linearization. In this study we show that if we include some additional physics-consistent conditions for the MOSFET equations we obtain a very compact model that we call the advanced compact MOSFET (ACM) model. The core ACM model, design-oriented equations, parameter extraction, and a design example are presented.

Keywords: MOS transistor, MOSFET models, compact models, transistor-level design

I. Introduction

Compact models for the MOSFET are based on the gradual channel approximation in which the longitudinal component of the electric field is assumed to be much smaller than the transversal component [1]. Based essentially on the gradual channel approximation, the Pao-Sah formula has served as a reference to test the accuracy of compact models [2], but has been considered numerically too involved to be used as the core of a compact model. With the addition of the charge-sheet approximation to the gradual channel approximation, surface potential models have been developed since the pioneering work in [3], [4]. The main drawbacks of these first generation surface potential models are their cumbersome expressions for total charges and capacitances. To simplify the current and total stored charge expressions, the linearization of the depletion charge terms has been widely adopted [5]-[7].

In this study, after reviewing the Pao-Sah formula and the main approximations for compact models, we discuss the consistency of the compact equation for the current with the Pao-Sah formulation. A very simple fully-consistent model is obtained, which is summarized in Section IV. Parameter extraction is presented in Section V and a design example is developed in Section VI.

II Pao-Sah current expression

The Pao-Sah equation [8] for the drain current is

$$I_D = -\mu W Q_I' \frac{dV_C}{dy} \qquad (1)$$

where W is the channel width, μ is the carrier mobility, Q_I' is the inversion charge density, y is the distance along the channel, and V_C is the channel potential, which ranges between V_S and V_D, the source-to-bulk and drain-to-bulk potentials, respectively. Expression (1), which assumes μ to be independent of the depth x, includes both the drift and diffusion transport mechanisms, and gives an exact model of the long-channel MOSFET. For this reason, (1) is used as a golden reference to test the accuracy of compact models.

Since the current is constant along the channel, the integration of (1), from source to drain yields

$$I_D = -\frac{W}{L}\int_{V_S}^{V_D} \mu Q_I'(V_C)\,dV_C \qquad (2)$$

where L is the channel length.

The small-signal output conductance of the transistor is defined as

$$g_d = \left.\frac{\partial I_D}{\partial V_D}\right|_{V_G,V_S} \qquad (3)$$

where V_G *is* the gate-to-bulk potential. Applying the definition of (3) to the Pao-Sah formula (2), we obtain

$$g_d = -\frac{W}{L}\mu Q_I'(V_D)\,. \qquad (4)$$

It is remarkable that the very simple Eq. (4) is valid from weak inversion (where the current transport is dominated by diffusion) to strong inversion (where drift dominates).

III Basic approximations for compact models

A. *Charge-Sheet Approximation*

Representing the three-terminal MOS structure by a capacitive model [9] as shown in Fig. 1, it follows that

$$dQ_I' = C_i'\left(dV_C - d\phi_s\right) \qquad (5)$$

where C_i' is the inversion capacitance and ϕ_s is the surface potential.

The charge-sheet approximation assumes that the inversion layer has zero thickness. It can be shown that, using this approximation, the inversion capacitance reduces to

$$C_i' = -\frac{Q_I'}{\phi_t}. \qquad (6)$$

It is worth observing that (6) is only accurate in weak inversion. In effect, the resolution of the Poisson equation in the semiconductor shows that the logarithmic slope of the $Q_I'(\phi_s)$ curve varies from $1/\phi_t$ in weak inversion to $1/2\phi_t$ deep in strong inversion [10].

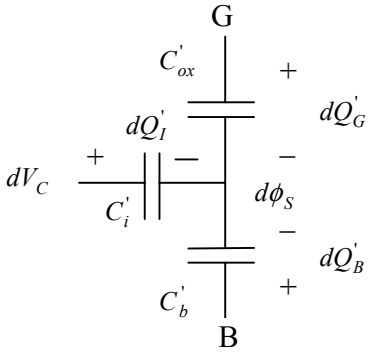


Fig. 1: Small-signal model for the three-terminal MOSFET

Substituting (6) into (5) we get [11, 12]

$$\frac{dV_C}{d\phi_s} = 1 - \frac{\phi_t}{Q_I'}\frac{dQ_I'}{d\phi_s}. \qquad (7)$$

Finally, from (1) and (7) the charge-sheet expression of the current results

$$I_D = I_{drift} + I_{diff} = -\mu W Q_I' \frac{d\phi_s}{dy} + \mu W \phi_t \frac{dQ_I'}{dy} \qquad (8)$$

where the first term corresponds to drift and the second to the diffusion component of the current.

B. Linearization of the Inversion Charge Density vs. Surface Potential

In the charge-sheet approximation, the inversion charge density is calculated as the total semiconductor charge minus the depletion charge density as indicated below

$$Q_I' = -C_{ox}'\left(V_G - V_{FB} - \phi_s - \gamma\sqrt{\phi_s - \phi_t}\right) \qquad (9)$$

where C_{ox}' is the oxide capacitance per unit area, V_G is the gate-to-bulk potential, V_{FB} is the flat-band potential and γ is the body effect factor.

For constant V_G, it follows from (9) that

$$dQ_I' = nC_{ox}'d\phi_s, \qquad (10)$$

where

$$n = 1 + \frac{\gamma}{2\sqrt{\phi_s - \phi_t}} \qquad (11)$$

is the slope factor. In some models, *e.g.* [6] and [13], n is a function of the gate voltage only, while in others, *e.g.* [5] and [14], n is also a function of the channel voltage.

Substituting (10) into (8), and assuming that both n and μ are constant along the channel, the integration of the resulting equation from source to drain gives the current in terms of the inversion charge densities at the source and drain ends of the channel [5], [6]:

$$I_D = \frac{\mu W}{L}\left[\frac{Q_{IS}'^2 - Q_{ID}'^2}{2nC_{ox}'} - \phi_t\left(Q_{IS}' - Q_{ID}'\right)\right]. \qquad (12)$$

C. Consistency of the Current Equation with the Pao-Sah Formulation

To illustrate the advantage of choosing n as a function of the gate voltage only, let us consider the limit case of (12) in the familiar strong inversion (SI) region, where the inversion charge density is a linear function of the applied voltages [13] as given below

$$Q_I' = -C_{ox}'\left(V_G - V_{T0} - nV_C\right) \qquad (13)$$

where V_{T0} is the equilibrium threshold voltage. Substituting (13) into (12) and neglecting the linear terms in (12) we obtain the classical SI current law

$$I_D = \mu C_{ox}'\frac{W}{L}\left[V_G - V_{T0} - \frac{n}{2}\left(V_S + V_D\right)\right]\left(V_D - V_S\right). \qquad (14)$$

For n=1 (neglecting the body effect), (14) reduces to the classical textbook expression [1]. The output conductance of a transistor modeled by (14) is, for both slope factor and mobility independent of the channel voltage, given by

$$g_d = \left.\frac{\partial I_D}{\partial V_D}\right|_{V_G, V_S} = \mu C_{ox}'\frac{W}{L}\left(V_G - V_{T0} - nV_D\right), \qquad (15)$$

which complies with (4).

Let us now consider the all-region current equation (12), assuming that n and μ are functions of the gate voltage only. The output conductance calculated differentiating (12) is

$$g_d = \left.\frac{\partial I_D}{\partial V_D}\right|_{V_G, V_S} = \frac{\mu W}{L}\left[\frac{-Q_{ID}'}{nC_{ox}'} + \phi_t\right]\frac{dQ_{ID}'}{dV_D}. \qquad (16)$$

From (4) and (16) it follows that

$$dQ_{ID}'\left(\frac{1}{nC_{ox}'} - \frac{\phi_t}{Q_{ID}'}\right) = dV_D. \qquad (17)$$

Equation (17) provides the condition for consistency between the Pao-Sah formula (1) and the charge-sheet current expression (12). Using (17) to calculate the derivative of the channel charge allows simple expressions for all the small-signal parameters, namely (trans)conductances and (trans)capacitances.

D. Model Consistency for the Series Association of MOSFETs [15]

The consistency of a transistor model for the series association of MOSFETs, as shown in Fig. 2, is an important benchmark for the following reasons: (i) the MOSFET channel can be considered as a double-contact device with a

distributed channel composed of small-channel elements connected in series, (ii) some modern bulk transistors, *e.g.* with pocket-implanted regions can be described as the series association of transistors with different electrical parameters, (iii) integrated circuit designers often make use of series association of transistors to obtain very accurate ratios of numbers, *e.g.* a current mirror where a very high (or low) gain is required, (iv) some accurate models for transistor noise and matching [19], [20] are calculated by adding the individual contributions of elementary MOSFET channels connected in series. It is worth noting that several dc, noise, and matching models [19], [20] do not represent consistently the series association of MOSFETs, even though this property seems to be quite obvious.

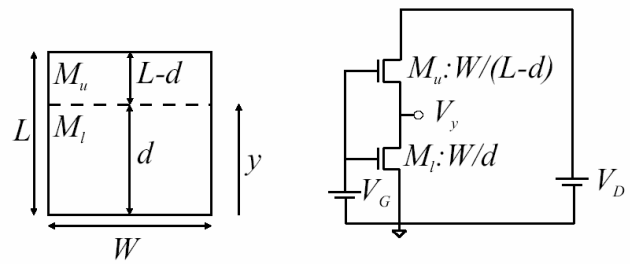


Fig. 2 Virtual cut of a transistor into two slices and its representation as a series association of transistors.

Since the current equation in (12), with n and μ as functions of the gate voltage only, is consistent with the Pao-Sah equation, the current law (12) represents consistently the series association of transistors.

IV The ACM Core Model

A. Effective mobility and velocity saturation

The effect of carrier velocity saturation is included in the mobility model as [5], [16]

$$\mu = \frac{\mu_s}{1+\frac{\mu_s}{v_{sat}}\frac{d\phi_s}{dy}}, \qquad (18)$$

where v_{sat} is the saturation velocity and μ_s is the mobility of the long-channel device, which is assumed to be a function of V_G only. From (8), (10) and (18) the relationship between the differential of channel length and the differential of inversion charge is

$$dy = -\frac{\mu_s W}{nC'_{ox}I_D}\left(Q'_I - nC'_{ox}\phi_t + \frac{I_D}{Wv_{sat}}\right)dQ'_I. \qquad (19)$$

Since n depends on V_G only, and I_D is constant along the channel, we can define a virtual charge density that differs from the real charge by a constant term, *i.e.*

$$Q'_V = Q'_I - nC'_{ox}\phi_t + \frac{I_D}{Wv_{sat}}. \qquad (20)$$

Using (20), the total inversion charge stored in the channel is easily calculated as [17]

$$Q_I = W(L-\Delta L)\left[\frac{2}{3}\frac{1+\alpha+\alpha^2}{1+\alpha}Q'_{VS} + nC'_{ox}\phi_t\right] - \frac{LI_D}{v_{sat}}, \qquad (21)$$

where ΔL is the channel length shortening and α is the channel linearity coefficient defined as

$$\alpha = \frac{Q'_{VD}}{Q'_{VS}}. \qquad (22)$$

$\alpha \cong 1$ in weak inversion or in the linear region for $V_{DS} \to 0$, while, for the long-channel device $\alpha \to 0$ in strong inversion saturation. At this point we must emphasize that the choice of the mobility law in (18) is of prime importance for arriving at closed form expressions to calculate charges and capacitances in the short-channel transistor. Additionally, we have obtained for the short-channel MOSFET model expressions which are, in any operating region, similar with the conventional long-channel model in strong inversion [1]. This similarity is an important consequence of the use of the virtual charge as a key variable. In fact, we can obtain the expressions for the model parameters of the short-channel device from the conventional strong inversion equations by simply replacing the inversion charge density with the virtual charge density, which describes both the diffusion and saturation velocity phenomena, in addition to drift transport.

The integration of (19) along the channel allows the calculation of the drain current. Normalizing the charges with respect to the thermal charge $Q'_{IP} = -nC'_{ox}\phi_t$ and the current with respect to the normalization current

$$I_S = \frac{W}{L}\mu_s nC'_{ox}\frac{\phi_t^2}{2}, \qquad (23)$$

the drain current equation is written as

$$i_D = \frac{(q'_{IS}+q'_{ID}+2)}{1+\zeta(q'_{IS}-q'_{ID})}(q'_{IS}-q'_{ID}), \qquad (24)$$

where i_D and $q'_{IS(D)}$ are the normalized drain current and source (drain) inversion charge density, respectively. The dimensionless short-channel parameter ζ is defined as

$$\zeta = \phi_t\mu_s / Lv_{sat}. \qquad (25)$$

ζ can be regarded as the ratio of the diffusion-related velocity $\mu_s(\phi_t/L)$ at the source of a saturated transistor to the saturation velocity v_{sat}. For long channel transistors, $\zeta \cong 0$. It is worth noting that (24) represents consistently the series association of transistors.

The maximum current that can flow in the channel is limited by the maximum carrier velocity. When electrons at the drain end of the channel reach the saturation velocity, the normalized drain current is expressed as

$$i_{Dsat} = \frac{I_{Dsat}}{I_S} = -\frac{Wv_{sat}Q'_{IDsat}}{I_S} = \frac{2}{\zeta}q'_{IDsat}. \qquad (26)$$

The saturation condition, relating the source charge to the drain charge in saturation is obtained imposing the equality of

the general expression of the drain current (24) with the saturated current (26). Thus, the saturation condition is written as

$$q'_{IS} = \sqrt{1+\frac{2}{\zeta}q'_{IDsat}} - 1 + q'_{IDsat} \qquad (27)$$

or

$$q'_{IS} = \sqrt{1+i_{Dsat}} - 1 + \frac{\zeta}{2} i_{Dsat} . \qquad (28)$$

The relationship between applied voltages and charges is obtained integrating (17) from source to drain, yielding

$$\frac{V_{DS}}{\phi_t} = q'_{IS} - q'_{ID} + \ln\left(\frac{q'_{IS}}{q'_{ID}}\right). \qquad (29)$$

B. Long-Channel Model [18]

Table I gives the main equations of the MOSFET in terms of the normalized inversion charge densities. Expressions similar to some of those shown in Table I have been used for hand analysis [21] and automated design [22] of analog circuits. V_P is the pinch-off voltage that can be approximated by $V_P \cong (V_G - V_{T0})/n$ for hand analysis [13].

Due to the symmetry of the transistor, the expressions for capacitances C_{gd}, C_{bd}, and C_{sd} are obtained from C_{gs}, C_{bs}, and C_{ds}, respectively, by simply exchanging $S \leftrightarrow D$ and $\alpha \leftrightarrow 1/\alpha$. The small-signal schematic of Fig. 3 preserves the inherent symmetry of the MOSFET.

τ_1 is the first-order time constant for non-quasi-static operation. For operating frequencies such that $\omega\tau_1 << 1$, the small-signal model of Fig. 3 represents accurately the MOSFET ac behavior.

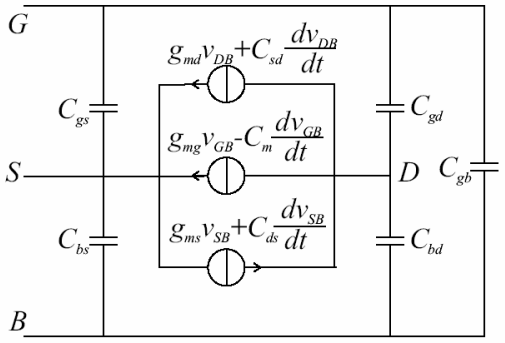


Fig. 3 Simplified small signal MOSFET model.

C. Mismatch and Noise Modeling [19, 20]

To calculate the effect of local fluctuations on the drain current along the channel, we split the transistor into 3 series elements: an upper transistor, a lower transistor, and a small channel element. Small-signal analysis allows one to calculate the effect of the local current fluctuation ($i_{\Delta A}$) on the drain current deviation (ΔI_d), as shown in Fig. 4. The current division between the channel element and the equivalent small signal resistance of the rest of the channel gives $\Delta I_d = (\Delta y/L) i_{\Delta A}$ in the case of constant mobility.

This very simple result for the current division, proportional to a geometric ratio, is a consequence of the Pao-Sah formulation for the drain current (1), *i.e.*, the conductance of the channel element and the transconductances of the upper and lower transistors are proportional to the local charge density. The effect of a non constant mobility can be taken into account as developed in [10]. Considering the fluctuation of the drain current around its nominal value as the sum of contributions of local fluctuations along the channel, the mismatch and noise formulas in Table I result. Fig. 5 shows an example of the fitting of the mismatch model from weak ($i_f \leq 1$) to strong inversion ($i_f \geq 100$) and from the linear to the saturation region.

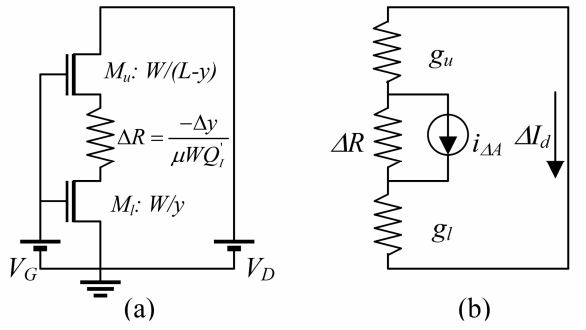


Fig. 4 Splitting of a transistor into three series elements: (a) transistor equivalent circuit and (b) small-signal equivalent circuit.

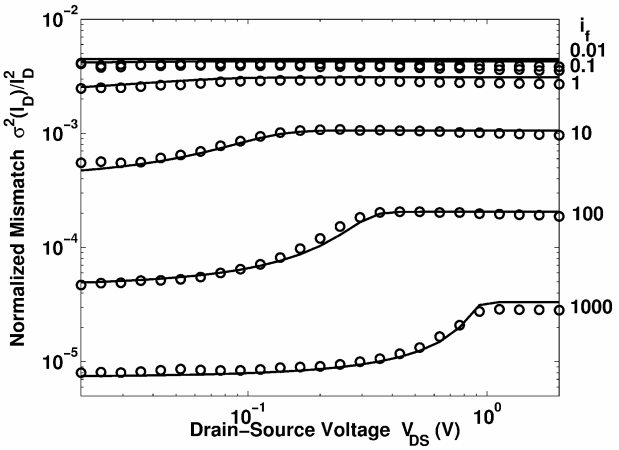


Fig. 5 Normalized mismatch of 3µm/2µm (W/L) n-channel MOSFETs of a TSMC 0.35 µm process, from linear (20mV) to saturation (2V) region, under a wide range of inversion levels (i_f is defined in Table II). Circles represent measurements while solid lines represent the mismatch model [10], [20].

TABLE I
LONG-CHANNEL MOSFET MODEL

Variable	Charge-Based Expression
I_D	$I_S\left(q'_{IS}-q'_{ID}\right)\left(q'_{IS}+q'_{ID}+2\right)$
$g_m=\frac{g_{ms}-g_{md}}{n}$	$\frac{2I_S}{n\phi_t}\left(q'_{IS}-q'_{ID}\right)$
C_{gs}	$\frac{2}{3}C_{ox}\frac{1+2\alpha}{(1+\alpha)^2}\frac{q'_{IS}}{1+q'_{IS}}$
C_{bs}	$(n-1)C_{gs}$
C_{gb}=C_{bg}	$\frac{n-1}{n}\left(C_{ox}-C_{gs}-C_{gd}\right)$
C_{ds}	$-\frac{4}{15}nC_{ox}\frac{1+3\alpha+\alpha^2}{(1+\alpha)^3}\frac{q'_{IS}}{1+q'_{IS}}$
C_m=C_{dg}-C_{gd}	$\frac{C_{sd}-C_{ds}}{n}$
τ_1	$\frac{L^2}{\mu\phi_t}\frac{4}{15}\frac{1+3\alpha+\alpha^2}{(1+\alpha)^3}\frac{1}{1+q'_{IS}}$
{1} $\frac{\sigma^2_{I_D}}{I_D^2}$	$\frac{q^2N_{oi}\mu}{L^2nC'_{ox}I_D}\ln\left(\frac{q'_{IS}+1}{q'_{ID}+1}\right)$
{2} $\frac{\overline{\delta I_D^2}}{I_D^2\Delta f}$	$\frac{q^2N_{ot}\mu}{L^2nC'_{ox}I_D}\frac{1}{f}\ln\left(\frac{q'_{IS}+1}{q'_{ID}+1}\right)$
{3} $\frac{\overline{\delta I_D^2}}{\Delta f}$	$4kT\mu\frac{W}{L}\left[\frac{2}{3}\frac{1+\alpha+\alpha^2}{1+\alpha}(q'_{IS}+1)-1\right]nC'_{ox}\phi_t$
V_P-$V_{S(D)}$	$\phi_t\left[q'_{IS(D)}-1+\ln\left(q'_{IS(D)}\right)\right]$

N_{oi} and N_{ot} are the equivalent densities of impurities and oxide traps for the mismatch {1} and flicker noise {2} expressions, respectively. {3} is the thermal noise power spectral density.

D. The Unified Charge Control Model (UCCM)

Integrating (17) between the pinch-off voltage V_P and $V_{S(D)}$, yields the UCCM in the last row of Table I. It is interesting to observe that when calculating the charge densities through UCCM we are using exactly the same approximations as in the formula of the current, guaranteeing a fully consistent model.

To obtain accurate values of the inversion charge the linear approximation of the pinch-off voltage in terms of the gate voltage is not appropriate. Using V_P given by (30-31), UCCM yields inversion charge values as accurate as those obtained using the surface potential model.

$$V_P=\phi_{sa}-\phi_0 \qquad (30)$$

$$\phi_0=2\phi_F+\phi_t\left[1+\ln\left(\frac{n}{n-1}\right)\right]. \qquad (31)$$

ϕ_{sa} [1] is the surface potential calculated disregarding the channel charge and ϕ_F is the Fermi potential in the bulk.

In Fig. 6 the inversion charge density curve and its first and second order derivatives, calculated either numerically, or using UCCM, or the surface potential model, are plotted. As can be seen in Fig. 6, UCCM is as accurate as the surface potential model for the calculation of the derivatives, and consequently, to determine distortion.

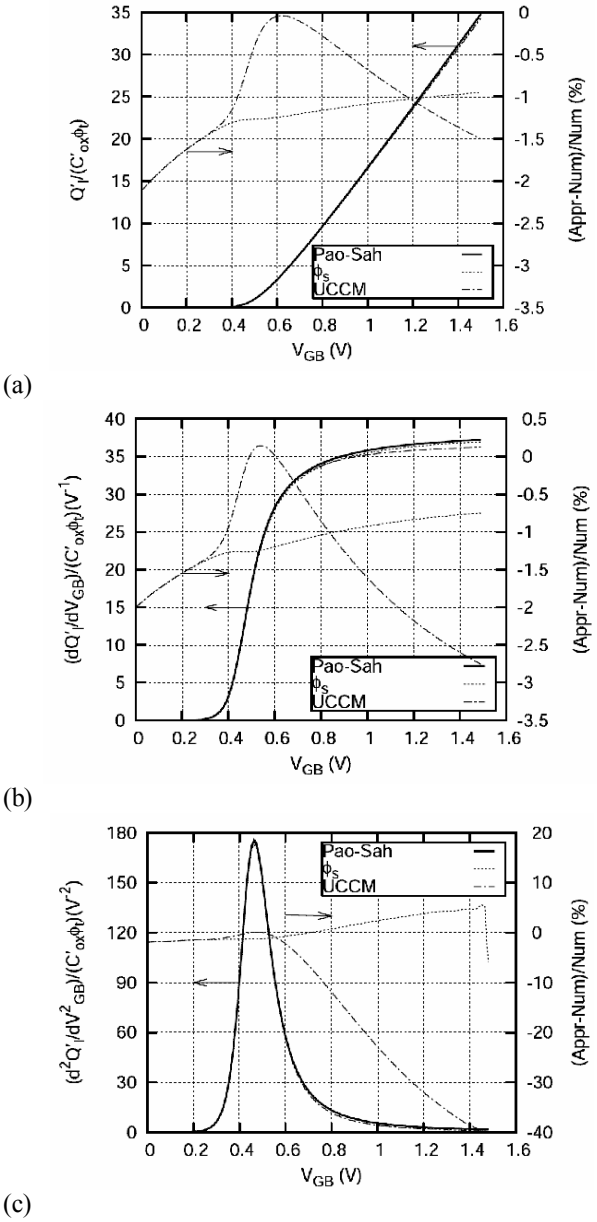


Fig 6 (a) Inversion charge density, (b) first and (c) second derivatives of the inversion charge density calculated either numerically (Pao-Sah) (——), or using the surface potential (····) and UCCM models (— · —) .

E. Design-oriented expressions

Since analog circuits are generally current-biased and the transistors most often operate in saturation, we provide in Table II a set of useful expressions of parameters in terms of the normalized drain current, i_f, which represents the inversion level at the source. A low i_f ($\leq$1) is associated with weak inversion whereas a high i_f ($\geq$100) is associated with strong inversion. I_{SQ} is the sheet normalization current which, for practical purposes, can be taken as a technological parameter due to its usually small variation for the whole range of gate voltages. The transconductance g_m depends on both transistor aspect ratio and inversion level. The maximum transconductance-to-current ratio, equal to $1/(n\phi_t)$ is achieved in weak inversion. Once I_D and g_m have been determined, the aspect ratio is calculated according to the expression of the 5th row in Table II. The approximate expression for the drain-to-source saturation voltage is very useful for the determination of biasing circuits. f_T, the transition frequency, is the frequency at which the current gain in the common-source configuration equals one. The formulas that follow allow the calculation of mismatch, flicker noise, thermal noise, and finally, we have the unified current-control model (UICM), which gives the normalized current in terms of the gate-to-bulk and source-to-bulk voltages.

V Parameter Extraction

The charge-based expressions of Table I give

$$\frac{\frac{g_m}{I_D}}{\left(\frac{g_m}{I_D}\right)_{\max}} = \frac{2}{q'_{IS} + q'_{ID} + 2} \qquad (32)$$

where $\left(g_m / I_D\right)_{max} = 1/\left(n\phi_t\right)$ is the value of the transconductance-to-current ratio deep in weak inversion.

In the ACM model the threshold voltage is defined as the value of V_G for which the drift and diffusion components of the drain current are equal $\left(q'_I = 1\right)$. Applying this criterion to (32) for small V_{DS} ($q'_{IS} \cong q'_{ID}$) and assuming n to be almost constant, allows the extraction of the threshold voltage from the g_m/I_D characteristic (Fig.7) by simply measuring the peak value of g_m/I_D and determining the gate voltage at which the value of g_m/I_D drops to one-half of the peak value. The slight variations in the slope factor and mobility with gate voltage are negligible over the required measurement range. Applying the previously described methodology to the curve generated using the PSP model in ELDO, we find V_{T0}=208 mV and I_{SQ}=158 nA. To generate the transconductance-to-current ratio in Fig. 7 associated with the ACM model we embedded the values of V_{T0}=208 mV and I_{SQ}=158 nA as well as the values of γ, $2\phi_F$ into the ACM equations. The PSP and the ACM models fit very well in weak and moderate inversion, over several decades of current. In the design example shown in Section VI, the transistors operate in moderate inversion.

TABLE II
Design-Oriented Expressions for the Long-Channel MOSFET in Saturation

Parameter	Expression
i_f	I_D / I_S
I_S	$I_{SQ}\frac{W}{L} = \frac{\mu C'_{ox} n \phi_t^2}{2}\frac{W}{L}$
g_m	$\frac{I_D}{n\phi_t}\frac{2}{\sqrt{1+i_f}+1}$
$\frac{L}{W}$	$\frac{2\mu C'_{ox}\phi_t}{g_m}\left(\frac{I_D}{n g_m \phi_t}-1\right)$
V_{DSsat}	$\phi_t\left(\sqrt{1+i_f}+3\right)$
f_T	$\frac{\mu\phi_t}{\pi L^2}\left(\sqrt{1+i_f}-1\right)$
$\frac{\sigma^2_{I_D}}{I_D^2}$	$\frac{N_{oi}}{WL\left(nC'_{ox}\phi_t/q\right)^2}\frac{\ln\left(1+i_f\right)}{i_f}$
$\frac{\overline{\delta I_D^2}}{I_D^2 \Delta f}$	$\frac{N_{ot}}{WL\left(nC'_{ox}\phi_t/q\right)^2}\frac{\ln\left(1+i_f\right)}{i_f}\frac{1}{f}$
$\frac{\overline{\delta I_D^2}}{\Delta f}$	$\frac{8}{3}kTng_m\frac{\sqrt{1+i_f}+1/2}{\sqrt{1+i_f}+1}$
V_P-V_S	$\phi_t\left[\sqrt{1+i_f}-2+\ln\left(\sqrt{1+i_f}-1\right)\right]$

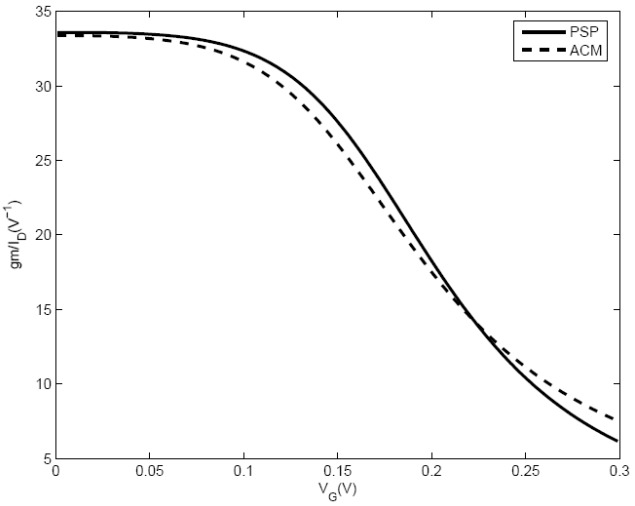


Fig. 7 Transconductance-to-current characteristic of an n-MOS transistor for V_{DS}=1mV. The PSP curve was used to determine both the threshold voltage and the sheet specific current.

VI Design Example

To demonstrate the usefulness of the ACM model, we designed a folded cascode operational amplifier using the ACM equations for later comparison with simulation results from PSP. The specs and simulation results for the op amp are given in Table III whereas the topology is shown in Fig. 8.

The op amp was designed using the ACM parameters extracted from MOSFET characteristics simulated with version 6.6, release 2005.3, of ELDO using the level 70 (PSP) model with default parameters. In the default technology, the p-channel and n-channel transistors are "symmetric" devices. This symmetry is not a problem for our purpose, which is to demonstrate the close proximity between the results of the ACM equations and those from simulation using the PSP model.

The first parameter determined in our design was the transconductance g_{m1} of the input transistors from

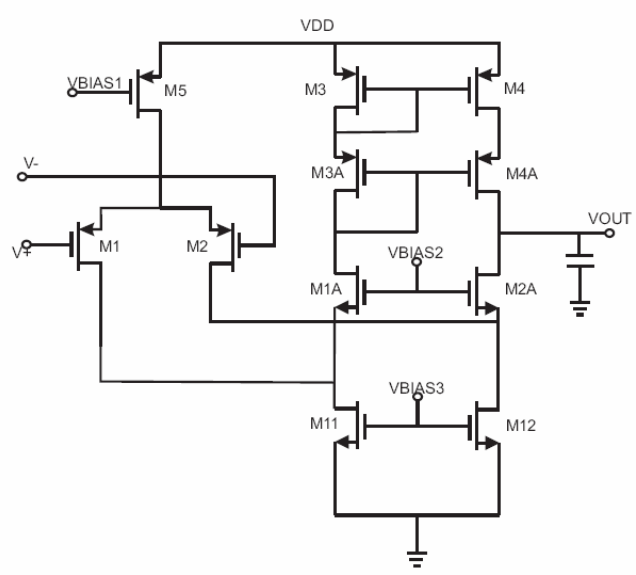
$$g_{m1} = 2\pi.GBW.C_L, \qquad (33)$$

which gives g_{m1}= 314 μA/V. The minimum current that meets the transconductance specification is obtained in weak inversion, *i.e.,* making $i_f \to 0$ in the expression of g_m/I_D in Table II. One can easily verify that, for $i_f \to 0$, $g_m \to I_D/n\phi_t$. Therefore, the minimum current of the input transistors M1 and M2 is I_{D1min}= 9.1 μA (we have used n=1.12 and ϕ_t=25.9 m*V*). In our design we have chosen the commonly employed relationship between currents $I_{D11}= I_{D12}=I_{D5}$. In this way, both the rising and falling slew rates are equal to I_{D5}/C_L. Therefore, to comply with the required slew rate spec, we need I_{D5}=2I_{D1}>20 μA. We decided to choose the bias current I_{D5}=27 μA, which is slightly higher than the minimum required to satisfy the slew rate specification. Using I_{D1}=13.5 μA together with g_{m1}= 314 μA/V we find the inversion level $i_{f1}\cong$3. We decided to set the inversion levels of all transistors, except one in the bias network, equal to 3. The advantage of having such a low inversion level is that the saturation voltage of the transistors is around 5$\phi_t\cong$130 mV, a relatively small value. Once we had chosen the drain current of the transistors, we could readily find the aspect ratios using the expression in Table II, which gives *L/W* as a function of the drain current and transconductance, besides the technological parameters.

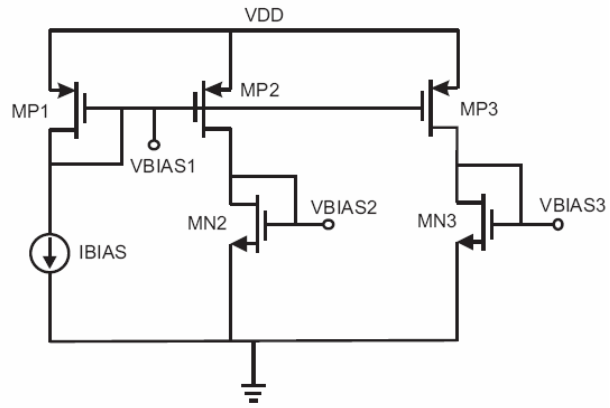
Table III – Specifications and simulation results of the folded-cascode amplifier

	Spec	Simulation	Unit
V_{DD}	1.2	1.2	V
C_L	5	5	pF
GBW	10	9.77	MHz
A_{V0}	>100	141	dB
SR	>4	5	V/μs
$V_{ICM, max}$	>V_{DD}-0.3	0.9	V
$V_{ICM, min}$	<0.3	0	V
$V_{OCM, max}$	>V_{DD}-0.3	0.9	V
$V_{OCM, min}$	<0.3	0.26	V
Input referred white noise	<100	17.5	nV/Hz$^{1/2}$

Transistors M3A, M3, M4A, M4 form a self-biased cascode current mirror, which is generally assumed to be not a good choice for low-voltage circuitry. In our design, however, the gate-to-source voltage of the diode-connected transistors is relatively small due to both the low threshold voltage and low inversion level.



(a)



(b)

Transistor	L(μm)	W(μm)
M1, M2	0.5	13.5
M11, M12	0.5	27
M3, M4	0.5	13.5
M1A,M2A	0.5	13.5
M3A,M4A	0.5	13.5
M5	0.5	27
MP1, MP2, MP3	0.5	13.5
MN2	2(4x0.5)	3.5
MN3	0.5	13.5

Fig. 8 (a) Folded-cascode op amp. (b) Bias network of the folded-cascode op amp and transistor dimensions. Nominal currents are 27 µA for M5, M11, and M12 and 13.5 µA for all the remaining transistors. The inversion level i_f=3 for all devices, except for MN2, for which i_f=46

The bias network is driven by a current source I_{BIAS}=13.5 μA. Note that the aspect ratios of MP1 (MP2, MP3) and MN3 are equal to one half the aspect ratios of M5 and M11, respectively. On the other hand, the bias voltage V_{BIAS2} must be, at least, equal to the gate-to-source voltage of M1A plus the saturation voltage V_{DSsat} of M11 [23], which is

approximately equal to $5\phi_t \cong 130$ mV. The inversion level of MN3 must be such that

$$V_{GS(MN3)} = V_{BIAS3} = V_{GS(M1A)} + V_{DSsat(M11)} + \Delta V \qquad (34)$$

where ΔV is a safety margin which has been included in the design equations to ensure that the drain voltage of M11 is slightly above the drain saturation voltage. This safety margin prevents M11 from operating in the linear region due to either component mismatch and/or to non accurate dc modeling. In our design we chose $\Delta V \cong 40$ mV. Using the linearized form of UCCM we find that

$$V_{BIAS3} = V_{T0} + n\phi_t \left[\sqrt{1 + i_{f(MN3)}} - 2 + \ln\left(\sqrt{1 + i_{f(MN3)}} - 1 \right) \right] \qquad (35)$$

The term $V_{GS(M1A)}$ can also be found from the linearized UCCM. Since the inversion level of M1A is 3, we write, for M1A

$$\frac{V_{GB(M1A)} - V_{T0}}{n} - V_{SB(M1A)} = 0 \qquad (36)$$

The combination of the three previous equations allowed us to calculate the inversion level of MN3, which is around 46.

VII Summary and Conclusions

A derivation of the ACM model for circuit analysis and design highlighting its consistency with the exact Pao-Sah MOSFET model was presented. Simple formulas for circuit design were summarized and a design example verified by simulations carried out using the PSP model was presented.

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Appendix: Computer Implementation of the ACM Model

The ACM model was implemented into the ELDO simulator using the UDM (User Definable Model) [24] module. The model code was written in C. The algorithm used for the numerical calculation of the inversion charge in the UCCM is the second one presented in [25]. Even though it is an iterative algorithm, only one iteration is necessary to obtain relative errors of less than 10^{-7} in the whole inversion range.

For the calculation of the drain current, the factor $1 + \zeta(q'_{IS} - q'_{ID})$ in the denominator of equation (24) is replaced with a continuous and smooth function to avoid discontinuities in the derivatives of the drain current around $V_{DS}=0$.

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