Design of a Fully Integrated Colpitts Oscillator Operating at V_{DD} below $4kT/q$

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***Abstract* — This paper presents a fully integrated enhanced swing Colpitts oscillator that operates from supply voltages below $4kT/q$. Design equations considering the oscillation frequency and start-up conditions required for operation of the Colpitts oscillator are derived. The oscillator was built with a zero-VT transistor, due to its high drive capability at low voltages. Measurement results obtained for a prototype integrated in the IBM 130 nm technology demonstrated the operation of the oscillator with 86 mV of supply voltage.**

***Index Terms* - Ultra-low-voltage circuits, ultra-low-voltage oscillators, MOSFET analog circuits, zero-VT transistor, energy harvesting.**

I. INTRODUCTION

Emerging applications like wireless sensor networks and implantable medical devices, which require self-powered solutions, have increased dramatically. Ambient energy-harvesting sources, such as mechanical vibrations, thermal gradients, light or RF signals, provide important alternatives for powering silicon-based electronics [1]. The voltage level available from ambient energy sources (excluding light) is generally below 100 mV. The operation of electronics at very low voltages results in advantages such as an increase in the time for active operation and a reduction in the standby power of the circuit [2]

With regard to ultra-low-voltage (ULV) electronics, oscillators are particularly useful for circuits powered by energy harvesting devices such as thermoelectric generators. In effect, the attainment of a dc supply voltage of the order of 500 mV or more for powering state-of-the-art electronics from very low DC voltages requires a time-varying signal usually obtained from an oscillator, as shown in Fig. 1. However, the generation of oscillations from ultra-low voltages is extremely difficult. In recent years some topologies have addressed this subject with the use of, for example, mechanical switches, or a post-fabrication tuned oscillator [3], [4]. However, the design of fully-integrated ULV oscillators continues to be an unsolved problem.

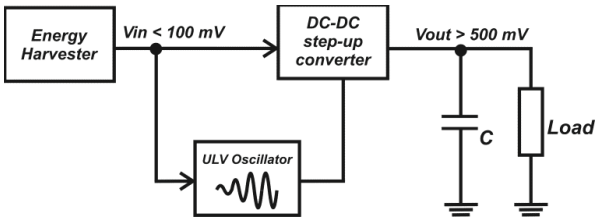

Figure 1. Boost DC-DC converter topology used in energy harvesting applications.

In this paper we present a fully-integrated Colpitts oscillator in which the inductors have a quality factor, Q, of around 10. The oscillator is capable of operating down to supply voltages below $4kT/q$. The oscillator employs a "zero-threshold-voltage (zero-VT)" MOS transistor, due to its high drive capability at very low supply voltages. In order to increase the amplitude swing beyond the supply voltage and ground, we employed the Enhanced Swing Colpitts Oscillator (ESCO) [5, 9] for the oscillator topology.

The paper is organized as follows. Section II presents the operating frequency and start-up conditions for the enhanced swing Colpitts oscillator. In Section III we describe the oscillator design methodology and report the experimental results, and Section IV concludes the paper.

II. THE ENHANCED SWING COLPITTS OSCILLATOR (ESCO)

A schematic of the conventional Colpitts oscillator is given in Fig. 2. We will discuss some of its limitations for ultra-low-voltage applications before analyzing the enhanced swing Colpitts oscillator (ESCO).

When the voltage swing is large and the current source enters the triode region for a fraction of the period, the voltage drop across the current source can be close to zero. Thus, the minimum voltage at the source and also at the drain is around zero volts (ground level). Consequently, the maximum sinusoidal peak-to-peak voltage swing at the drain cannot exceed $2V_{DD}$ (supply limited region), which is an important drawback of the Colpitts oscillator in Fig. 2.

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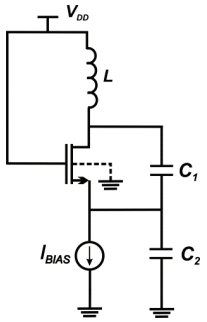

Figure 2. Conventional Colpitts oscillator.

In order to circumvent the limitations of the conventional Colpitts oscillator, one can use the ESCO [5]. This topology is capable of boosting the oscillation amplitude beyond the supply rails. In the small-signal model of the ESCO of Fig. 3, g_{ms} and g_{md} represent the source and drain transconductances [6]. The transistor capacitance C_{gs} can be absorbed into C_2. Capacitance C_p represents the sum of all capacitances between the drain node and the ac ground. G_1 and G_2 model the losses of inductors L_1 and L_2, respectively.

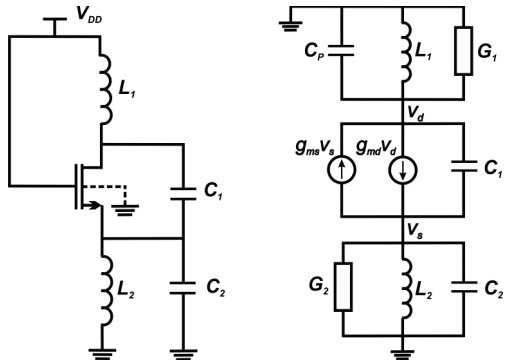

Figure 3. Schematic of the ESCO and its small-signal model.

A. Analysis of the ESCO

Assuming for the sake of simplicity that the ESCO oscillation frequency is independent of the losses and of the transistor parameters, the oscillation frequency [7] is

$$\omega^2 L_1 C_{eq} = 1 \tag{1}$$

where C_{eq}[1] is defined by

$$C_{eq} = \frac{k_L(C_1+C_2)+C_1+C_p-\sqrt{\left[k_L(C_1+C_2)-(C_1+C_p)\right]^2+4k_L C_1^2}}{2} \tag{2}$$

and $k_L=L_2/L_1$.

Neglecting C_P and the losses of the passive devices, one can write the KCL for nodes V_d and V_s, which leads to equations (3) and (4), respectively.

$$\frac{V_d}{V_s} = \frac{L_1}{L_2}\left(\omega^2 C_2 L_2 - 1\right) \tag{3}$$

[1] In fact, two solutions can be found for the equivalent capacitance; however, only the lower capacitance is a viable solution. The reason for this is that the loop gain will be negative for the lower frequency; thus, the circuit cannot oscillate at the lower frequency [7].

$$\frac{V_d}{V_s} = 1+\frac{C_2}{C_1}\left(1-\frac{1}{\omega^2 C_2 L_2}\right) \tag{4}$$

These two equations, which give the relation between the drain and source potentials in terms of the oscillation frequency ω, are shown in Fig. 4. As can be seen in the figure, for a specified L_1/L_2 ratio the curves intersect at two points. However, only the higher frequency, which results in a positive V_d/V_s ratio (see footnote), is a solution.

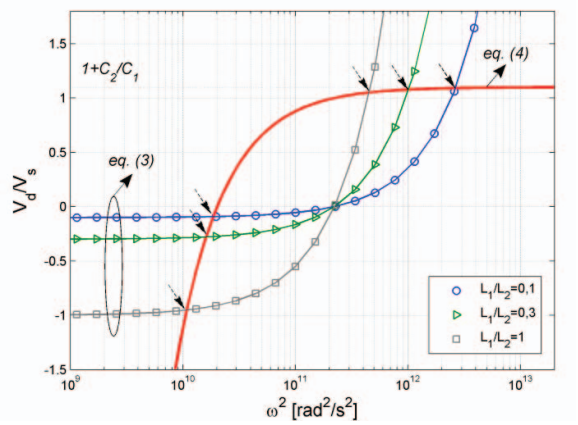

Figure 4. V_d/V_s ratio in terms of ω^2, for the cases where L_1/L_2 = 0.1, 0.3, and 1, with C_2/C_1=0.1.

The minimum gain required for the starting up of the oscillations can be calculated from the oscillator model in Fig. 5, where the relationship between the source and drain voltages [7] is

$$\frac{V_d}{V_s} = a = u+\sqrt{u^2+\frac{1}{k_L}} \tag{5}$$

and

$$u = \frac{1}{2}\left(1+\frac{C_2}{C_1}-\frac{L_1}{L_2}\right) \tag{6}$$

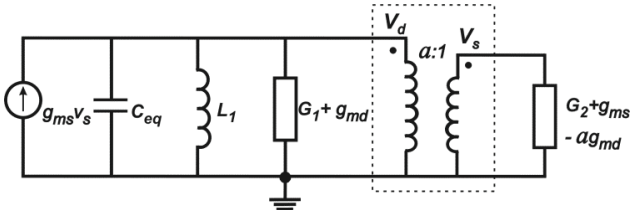

Figure 5. ESCO with capacitive divider modeled as a transformer [8].

For the starting up of oscillations at low supply voltages, we will see that the value of a chosen must be relatively close to unity, which is achieved when $C_2/C_1 \ll 1$. In this case (5) can be approximated as

$$a_{C_2 \ll C_1} = 1+\frac{C_2/C_1}{1+1/k_L} \tag{7}$$

For the occurrence of oscillation, the transistor must be able to compensate the losses of the passive components. From Fig. 5 the requirement for oscillation is written as

$$g_{ms} > a g_{md} + \frac{a^2 G_1}{(a-1)} + \frac{G_2}{(a-1)} \tag{8}$$

From (8) the minimum intrinsic gain of the transistor (g_{ms}/g_{md}) is

$$\frac{g_{ms}}{g_{md}} > a + \frac{G_1}{g_{md}} \frac{a^2}{a-1} + \frac{G_2}{g_{md}} \frac{1}{a-1} \tag{9}$$

The value a_{opt} which minimizes (9) is

$$a_{opt} = 1 + \sqrt{\frac{G_1 + G_2}{G_1 + g_{md}}} \tag{10}$$

Assuming that the quality factors of the inductors are equal, *i.e.* $G_1/G_2=L_2/L_1$, the substitution of (10) into (9) yields the optimized minimum value for the intrinsic gain

$$\frac{g_{ms}}{g_{md}} > 1 + 2\frac{G_1}{g_{md}} + 2\sqrt{\left(1+\frac{L_1}{L_2}\right)\left(1+\frac{G_1}{g_{md}}\right)\frac{G_1}{g_{md}}} \tag{11}$$

From (11) it follows that the gain required for oscillation can be reduced for high values of g_{md} and low L_1/L_2 ratios.

Using (11) and (A5) we find that the supply voltage required for oscillation is

$$\frac{V_{DD}}{\phi_t} = \frac{V_{DS}}{\phi_t} = \frac{\phi_t g_{md}}{2I_S}\left(\frac{g_{ms}}{g_{md}} - 1\right) + \ln\frac{g_{ms}}{g_{md}} \tag{12}$$

which is minimized for the optimized value of g_{ms}/g_{md} in (11).

From (7) and (10), after choosing g_{md}, L_1 and L_2, we can determine the C_1/C_2 ratio, for $G_1/G_2=L_2/L_1$, as

$$\left.\frac{C_2}{C_1}\right|_{opt} = \left(1+\frac{L_1}{L_2}\right)^{3/2}\sqrt{\frac{G_1/g_{md}}{1+G_1/g_{md}}} \tag{13}$$

III. DESIGN AND EXPERIMENTAL RESULTS

High-quality inductors (Q>10), with the inductances indicated in Fig. 6, were designed. The oscillator employs a wide zero-VT transistor (W/L=1500µm/420nm) to provide enough drive capability to compensate the inductor losses. The transistor was built as a parallel association of 300x5µm-width transistors.

It is worth noting here that the drain transconductance of the zero-VT transistor operating at low voltages with $V_G=V_D$ is almost bias-independent. To demonstrate this, consider the transistor model described in Appendix A, biased at $V_S=V_B$ and $V_G=V_D=V_{DD}$. Assuming that n=1, (A2) can be written as

$$\frac{-V_T}{\phi_t} = \left[\sqrt{1+i_r} - 2 + \ln\left(\sqrt{1+i_r} - 1\right)\right] \tag{14}$$

Thus, the reverse inversion level is, at least for low voltages, almost independent of the gate voltage. If, in addition, the value of V_T is exactly zero, the solution of (14) corresponds to i_r = 3, and the value of g_{md} calculated from (A4) is

$$g_{md} = 2I_S / \phi_t \tag{15}$$

Therefore, in a first-order approximation, the g_{md} value is dependent only on the specific current I_S, defined in Appendix A, and the thermal voltage ϕ_t. Equation (15) can be used for a back-of-the-envelope calculation of g_{md}.

Once the inductors and transistor parameters are known, the capacitive feedback can be readily determined from (13), which, in our design, yields an optimum capacitive ratio ≈ 0.7. From (1) and (2), after some adjustment to account for parasitic capacitances due to layout, the C_1 and C_2 values of 6 pF and 3.5 pF, respectively, were chosen.

A schematic diagram of the oscillator is shown in Fig. 6. The device parameters were extracted from Cadence EDA tools. A tapered inverter chain was chosen for the buffer since it presents a small capacitive load to the oscillator. The layout of the circuit implemented in the IBM 130 nm technology is shown in Fig.7

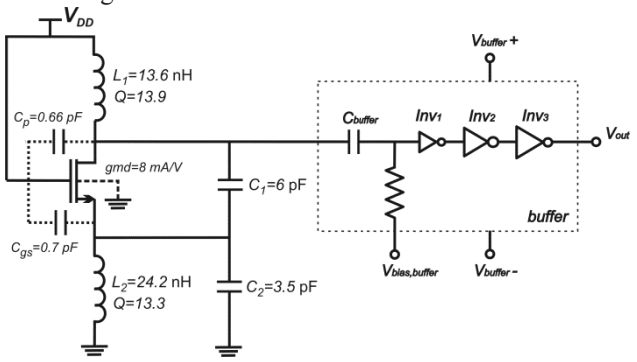

Figure 6. Schematic diagram of the ESCO design along with the voltage buffer. Inductors were simulated at 800 MHz.

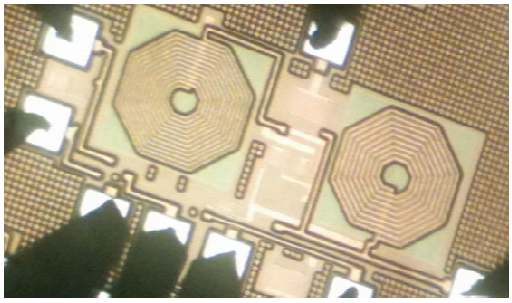

Figure 7. Micrograph of the ESCO buit in the IBM 130 nm technology.

Measurements for the prototype showed that the circuit oscillates from V_{DD}=86 mV, whereas the calculation from (11) and (12) gives a minimum supply voltage of 56 mV. The main results obtained with the fully-integrated ESCO are summarized in Table I. The calculated values were taken from the simulated parameters detailed in Fig. 6, without taking into account the parasitic elements due to the layout. The spectrum for the oscillator biased at V_{DD}=110 mV is shown in Fig. 8.

The extracted transconductances of the transistor are shown in Fig. 9. As can be seen, the transistor presents a gain of $g_{ms}/g_{md} > 2$ when operating from voltages above 50 mV. In comparison with the simulation, the experimental value of g_{md} is around two times higher. This difference can be mainly assigned to a variation in the V_T value.

Table I. Summary of the main results for the fully-integrated ESCO.

	Calculated	Simulated from layout	Experimental
Frequency	850 MHz	715 MHz	706 MHz
$V_{DD,min}$	56 mV	50 mV	86 mV

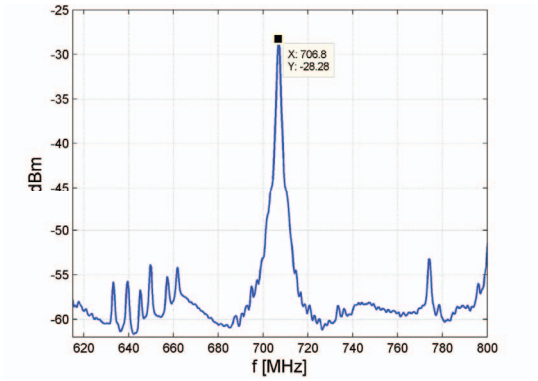

Figure 8. Spectrum for the ESCO. V_{DD} = 110 mV.

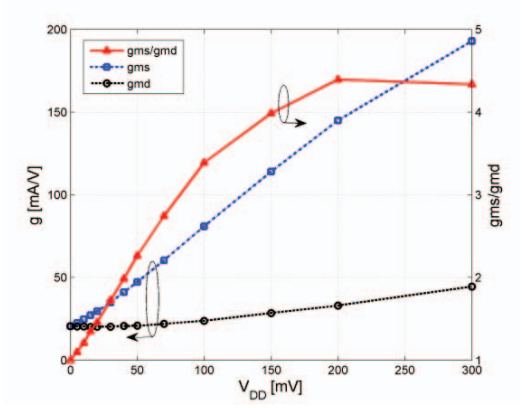

Figure 9. Experimental transconductances of the zero-VT transistor (W/L=300x5µm/0.48µm), for V_S=V_B=0 and V_G=V_D=V_{DD}.

IV. Conclusions

We have presented a fully-integrated prototype of a Colpitts oscillator in which the active component is a zero-VT MOSFET. The Colpitts oscillator considered in this study operates down to a supply voltage of 86 mV. The topology functionality was verified through experimental results in a prototype in the IBM 130 nm CMOS technology. Experimental results verified that the topology is suitable for energy harvesting applications, either a start-up oscillator, for instance, to provide a kick-up input voltage for a boost converter [4], or to deliver the input signal to a voltage multiplier to energize low-power circuits.

Appendix A - The Transistor Model

The MOSFET model used in this paper is the Unified Current Control Model (UICM) [6], which is written as

$$I_D = I_S\left(i_f - i_r\right) \tag{A1}$$

where,

$$\frac{V_P - V_{S(D)}}{\phi_t} = \ln\left(\sqrt{1+i_{f(r)}}-1\right)+\sqrt{1+i_{f(r)}}-2 \tag{A2}$$

$$V_P \cong \frac{V_{GB}-V_T}{n} \tag{A3}$$

The differentiation of the current with respect to V_S and V_D allows us to write

$$g_{ms(d)} = -\frac{\partial I_D}{\partial V_{S(D)}} = \frac{2I_S}{\phi_t}\left(\sqrt{1+i_{f(r)}}-1\right) \tag{A4}$$

V_{DS} can be expressed in terms of i_f and i_r using (A2). The resulting expression for V_{DS} can be subsequently written in terms of the transconductances making use of (A4), which yields

$$\frac{V_{DS}}{\phi_t} = \sqrt{1+i_f}-\sqrt{1+i_r}+\ln\left(\frac{\sqrt{1+i_f}-1}{\sqrt{1+i_r}-1}\right) = \frac{\phi_t}{2I_S}\left(g_{ms}-g_{md}\right)+\ln\frac{g_{ms}}{g_{md}} \tag{A5}$$

The symbols are defined as follows: I_D – drain current; I_S – specific current, i_f and i_r – forward and reverse inversion levels; V_P - pinch-off voltage; V_T – threshold voltage; g_{ms}, g_{md}, – source and drain transconductances [6].

Acknowledgments

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References

[1] R. J. M. Vullers, R. van Schijk, I. Doms, C. van Hoof, and R. Mertens, "Micropower energy harvesting," *Solid-State Electronics,* vol. 53, pp. 684-693, July 2009.

[2] N. Lotze and Y. Manoli, "A 62 mV 0.13µm CMOS standard-cell-based design technique using Schmitt-trigger logic," *IEEE J. Solid-State Circuits*, vol. 47, no. 1 pp. 47-60, Jan. 2012.

[3] Y. K. Ramadass and A. P. Chandrakasan, "A battery-less thermoelectric energy harvesting interface circuit with 35 mV startup voltage," *IEEE J. of Solid-State Circuits*, vol.46, no.1, pp. 333-341, January 2011.

[4] P.-H. Chen, X. Zhang, K. Ishida, Y. Okuma, Y. Ryu, M. Takamiya, and T. Sakurai, "An 80 mV startup dual-mode boost converter by charge-pumped pulse generator and threshold voltage tuned oscillator with hot carrier injection," *IEEE J. of Solid-State Circuits*, vol.47, no.11, pp. 2554-2562, Nov. 2012.

[5] T. W. Brown, F. Farhabakhshian, A. G. Roy, T. S. Fiez, and K. Mayaram, "A 475 mV, 4.9 GHz enhanced swing differential Colpitts VCO with phase noise of -136 dBc/Hz at a 3 MHz offset frequency," *IEEE J. Solid-State Circuits*, vol. 46, no. 8 pp. 1782-1795, Aug. 2011

[6] M. C. Schneider and C. Galup-Montoro. *CMOS Analog Design Using All-Region MOSFET Modeling*, Cambridge University Press, 2010.

[7] M. B. Machado, M. C. Schneider, and C. Galup-Montoro "On the minimum supply voltage for MOSFET Oscillators," accepted to *IEEE Trans. on Circuits and Systems I: Regular Papers*, Aug. 2013.

[8] K. K. Clarke and D. T. Hess, *Communication Circuits: Analysis and Design, Krieger Publishing Company*, Malabar, FL, 1971.

[9] F. R. De Sousa, M. B. Machado, and C. Galup-Montoro, "A 20 mV Colpitts oscillator powered by a thermoelectric generator," in Proc. IEEE Int. Symp. on Circ. and Systems, pp. 2035-2038, Seoul, Korea, May 2012.