A Setup for Automatic MOSFET Mismatch Characterization under a Wide Bias Range

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ABSTRACT

This paper describes a test setup for automatic characterization of MOS transistors mismatch. It is composed by a custom made test chip, a computer and measurement equipment. The chip aggregates analog switches, a programmable shift register and a reference circuit, as well as the matrix of 1296 transistors to be tested. It was already successfully integrated in 0.35 μm and 0.18 μm bulk technologies, and was designed to give experimental support for our MOSFET mismatch model. This setup brings to low-budget research laboratories, the facility of a completely autonomous dc characterization, over a wide range of operation conditions, from weak to strong inversion and from linear to saturation region, allowing statistical analysis of MOSFET process and devices.

Keywords: MOSFET, analog design, matching, mismatch, characterization, test structure

1 INTRODUCTION

Mismatch is the denomination of time-independent variations between identically designed components [1]. The performance of most analog or even digital circuits relies on the concept of matched behavior between identically designed devices. In analog circuits, the spread in the dc characteristics of supposedly matched transistors results in inaccurate or even anomalous circuit behavior. Also, for digital circuits, transistor mismatch leads to propagation delays whose spread can be of the order of several gate delays for deep-submicron technologies [2]. The shrinkage of the MOSFET dimensions and the decreasing in the supply voltage make matching limitations even more important in today advanced processes [3].

The stochastic nature of local mismatch of MOS transistors makes its electrical characterization a complex, time consuming task. A large number of samples, having different geometries, must be measured under a wide range of bias conditions, as a way to characterize device behavior and extract statistical model parameters.

Traditional design of test structures for mismatch characterization is based on grouping the transistors in an n-dimensional matrix, as a way to share the limited number of output pads. So, similar transistors are joined in common-drain (or source, or gate, or even bulk) arrays, and individually measured by selective bias applied to a specific combination of pads [4]. Pad selection can be hand-made, rendering the measurement results very susceptible to human mistakes, or can be done by high-cost servo-controlled microprobes or even by huge automated switching test equipment.

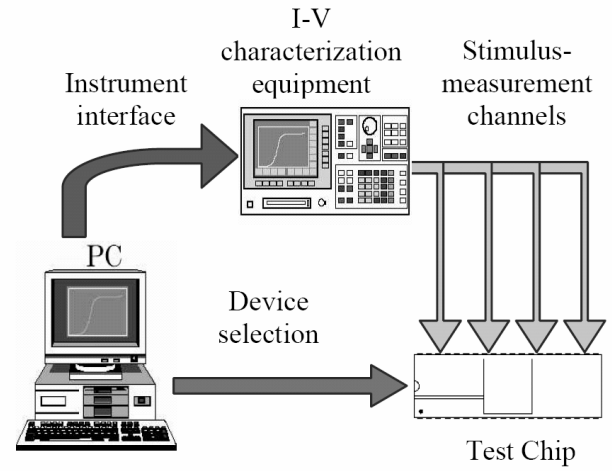

Figure 1: Dc characterization setup, composed by a test chip, a computer and measurement equipment.

In this paper we describe a test chip that contains 648 pairs of transistors for dc mismatch characterization, where the device selection strategy was included inside the chip, through the use of analog CMOS switches and a programmable register. These features, besides custom software running in a PC microcomputer, and an *Agilent 4156 Semiconductor Parameter Analyzer* (Fig. 1), result in a fully automated mismatch characterization setup proper for academic laboratories.

2 TEST CIRCUIT

MOSFET mismatch is characterized through the measurement of the dc voltage-current behavior of an array of identically designed test transistors. The accuracy and completeness of this process depend on several factors, like the *number of measured devices*, the *number of device arrays*, their *geometry* and *spatial organization*, the way the test devices are *externally accessed*, and the *bias* and *measurement strategies*.

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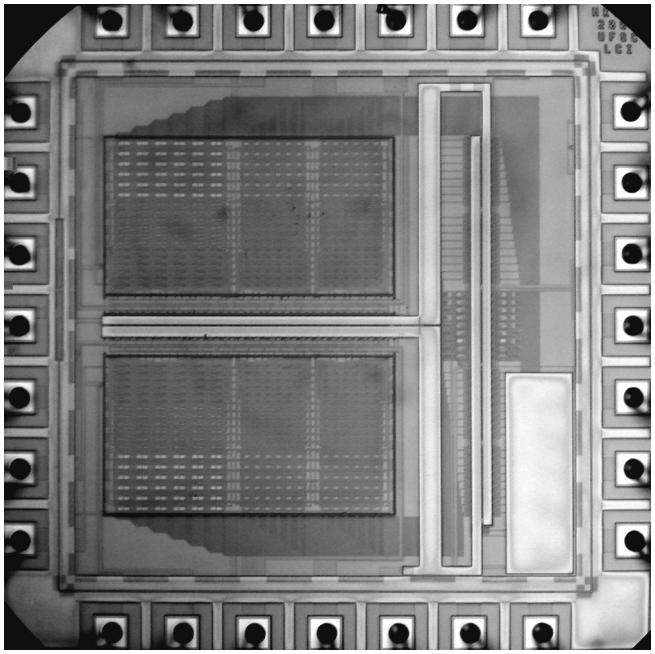

Figure 2: Microphotograph of the test chip (fabricated in the *TSMC 0.35 μm* process, on a 28-pad 1.5 mm square chip). The two rectangular large areas are the NMOS (down) and the PMOS (up) transistor arrays. Between them is part of the serial register (36 bits) and the drain selection switches. On the right side of the die are the last 45 bits of the serial register, and the reference transistors for biasing.

Our test chip was designed having the *TSMC 0.35 μm* (3.3 V n-well CMOS) as the target process (Fig. 2), since this technology is widely used for analog and mixed-signal prototyping. A second version, adapted to the TSMC 0.18 μm (1.8 V double-well p-substrate CMOS) was also fabricated.

Since we need to characterize geometric effects, like short and narrow-channel, edge, and other second order effects, we decided to design a rectangular matrix containing 9 arrays with 3 scaled ratios for transistor length (*L*) and width (*W*), disposed in order to optimize area consumption. Each dimension (*L* and *W*) was scaled as 1, 4 and 16 multiples of the minimum *L* and *W*, respectively (which are $L_{min} = 2\lambda$ and $W_{min} = 3\lambda$, being $\lambda = 250$ nm for the 0.35 standard rules and $\lambda = 100$ nm for the 0.18 submicron rules).

Differential pooling [5] was chosen, since it can highlight local mismatch causes more properly than complete pooling. So, each array was designed as a 6x6 matrix of pairs of transistors, resulting in 72 transistors per array, or 648 test transistors of each type (N and PMOS).

External access to drain terminals is multiplexed using 9 groups of 4 switches, each group being responsible for the connection of a specific array. To minimize the effects of the mismatch between the equipment channels (instrumental errors), the drains of the left and right transistors of each pair can be connected alternately to A or B measurement channels (Fig. 3). Each measurement on a transistor of the pair is the average of the two channel measurements.

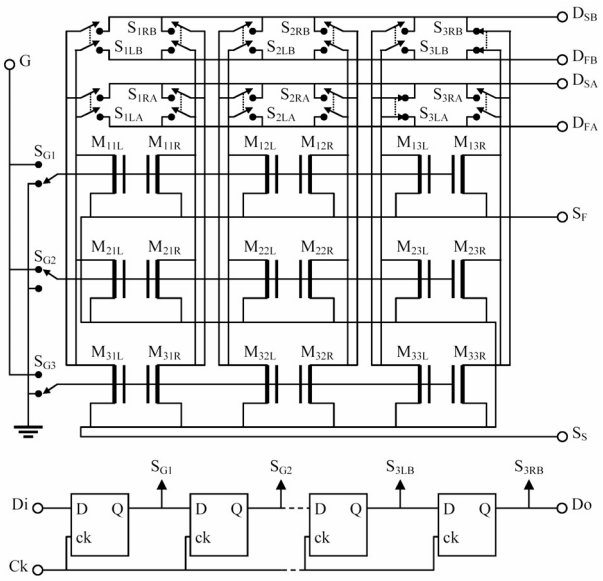

Figure 3: Simplified schematic diagram of the transistor matrix. It shows a 3x3 matrix for differential pooling, with the drain and gate selection switches and the serial register. The reference bias circuit is not shown. Common source connection also provides force-sense access.

A specific pair of an array can be selected by the activation of one switch, among 36, that connects its gates to the bias reference path (G). The other 35 deactivated switches keep the unselected pairs in the *off* condition. Since the arrays have different geometries, 9 reference transistors are needed for bias, being the respective one selected by multiplexing switches. An 81-bit serial register was needed for controlling the switches.

Figure 3 shows a simplified schematic of the matrix, composed by 3 arrays (columns), each one containing 3 identical pairs. The third column array is connected to the A and B *force* and *sense* drain pads (D_{FA}, D_{SA}, D_{FB}, and D_{SB}) by the S_{3LA} and S_{3RB} pairs of switches. Force and sense terminals were employed to avoid the influence, at higher currents, of the voltage drops along the signal path to the device under test. Also the pads connection of the common source (S_F and S_S) of all transistors uses the force-sense scheme. The second pair of the connected array is selected by the gate switch (S_{G2}), while the remaining transistors are kept unselected. The bias reference transistors and their selection switches are not shown.

The complete circuit, containing 9 arrays, selection switches, bias references and output pads, must be doubled for N and PMOS characterization, but the same serial register can be used for both matrixes.

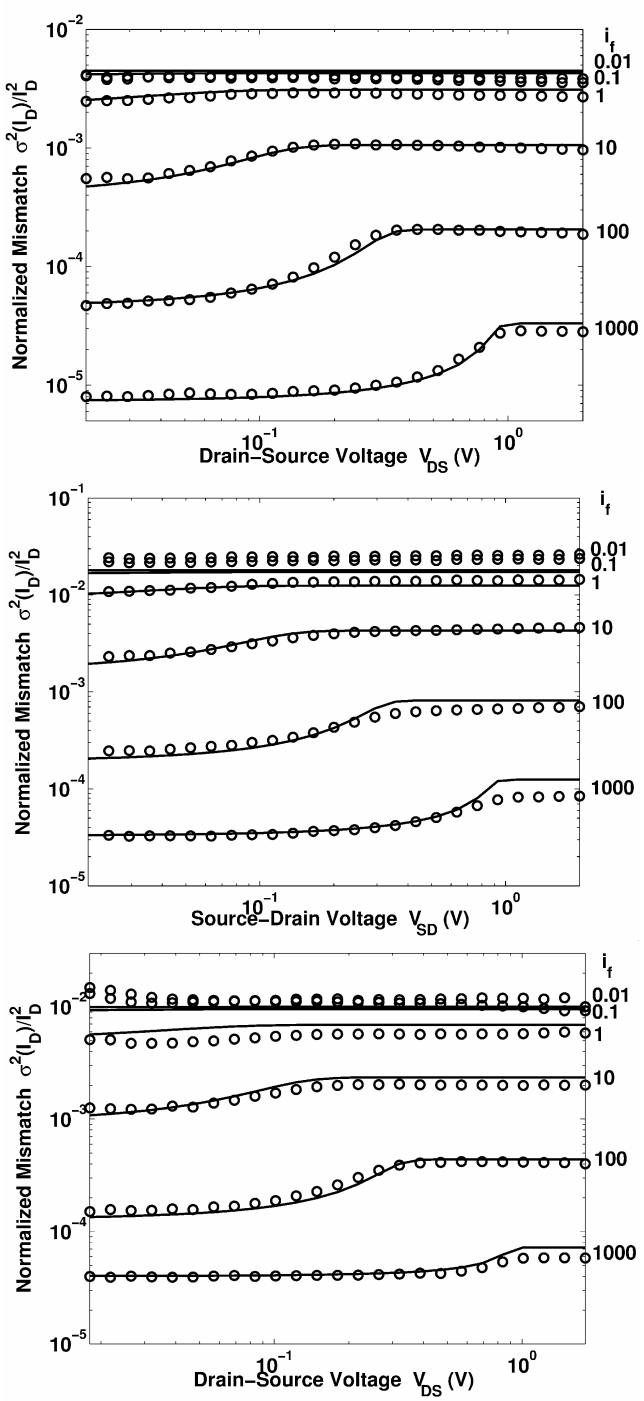

Figure 4: Normalized mismatch from linear (20mV) to saturation (2V) region, under a wide range of inversion levels (i_f: from 0.01 to 1000). Measurements (circles) are from 3µm/2µm *TSMC 0.35* NMOS (up) and PMOS (middle) devices, and from 1.2µm/0.8µm *TSMC 0.18* NMOS (down). Solid lines represent eq. (1).

Guard rings were included around the transistor arrays, references, switches and the serial register, to reduce dc coupling through the bulk. Wide metal connections and multiple contact windows were employed in the critical paths of the layout to lower ohmic drops. The layout was done employing matching techniques to reduce undesirable global mismatch.

The test setup also includes an IBM-PC compatible computer, running the characterization software that was developed for this application. This software is responsible for the stimulus-measurement sequential stepping, controlling the *Agilent 4156* by its GPIB interface, programming the test chip serial stream, and for data storing of the results. The serial register is controlled by 3 pins of the parallel interface of the computer. An optically-isolated interface was also developed to avoid noise injection from the computer to the test chip and to adapt the level of the interface signals. The data out signal (D_O) that comes from the register is used to check the correctness of the programming data.

3 MISMATCH COMPACT MODEL

Many MOSFET mismatch models have been proposed in the last 20 years. The most popular of them is known as the Pelgrom's model [1], was proposed in 1989 and became an industry standard. Unfortunately this model does not consider the nonlinear nature of MOSFETs in a proper manner [6], yielding to inconsistent formulas [7]. This inconsistency has being highlighted by the shrinking dimensions and reduced supply voltage of current submicron technologies, where transistors are designed to work from very weak to very strong inversion condition.

Recently we developed a new mismatch model, based on the integration of the contribution of the local dopant fluctuation along the MOSFET channel [4], keeping in mind its nonlinearities through the use of the Advanced Compact MOSFET (ACM) model [8]. Doping concentration fluctuation that derives from the discrete nature of charges is widely recognized as the main mismatch cause for today's advanced technologies [9]. This model will not be described here since its detailed derivation is available in recent publications [3], [4].

The main result from our model is a compact formula for current mismatch evaluation, which predicts mismatch from geometry (W and L), bias (i_f and i_r) and technology (N_{oi} , B_{ISQ} and N^*)

$$\frac{\sigma^2_{I_D}}{I_D^2} = \frac{1}{WL}\left[\frac{N_{oi}}{N^{*2}}\frac{1}{i_f - i_r}\ln\left(\frac{1+i_f}{1+i_r}\right) + B^2_{I_{SQ}}\right] \qquad (1)$$

where i_f and i_r are the forward and reverse inversion levels, and $N^* = -Q'_{IP} / q = nC'_{ox}\phi_t / q$ is the channel charge number density at pinch-off. N_{oi} is the main mismatch model parameter, representing the effective number of impurities per unit area in the channel depletion volume. B_{ISQ} is a less significant model parameter that accounts for variations in the specific current ($I_{SQ} = \frac{1}{2}\mu C'_{ox} n\phi_t^2$).

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4 EXPERIMENTAL RESULTS

The versatility of the test chip, with individual software-controlled access to gate and drain terminals, allows a wide variety of MOSFET statistical voltage-current characterization, including the measurement of threshold voltage (V_T), slope factor (n), specific current (I_S), as well as mismatch.

Average specific current (I_S) was measured from the *TSMC 0.35 large*, *medium* and *small* arrays (W/L = 12μm/8μm, 3μm/2μm and 0.75μm/0.5μm, respectively), resulting: I_{S_large}= 132 nA, I_{S_medium}= 129 nA, and I_{S_small}= 149 nA. Using some mathematical processing over the I_S measurements, a first approximation of the channel length and width shifts can be calculated, resulting ΔL= 0.09 μm and ΔW= 0.08 μm ($L_{eff} = L - \Delta L$, $W_{eff} = W - \Delta W$) [10]. I_S from the *TSMC 0.18 large*, *medium* and *small* arrays (W/L = 4.8μm/3.2μm, 1.2μm/0.8μm and 0.3μm/0.2μm), resulted: I_{S_large}= 229 nA, I_{S_medium}= 213 nA, and I_{S_small}= 311 nA.

Figure 4 shows the mismatch measurement from the *medium* N and P arrays of one *TSMC 0.35* chip, for drain to source voltage ranging from 20 mV (linear region) to 2V (saturation). Mismatch was measured for six different inversion levels (0.01, 0.1, 1, 10, 100 and 1000), covering the very weak to very strong inversion range. Solid lines were determined from our model using (1). Model parameters were calculated from *medium* and *large* size arrays, resulting in N_{oi} = 1.9x10^{12} cm^{-2} and B_{ISQ}= 0.69 %-μm for the NMOS, and N_{oi} = 6.6x10^{12} cm^{-2} and B_{ISQ}= 0.77 %-μm for the PMOS. Mismatch measurement from the *TSMC 0.18* process is also shown.

Systemic errors of the measurement setup, like leakage currents for example, were evaluated executing complete characterizations of some chips, but keeping all the drain switches in the *off* state. Experimental results showed that the *off* currents impact less than 1% of the mismatch measurement for currents above 10 nA.

MOSFETs mismatch was measured for N and PMOS arrays of 10 out of 40 encapsulated dies (DIP 28 package), all of them showing similar statistical behavior. Complete automatic measurement of the 9 N or PMOS arrays of one chip, in 6 different inversion levels, from linear to saturation condition, spends around 12 hours and generates 243,000 values. This excessive time spending results from the *Agilent 4156* slow measurements of small currents, below 100 nA. Also, to increase accuracy, the *Agilent 4156* is programmed to perform an average measurement over 16 samples.

5 CONCLUSIONS

A mismatch test circuit that enables the characterization of a high number of closely located MOSFETs without the need for high-cost equipment has been presented. A force-sense technique provides accurate stimulus and measurement in all device terminals. Differential pooling was also used for emphasizing local over global mismatch. Nine test device arrays were implemented in N and PMOS for the identification of geometric effects and complete technological characterization. Besides mismatch, chip versatility allows a wide range of device measurements and parameter extraction. Technological, geometric and mismatch parameters and curves were presented for the *TSMC 0.35μm* and *TSMC 0.18μm* processes.

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