# All-Region MOS Model of Mismatch due to Random Dopant Placement

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## ABSTRACT

This paper presents a study of drain current matching in MOS transistors. A new model for MOS transistor mismatch is summarized, using the carrier number fluctuation theory to account for the effects of local doping fluctuations. CMOS test structures were designed and fabricated to allow an extensive experimental work, where current mismatch was measured under a wide range of bias conditions. The model shows good fitting with measurements over a wide range of operation conditions, from weak to strong inversion, from linear to saturation region, and allows the assessment of mismatch from process and geometric parameters.

***Keywords***: mosfet, analog design, matching, mismatch, compact models

## 1 INTRODUCTION

Integrated circuit design strongly depends on the concept of similarity of identically designed electronic devices [1]-[3]. Progressive shrinkage of MOSFET dimensions and reduction of supply voltage has increased mismatch effects, which, in turn, impacts yield to such an extent that several new studies about transistor mismatch have been published in recent years [4]-[6]. Although a great progress have been done in mismatch understanding, existing models have some limitations, being restricted to some operation region or needing complex parameter sets.

## 2 MISMATCH MODELING

Existing mismatch models use either simple drain current models limited to a specific operating region [1], [2], [5], or complex expressions [4] like that of BSIM. In general, however, it is widely accepted that matching can be modeled by the random variations in geometric, process and/or device parameters, and the effect of these parameters on the drain current can be quantified using the dc model of the transistor. As pointed out in [5] and [6], there is a fundamental flaw in the current use of dc models for mismatch analysis that results in inconsistent formulas. Mismatch models implicitly assume that the actual values of the lumped model parameters ($V_T$, $\beta$, etc) can be obtained by integration of the position-dependent distributed parameters over the area of the channel region of the device. As analyzed in [5], the application of this concept to series association of transistors leads to an inconsistent result owing to the nonlinear nature of MOSFETs.

A better approach for mismatch modeling results when microscopic sources of mismatch are computed along the MOSFET channel. In this way the MOS transistor is split into 3 series elements (an upper transistor, a lower transistor, and a small channel element of length $\Delta x$ and area $\Delta A = W\Delta x$, where $W$ is the channel width). Small-signal analysis allows one to calculate the effect of the local current fluctuation of the small channel element ($i_{\Delta A}$) on the total drain current deviation ($\Delta I_d$) [7]. Considering local current fluctuations along the channel as uncorrelated, the square of the total drain current fluctuation is given by

$$\overline{\Delta I_D{}^2} = \sum(\Delta I_d)^2 = \lim_{\Delta x \to 0} \sum \left( \frac{\Delta x}{L} i_{\Delta A} \right)^2 = \frac{1}{L^2} \int_0^L \Delta x \left( i_{\Delta A} \right)^2 dx \qquad (1)$$

where $L$ is the channel length and $x$ is the distance from the channel element to the transistor source.

To obtain general results for all bias regions of the transistor we have used the Advanced Compact MOSFET (*ACM*) model, a physics-based one-equation all-regions model [8]. With the help of ACM model, the local current fluctuation ($i_{\Delta A}$) can be related to the inversion charge density fluctuation ($\Delta Q'_I$) along the channel, which, in turn, is related to the fluctuation in the concentration of ionized impurities ($\Delta Q'_{IMP}$) under the gate. Integrating (1) from drain to source, a compact expression for current mismatch can be derived [7]

$$\frac{\sigma^2_{I_D}}{I_D^2} = \frac{q^2 N_{oi} \mu}{L^2 n C'_{ox} I_D} \ln \left( \frac{n C'_{ox} \phi_t - Q'_{IS}}{n C'_{ox} \phi_t - Q'_{ID}} \right) \qquad (2)$$

where $q$ is the electron charge, $n$ is the slope factor, $C'_{ox}$ is the oxide capacitance per unit area, $\mu$ is the effective mobility, $\phi_t$ is the thermal voltage, $Q'_{IS}$ and $Q'_{ID}$ are the inversion charge densities at the source and drain ends of the channel, respectively, and $N_{oi}$ represents the average number of impurities per unit area, in the depletion region, which is the only parameter needed for our mismatch model, in addition to dc parameters.

In the ACM model [8], the drain current ($I_D$) is expressed as the difference between the forward ($I_F$) and reverse ($I_R$) components, $I_D = I_F - I_R = I_S (i_f - i_r)$, where

$I_S = ½\mu C'_{ox} n\phi_t^2 (W/L)$ is the specific current and $i_f$ and $i_r$ are the forward and reverse inversion levels. Using the relationship between inversion charge density and current [8], expression (2) can be rewritten as

$$\frac{\sigma^2_{I_D}}{I_D^2} = \frac{N_{oi}}{WLN^{*2}} \frac{1}{i_f - i_r} \ln\left(\frac{1+i_f}{1+i_r}\right) \qquad (3)$$

where $N^* = -Q'_{IP} / q = nC'_{ox}\varphi_t / q$, being $Q'_{IP}$ the channel charge density at pinch-off.

Expression (3) can be simplified under specific conditions as shown in Table 1. A complete description of this mismatch model can be found in [7].

| $\sigma^2_{I_D} / I_D^2$ | weak inversion ($i_f << 1$) | strong inversion ($i_f >> 1$) |
|---|---|---|
| linear ($i_f \cong i_r$) | $\frac{N_{oi}}{WLN^{*2}}$ | $\frac{N_{oi}}{WLN^{*2}} \frac{1}{1+i_f}$ |
| saturation ($i_r \to 0$) | | $\frac{N_{oi}}{WLN^{*2}} \frac{\ln(1+i_f)}{i_f}$ |

Table 1: Expression (3) simplified under specific conditions.

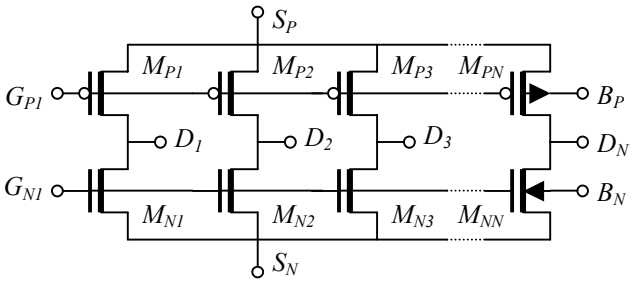


Figure 1: Schematic diagram of an array of PMOS and NMOS transistors with the same dimensions.

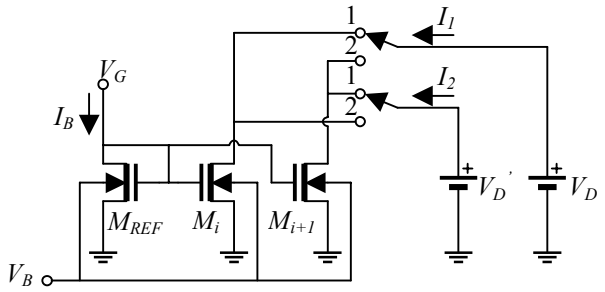


Figure 2: $M_{REF}$ is the reference transistor while $M_i$ and $M_{i+1}$ are the transistors under test. $I_B$ ($V_B$, $V_D'=V_D$) is a current (voltage) source. $I_1$ and $I_2$ are the measured currents.

# 3 MEASUREMENTS

A mismatch test circuit was designed and fabricated in the TSMC 0.35μm 3.3V CMOS n-well process, through the MOSIS Education Program (MEP). It is composed of a set of NMOS and PMOS transistors disposed in arrays of 20 identical functional devices, surrounded by dummy ones to ensure uniform boundary conditions for all active transistors. Transistor dimensions (*WxL*) of each array are 12μm x 8μm (*large*), 3μm x 2μm (*medium*), 0.75μm x 8μm (*narrow* - minimum width), 12μm x 0.5μm (*short* - minimum length) and 0.75μm x 0.5μm (*small* - minimum size). Figure 1 shows a schematic diagram of an array of our test circuit (NMOS and PMOS transistors shown).

Intradie current mismatch was measured from ten packaged dies out of forty, all of them presenting the same mismatch behavior. The circuit shown in Figure 2 was used for measuring current mismatch. The same $M_{REF}$ was used for all measurements while the remaining 19 transistors were measured in pairs of adjacent devices, $M_i$ and $M_{i+1}$ ($i=1, \ldots, 18$), for data acquisition. Transistor pairs $M_i$ and $M_{i+1}$ were sequentially characterized, with the currents of both transistors ($I_1$ and $I_2$) being measured simultaneously for each bias condition with the switches in either position 1 or 2. The dc current flowing in each device, $I_{D(i)}$ or $I_{D(i+1)}$, was taken as the average value of the two currents measured for each transistor. This procedure minimizes first order errors that may result from mismatch between the measurement channels.

Figure 3 presents the mismatch power normalized to the dc power ($SD^2(I_D)/I_D^2$) for drain-to-source voltage ranging from +(-)10mV (linear region) to +(-)2V (saturation) for the NMOS (PMOS) devices. Mismatch was measured for six different inversion levels (0.01, 0.1, 1, 10, 100, and 1000), for the *large*–device arrays. Simulated curves were determined from expression (3), with $i_r$ calculated through the long-channel ACM model [8]. Similar curves were measured for the *medium*–device arrays (not shown).

In weak inversion ($i_f$ = 0.01 and 0.1), mismatch is almost constant from the linear to saturation regions and independent of the inversion level, as predicted by (3). From moderate ($i_f$ = 1 and 10) to strong ($i_f$ = 100 and 1000) inversion, both the simulated and measured curves present similar behavior, increasing from the linear region to saturation, where a plateau is reached. Differences between measured and simulated curves at saturation, may be associated with spatial-nonuniformity concentration of dopant atoms [9].

Parameter $N_{oi}$ was estimated from measurements in weak inversion, using equation (3). $N^*$ was calculated based on parameters provided by MOSIS. The same value of $N_{oi}$, $1.8 \times 10^{12}$ cm$^{-2}$, for the NMOS devices, and $7 \times 10^{12}$ cm$^{-2}$ for the PMOS devices was obtained for both the *large* and *medium* transistors. Some authors [4] suggest that PMOS devices show better matching than NMOS devices, or vice-versa [3]. Our results, however, indicate that matching depends on process details, such as doping

patterns (halo implant, twin-well, surface implant adjustment, retrograde implant, etc). We conclude that there is not a simple "rule of thumb" regarding which type of MOS transistor is better matched.

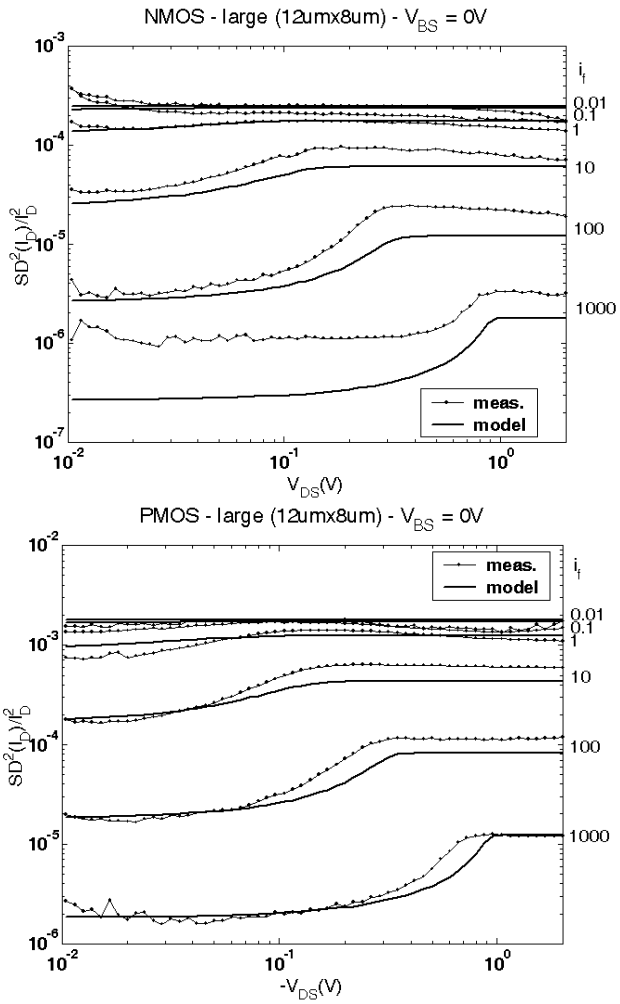


Figure 3: Normalized current mismatch for the NMOS and PMOS *large* (12µm x 8µm) transistor. Inversion level ($i_f$) ranges from 0.01 to 1000.

Figure 4 shows the measured and simulated dependence of current matching on inversion level for the linear and saturation regions of NMOS transistors, at two bulk bias voltages ($V_{BS}$). From these figures, one can see that larger transistors follow the "area rule", as shown in our model. For a particular bulk bias, we used the same $N_{oi}$ for modeling the matching of both the *large* and *medium* transistors, in the linear and saturation regions. The *small* transistors do not follow this rule, presenting a mismatch 55% lower than the model estimates (at zero volt bulk bias) using the same $N_{oi}$. Values of $N_{oi}$ for the *small* transistors different from those measured for the *large* transistors were chosen in order to obtain better fitting of the curves. Similar curves for the PMOS arrays were measured (not shown).

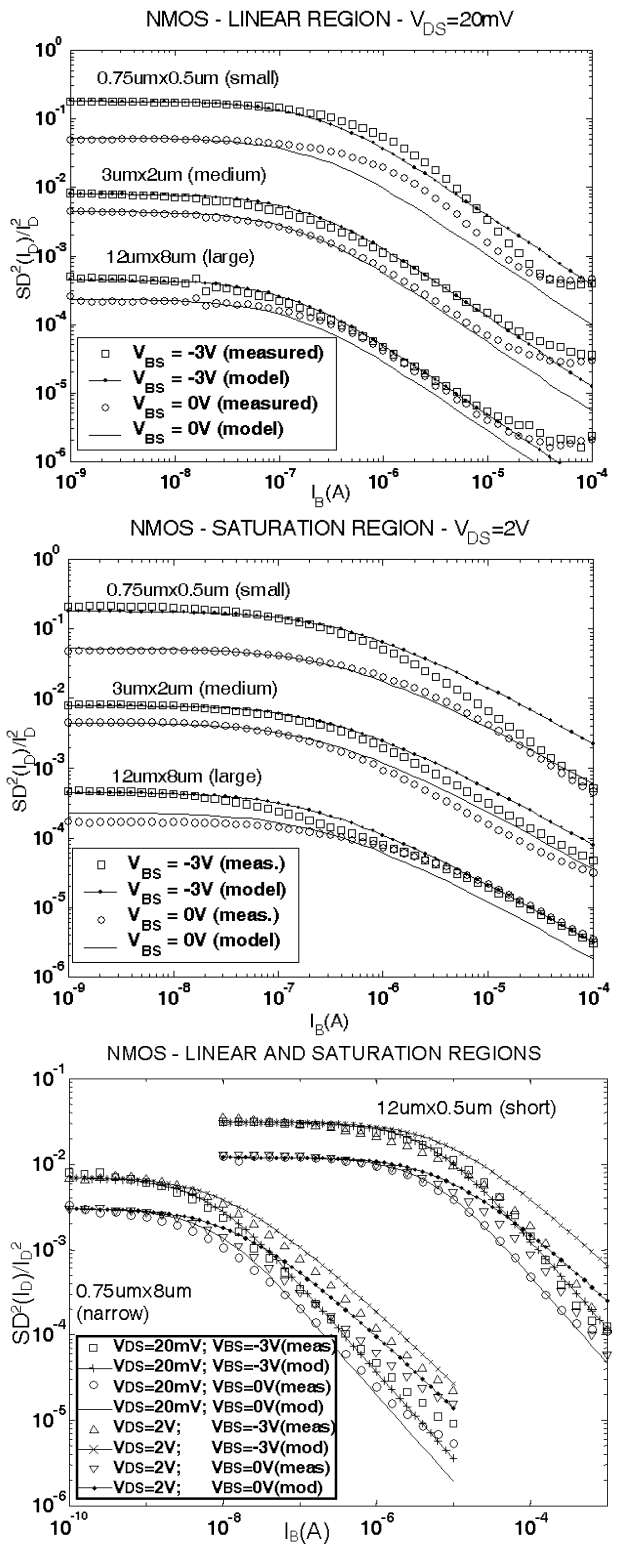


Figure 4: Current matching vs. inversion level for linear and saturation regions for the NMOS *large*, *medium*, *small*, *short* and *narrow* transistor arrays under two bulk bias voltages.

For the dies we characterized, *small* transistors presented an unpredictable $N_{oi}$, as previously observed in reference [10]. This high sensitivity of short-channel devices is one of the main reasons for the difficulties found in modeling mismatch, mainly in today's very complex submicron technologies. Also in the case of minimum length (*short*) and minimum width (*narrow*) transistors, our mismatch model is applicable to both devices showing good agreement with measured data.

Besides fluctuation of dopant atoms in the channel, gate dopant fluctuation and geometrical variations are also relevant mismatch factors [2], [11]. Many authors have shown from experiments that the first factor is the dominant factor for threshold voltage ($V_T$) mismatch (resulting in current mismatch), the second is very relevant for sub-micron processes, and the third being the least relevant in general. Gate dopant fluctuation results from the inherent poly-silicon clustering process, and doping implant concentration; therefore, it changes along the oxide interface. As a result, the gate depletion layer is not uniform over the gate area, affecting transistor behavior as if oxide thickness were not uniform (changing the charge density locally). As can be seen, other sources of mismatch can be included in our model to improve its accuracy but, for the moment, we have tried to keep it as simple as possible.

# 4 CONCLUSIONS

In this paper, we characterized current mismatch for the MOS transistor operating under a wide range of bias conditions. A set of arrays of identical transistors was manufactured in a 0.35 μm CMOS technology from TSMC to assess the influence of bias and geometry on current mismatch. Careful measurements were carried out obtain meaningful mismatch data. A previously developed mismatch model, continuous in all operating regions was used for comparison. The approach that was used for mismatch modeling is based on the integration of the random number of carriers along the channel, resulting in a compact easy-to-use formula for mismatch that covers all operating regions. The results we obtained for mismatch are closely related to those derived in [12] for *1/f* noise, since the physical mechanisms at the origin of both phenomena are similar. We conclude that fluctuations in lumped parameters such as the threshold voltage are not appropriate for describing mismatch owing to the nonlinear distribution of carriers along the transistor channel. Experimental results confirmed the accuracy of our model under a wide range of geometries and bias conditions, including different bulk bias voltages. For the technology under analysis, we concluded that the dominant factor in mismatch characterization is $N_{oi}$, the average number of dopants per unit area in the depletion layer below the channel. We expect this work will help circuit designers to predict transistor mismatch accurately from a single parameter ($N_{oi}$).

# 5 ACKNOWLEDGMENTS

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