0.7 V Supply Self-Biased NanoWatt MOS-Only Threshold Voltage Monitor

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***Abstract*—This work presents a self-biased MOSFET threshold voltage V_{T0} monitor. The threshold condition is defined based on a current-voltage relationship derived from a continuous physical model. The model is valid for any operating condition, from weak to strong inversion, and under triode or saturation regimes. The circuit consists in balancing two self-cascode cells operating at different inversion levels, where one of the transistors that compose these cells is biased at the threshold condition. The circuit is MOSFET-only (can be implemented in any standard digital process), and it operates with a power supply of less than 1 V, consuming tenths of nW. We propose a process independent design methodology, evaluating different trade-offs of accuracy, area and power consumption. Schematic simulation results, including Monte Carlo variability analysis, support the V_{T0} monitoring behavior of the circuit with good accuracy on a 180 nm process.**

I. Introduction

The threshold voltage (V_{T0}) of an MOS transistor is one of the most fundamental parameters used in all areas of circuit design and test. The measured V_{T0} value can be used for process characterization, monitoring and compensation, temperature measurements, bias circuits and voltage references. Many methods have been proposed to measure the threshold voltage value [1], varying widely with the used MOSFET model, the physical meaning of 'threshold' and with the choice of operation region of the device.

A threshold voltage monitor is a circuit that, ideally, delivers the estimated V_{T0} value as a voltage directly from its operational conditions, without external biases, parametric setups, curve fitting and/or any subsequent calculations. Through the years, many circuits have been proposed for this purpose [2], [3], [4], [5] and [6], but all of these are based on the strong inversion quadratic model for the drain current. The work of [7] uses a continuous transistor model [8] and proposes a circuit based on the channel conductance-to-current ratio (g_{ch}/i_d) methodology. Still, it requires a good estimation of the specific current of the fabrication process to correctly bias the transistor. The circuit presented in [9] is based on the same transistor model, and uses one self-cascode cell to balance two MOSFETs that have a common gate connection, but operate at different inversion levels. The circuit presented poor supply regulation because the topology did not allow a greater difference of inversion levels for the common-gate transistors. However, we do not state that these solutions are not good. The circuits are based on different definitions of threshold, making it difficult to fairly compare their performances.

In this paper we present a different self-biased topology, now based on the equilibrium of two self-cascode cells, that can be made to operate at a much higher difference of inversion levels. This makes its operating point more robust than the circuit of [9], which also translates into lower supply sensitivity. For example, the monitored threshold voltage can be used to compensate for variations in a nanoWatt sub-bandgap reference design presented in [10], where the mean variation of the reference voltage is heavily dependent on the MOSFET threshold. It can also be used as the complementary to absolute temperature (CTAT) term in voltage reference designs [11].

The text is organized as follows: section II presents the necessary equations for the MOSFET model, while section III presents the threshold voltage monitor. A design methodology is proposed in section IV, followed by simulation results in section V and the conclusion.

II. MOSFET Model

In the MOSFET model described in [8], the drain current I_D of a long-channel device is expressed as

$$I_D = I_F - I_R = SI_{SQ}(i_f - i_r) \tag{1}$$

where I_F and I_R are the forward and reverse currents, $S = W/L$ is the aspect ratio, W being the width and L the length of the transistor. i_f and i_r are the forward and reverse inversion coefficients, related to the source and drain inversion charge densities, while I_{SQ} is the sheet normalization transistor current $I_{SQ} = \frac{1}{2}n\mu C'_{ox}\phi_t^2$, where n is the subthreshold slope factor, μ is the channel effective mobility (both slightly dependent on the gate voltage V_G), C'_{ox} is the gate capacitance per unit area, and ϕ_t is the thermal voltage. The relationship between inversion levels i_f and i_r and terminal voltages is given by

$$\frac{V_P - V_{S(D)}}{\phi_t} = F(i_{f(r)}) = \sqrt{1+i_{f(r)}} - 2 + \ln\left(\sqrt{1+i_{f(r)}} - 1\right) \tag{2}$$

where V_S and V_D are the source and drain voltages (all terminal voltages are referenced to the transistor bulk), and V_P is the pinch-off voltage, approximated by

$$V_P \simeq \frac{V_G - V_{T0}}{n} \tag{3}$$

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being V_{T0} is the threshold voltage for zero bulk bias. In the used MOSFET model, the threshold voltage has a universal physical meaning, defined as the condition where the drift (square root term) and diffusion (ln term) components of the drain current on (2) have equal magnitude. In the forward saturation condition, $I_F \gg I_R$, and consequently, $I_D \simeq I_F = SI_{SQ}i_f$.

III. Circuit Description

The proposed threshold voltage monitor circuit, shown in Figure 1, is based on a self-biased current source topology presented in [12]. The circuit's DC operating point is defined by the equilibrium between two proportional to absolute temperature (PTAT) voltages generated by self-cascode (SC) cells. One of the SC cells operates in moderate inversion ($M_{1,2}$), while the other SC cell operates in weak inversion ($M_{3,4}$). Transistors M_5-M_{10} act as a voltage-following current mirror [13], making all the currents equal to I_X and $V_{X,12} = V_{X,34}$.

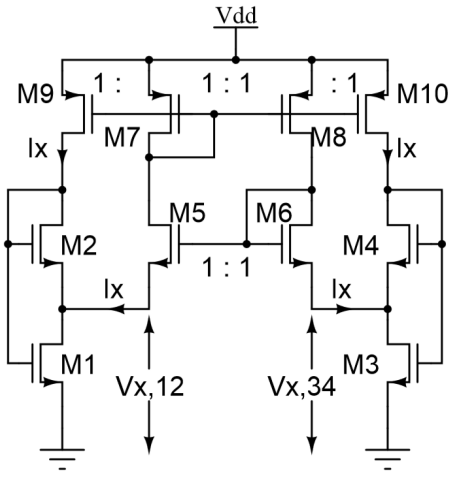

Fig. 1. Self-biased threshold voltage monitor circuit.

In [14], the voltage at the intermediate node of the self-cascode cell has been shown o be a PTAT voltage whenever the transistors operate at constant inversion levels i.e. the transistor currents are proportional to the specific current I_{SQ}. Interestingly, the absolute value of the PTAT voltage and its derivative can be adjusted by means of the inversion level. Transistors $M_{2,4}$ have to be saturated, whereas $M_{1,3}$ are in triode. The use of (1), (2) and (3) demonstrates that

$$V_{X,12} = \phi_t[F(i_{f1}) - F(i_{f2})] \tag{4}$$

$$V_{X,34} = \phi_t[F(i_{f3}) - F(i_{f4})] \tag{5}$$

where $V_{X,12}$ and $V_{X,34}$ will be ideally PTAT for any inversion level, as long as i_{f1-4} are kept constant over temperature.

From (2) and (3), one can see that an NMOSFET with grounded source and operating under a constant forward inversion level equal to 3 ($i_f = 3$) will have a gate voltage V_G equal to the threshold voltage V_{T0}. Suppose then that M_1 operates under such condition, being in the moderate inversion region. We can then derive the current I_X based on the inversion levels of M_1 and M_2. Since M_1 and M_2 have the same gate and bulk voltages, and share a common drain-source terminal, we know that $i_{f2} = i_{r1}$, which allows us to write

$$I_{D1} = S_1 I_{SQ}(3 - i_{f2}) = 2I_X \tag{6}$$

where i_{f2} defines the voltage $V_{X,12}$ according to (4). The inversion levels i_{f3-4} can then be defined to make $V_{X,12} = V_{X,34}$, and the circuit will be in equilibrium.

IV. Design Methodology

We have assumed an equal current between all branches, being useful to define I_X as a fraction of the specific current:

$$I_X = I_{SQ}/A \tag{7}$$

where A is a design constant used to determine the power consumption of the whole circuit ($I_{TOTAL} = 4I_X$). We also define another design constant $B = i_{f2}/i_{f3}$, that sets the difference between the inversion levels of each SC cell. By choosing a voltage $V_X = V_{X,12} = V_{X,34}$, it is possible to derive all inversion levels and aspect ratios for transistors M_1-M_4.

We present a design example with $A = 10$ and $B = 5$. Other values can be chosen, and due considerations will be made later on. If $i_{f1} = 3$, then $V_{X,12}$ is determined solely from i_{f2}, according to (4). Through design constant B the forward inversion level of M_3 is also defined, which leaves the ratio i_{f4}/i_{f3} to make $V_{X,34}$ equal to $V_{X,12}$. This is graphically illustrated on Figure 2.

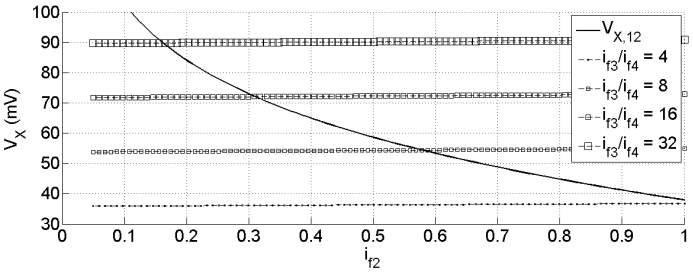

Fig. 2. $V_{X,12}$, $V_{X,34}$ vs i_{f2} at i_{f1} = 3.

In Figure 2 the forward inversion level of M_2 is on the X axis. The solid line represents the voltage $V_{X,12}$, while the marked lines are $V_{X,34}$ for different i_{f3}/i_{f4} ratios. The circuit's DC operating point is located at the crossing of the solid with the marked lines. For example, we pick $V_X = 58$ mV, which leads to $i_{f2} = 0.5$ and $i_{f3}/i_{f4} \approx 10$. The more orthogonal the crossing between the lines, the less sensitive the operating point is, at the expense of a larger area for M_4.

The sizing of the transistors can then be determined from (1) and (6). Again this is shown graphically on Figure 3, that plots S_x as a function of i_{fx}. It is useful to remember that in this design example $i_{f3} = i_{f2}/5$, and that $i_{f4} = i_{f3}/10$.

From Figure 3 we determine the two design vectors, i_{fx} and S_x that represent the forward inversion level of M_{1-4} and their respective aspect ratios.

$$i_{fx} = [3 \cdot 0.5 \cdot 0.1 \cdot 0.01] \tag{8}$$

$$S_X = [0.08 \cdot 0.2 \cdot 2 \cdot 10] \tag{9}$$

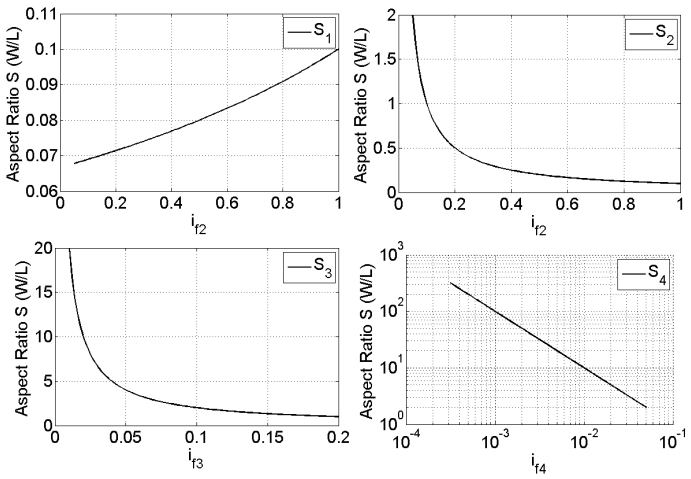

Fig. 3. Sizing of transistors M_1-M_4.

For the ideal circuit behavior, we have assumed that all transistors have the same process characteristics (V_{T0}, I_{SQ}, n, and so on). It is thus a good design practice to use series-parallel associations of unitary transistors to compose M_1-M_4, implementing common-centroid structures and dummies to provide a regular layout, and minimizing differences between the threshold voltage of the devices. Using (9) the sizing of M_1-M_4 becomes that of Table I, for a unitary transistor of $W = 2\mu$m and $L = 5\mu$m.

TABLE I. SIZING OF M_1-M_4 ACCORDING TO (9).

A = 10, B = 5	M1	M2	M_3	M4
W (μm)	2	2	5*2	25*2
L (μm)	5*5	2*5	5	5
Area (μm^2)	50	20	50	250

It is important to realize that this design methodology and the resulting sizing is independent of the chosen technology, as long as the assumptions made are respected. We now consider some practical implementation trade-offs such as power consumption, area, minimum power supply and V_{T0}.

A. Power Consumption and Area Trade-Off

Suppose we want to reduce the power consumption by an order of magnitude ($A = 100$). The resulting inversion level vector remains the same of (8), but (9) becomes (10).

$$S'_X = [0.008 \cdot 0.02 \cdot 0.2 \cdot 1] \tag{10}$$

Table II shows the resulting sizing, considering the same unitary transistor. The area occupied by $A = 100$ has increased by almost 10 times. Of course, it depends on the unitary transistor chosen, but the trade-off is clear.

B. Sizing for Local Variability Mismatches

The proposed sizing of Table I works well for the typical process condition, where no mismatch exists between each device. However, the circuit's equilibrium operating point is heavily affected by local random variations between the devices. As defined by Pelgrom's equation [15], the local mismatches are roughly proportional to $1/\sqrt{WL}$. Therefore, to achieve a reasonable performance, we stipulate that each transistor of the SC cells must have approximately the same area of M_4, which is the largest transistor. This leads to the updated sizing of Table III, maintaining the same inversion levels and aspect ratios of (8) and (9).

TABLE II. SIZING FOR 10X LESS POWER CONSUMPTION (10).

A = 100, B = 5	M1	M2	M_3	M4
W (μm)	2	2	2	25*2
L (μm)	50*5	20*5	2*5	10*5
Area (μm^2)	500	200	20	2500

TABLE III. UPDATED SIZING TO ACCOUNT FOR LOCAL MISMATCHES.

A = 10, B = 5	M1	M2	M_3	M4
W (μm)	4 (2*2)	6 (3*2)	20 (10*2)	50 (25*2)
L (μm)	50 (10*5)	30 (6*5)	10 (2*5)	5
Area (μm^2)	200	180	200	250

It is useful to remember that the drain current mismatch increases sharply for weak inversion operation, and that $i_{f1} > i_{f2} > i_{f3} > i_{f4}$. So, M_4 should probably have a slightly larger area than the others.

C. Minimum V_{DD} and V_{T0}

Referring to the circuit of Figure 1, assume that $V_{G1} > V_{G4}$. Then, there is a minimum value for the power supply that is defined by (11). We have designed transistors M_{5-M10} to be in weak inversion (which keeps $V_{DD,min}$ as low as possible), where we assume they will be saturated for $V_{DS,5-10} > 4\phi_t$.

$$V_{DD,min}(T) > V_{T0}(T) + 4\phi_t \tag{11}$$

There is also a lower limit for the threshold voltage value to be extracted, imposed by the condition that M_4 must be in saturation. This means that $V_{G4} > V_{X,34} + 4\phi_t$. (2), (3) and (5) define the minimum threshold value (12). In the case of this design example, (12) results in $V_{T0,min}(27°C) > 300$ mV.

$$V_{T0,min}(T) > \phi_t\left[(1-n)F(i_{f3}) - F(i_{f4})\right] + 4\phi_t \tag{12}$$

V. SIMULATION RESULTS

The results presented here are for SPICE schematic simulations in XFAB 180 nm. By using the g_m/I_D methodology described in [7], we find that $V_{T0}(27°C) = 426$ mV. In Figure 4(a) the estimated V_{T0} over temperature is shown, as defined by the model (ACM) through the g_m/I_D methodology, and as extracted by the circuit (VTEX). In Figure 4(b), we present the error - the difference between the two curves, being inferior to 7 mV over an extended temperature range.

Figure 5(a) shows that the Power Supply Rejection Ratio (PSRR) for V_{G1}, simulated at 100 Hz and $V_{DD} = 1.2$ V, is -38.9 dB. As predicted by (11), this implementation starts operating around 550 mV - Figure 5(b). The circuit consumes only 23 nW at room temperature, and reaches a maximum of

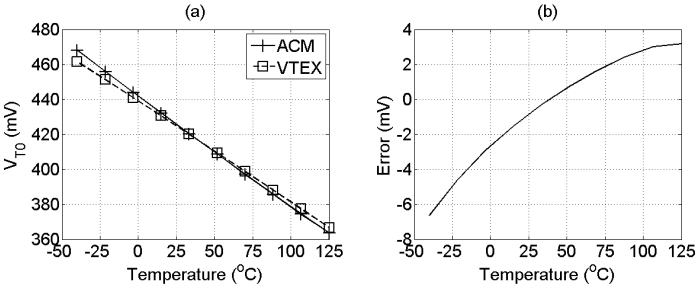

Fig. 4. Model (ACM) and extracted (VTEX) (a) voltages; (b) difference.

33 nW at 125 °C. The line sensitivity of V_{G1} is 3.6 mV/V while the current consumption sensitivity is 2.6 nA/V, both at 27 °C and from 0.6 V to 1.8 V.

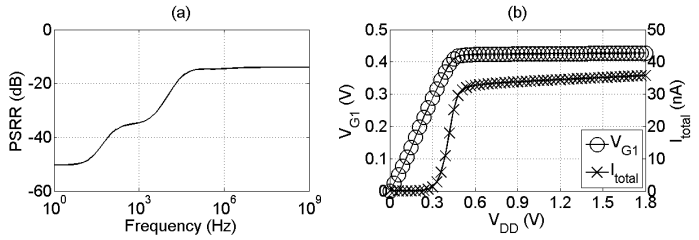

Fig. 5. Line regulation at 27°C. (a) PSRR; (b) V_{G1} and I_{TOTAL} vs V_{DD}.

A. Fabrication Variability

To analyze the fabrication variability of the error on the extracted threshold voltage, Monte Carlo (MC) simulations were done separately for local mismatch (LM) effects and average process (AP) variations, with 300 runs each - Figure 6. For AP MC, all the transistors have their parameters changed equally in each run (top). For LM MC, the parameters of each transistor are varied individually in each run (bottom). The results presented are for $V_{DD} = 0.7$ V at -40, 27 and 125 °C.

As shown in the design methodology, the circuit's equilibrium point depends only on geometrical factors. It is thus less sensitive to average process variations. LM variability, however, affects the current mirror and aspect ratio gains that define the V_X and I_X equality, resulting in a higher spread. Still, the maximum expected error falls within ±20 mV for the whole operating temperature range. The mean and standard deviations are shown in Figure 6.

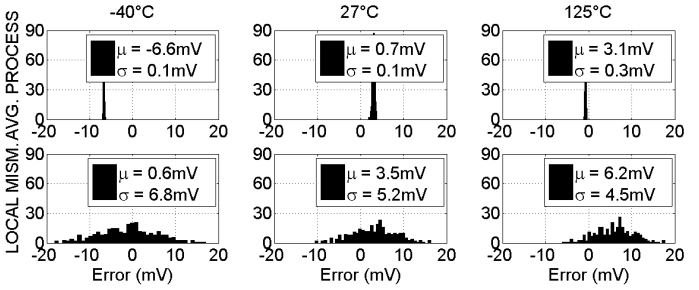

Fig. 6. Histogram of the error for 300 MC runs. Average process variation (top) and local random mismatch (bottom).

VI. Conclusion

A resistorless ultra-low-power threshold voltage monitor circuit was presented, described by a continuous physical MOSFET model. It is a self-biased topology composed by transistors operating in weak and moderate inversion, that works with $V_{DD,min}(T) \geq V_{T0}(T) + 4\phi_t$. Typical simulations of a 0.18μm CMOS process demonstrate an error for the extracted threshold voltage value inferior to 7 mV, at an extended temperature range of -40 to 125 °C. The circuit consumes 23 nW at room temperature with $V_{DD} = 0.6$ V. Monte Carlo simulations show that the maximum error spread is ±20 mV, dominated by local random variability.

Acknowledgment

The authors are grateful to CNPq, MOSIS and the CI-BRASIL program for financial support and PDK licensing.

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