Ultra-low-voltage CMOS circuit design

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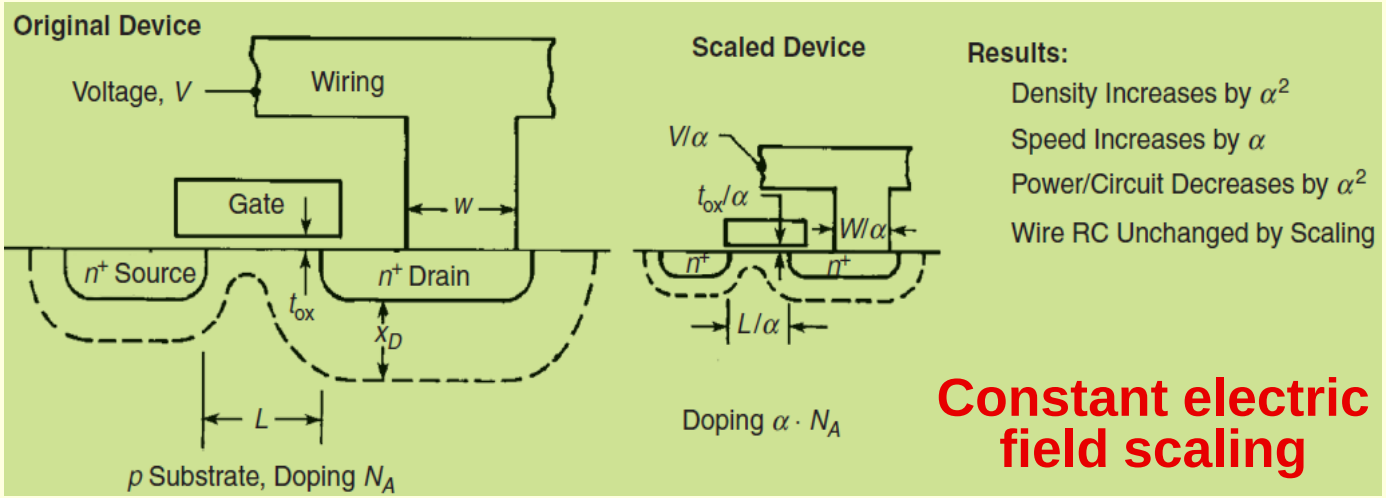
https://www.lci.ufsc.br/

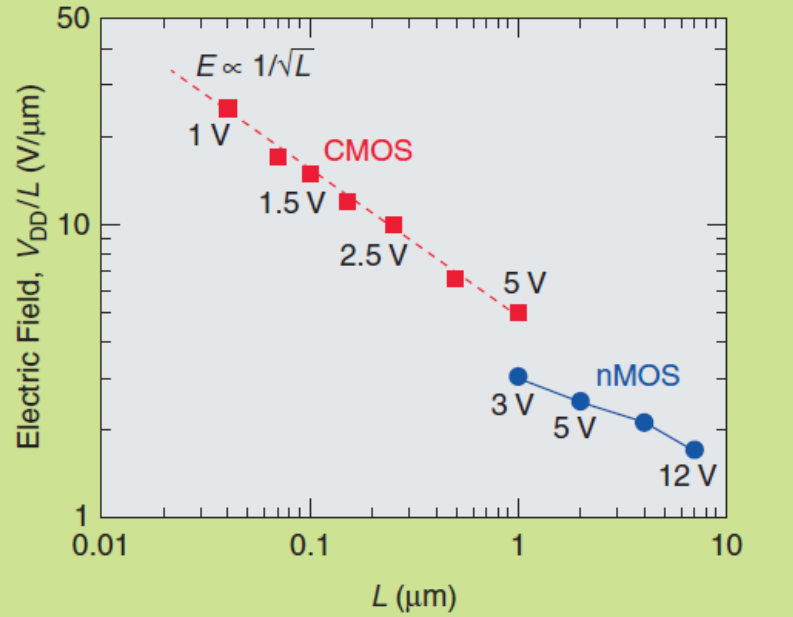
Outline

- 1. Introduction
- 2. Subthreshold MOSFET model
- 3. Ultra-low-voltage (ULV) CMOS digital circuits
- 4. ULV LC tank oscillators
- 5. ULV rectifiers and voltage multipliers

Motivations for low voltage

1. Scaling





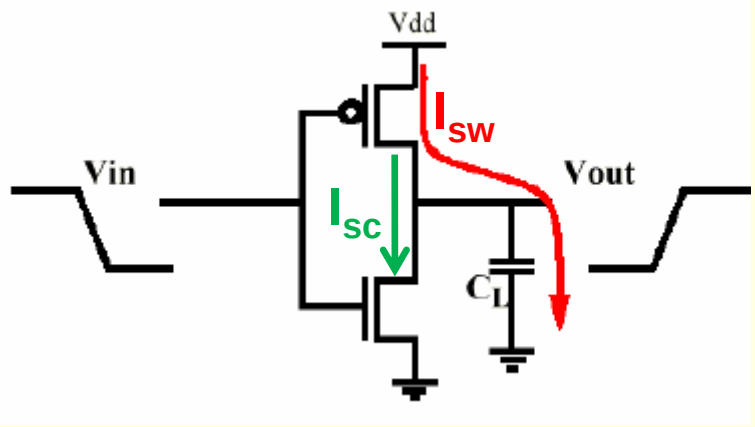
R. H. Dennard et et. al.
IEDM 72 & IEEE JSSC,
Oct. 1974

Motivations for low voltage

2. Power dissipation

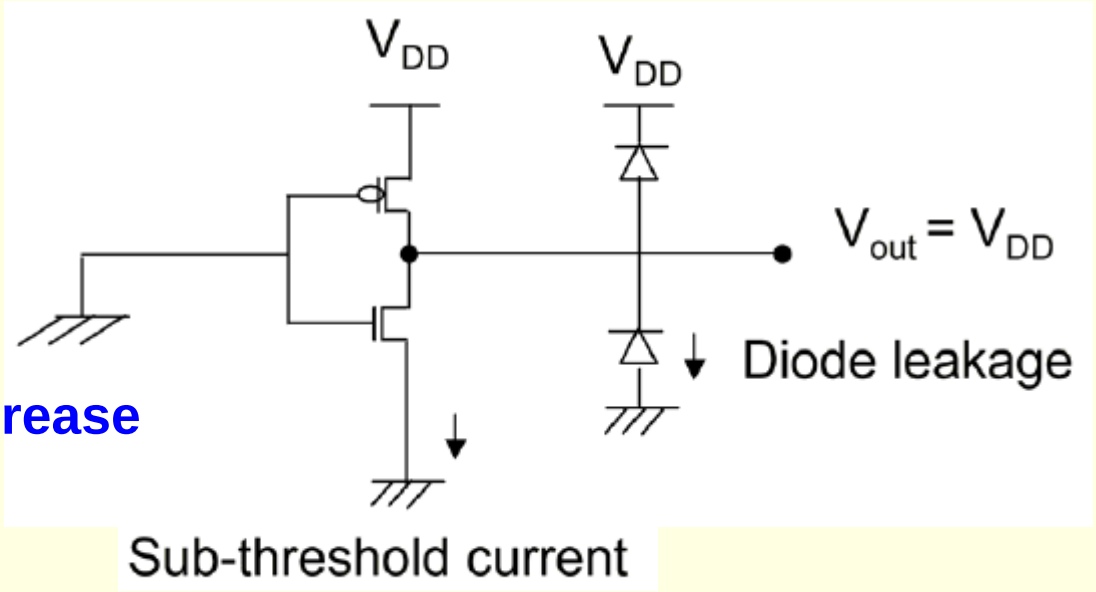
Switching power

$$\text{Power} = \text{Energy/transition} * f = C_L * V_{dd}^2$$



Short-circuit power :
due to non-zero rise/fall times

Leakage power α V_{DD}



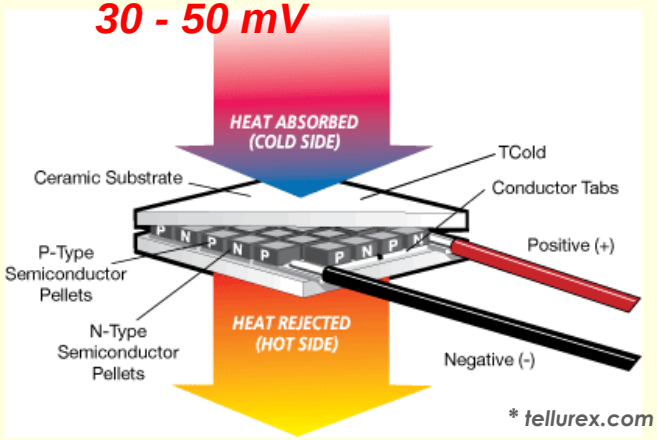
Most effective way to decrease power is to lower V_{DD}

Motivations for low voltage

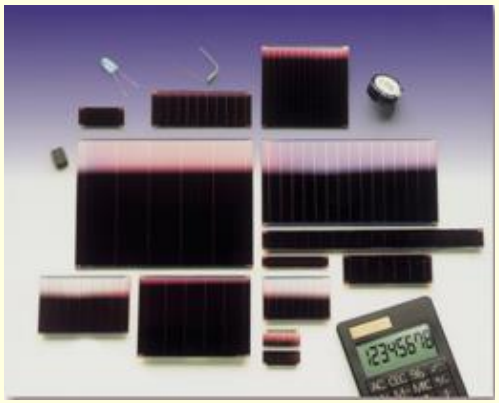
3. Low supply voltages

Thermoelectric generator

$V_{o(body\text{-}environment)} \approx$ *30 - 50 mV*



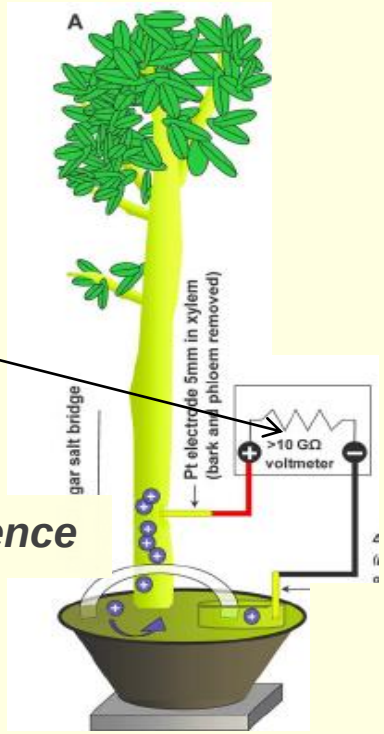
Photovoltaic cell



$V_{o(dark\ room)} \approx$ *100 - 200 mV*

Energy provided by trees

Vo ≈ 20-200 mV

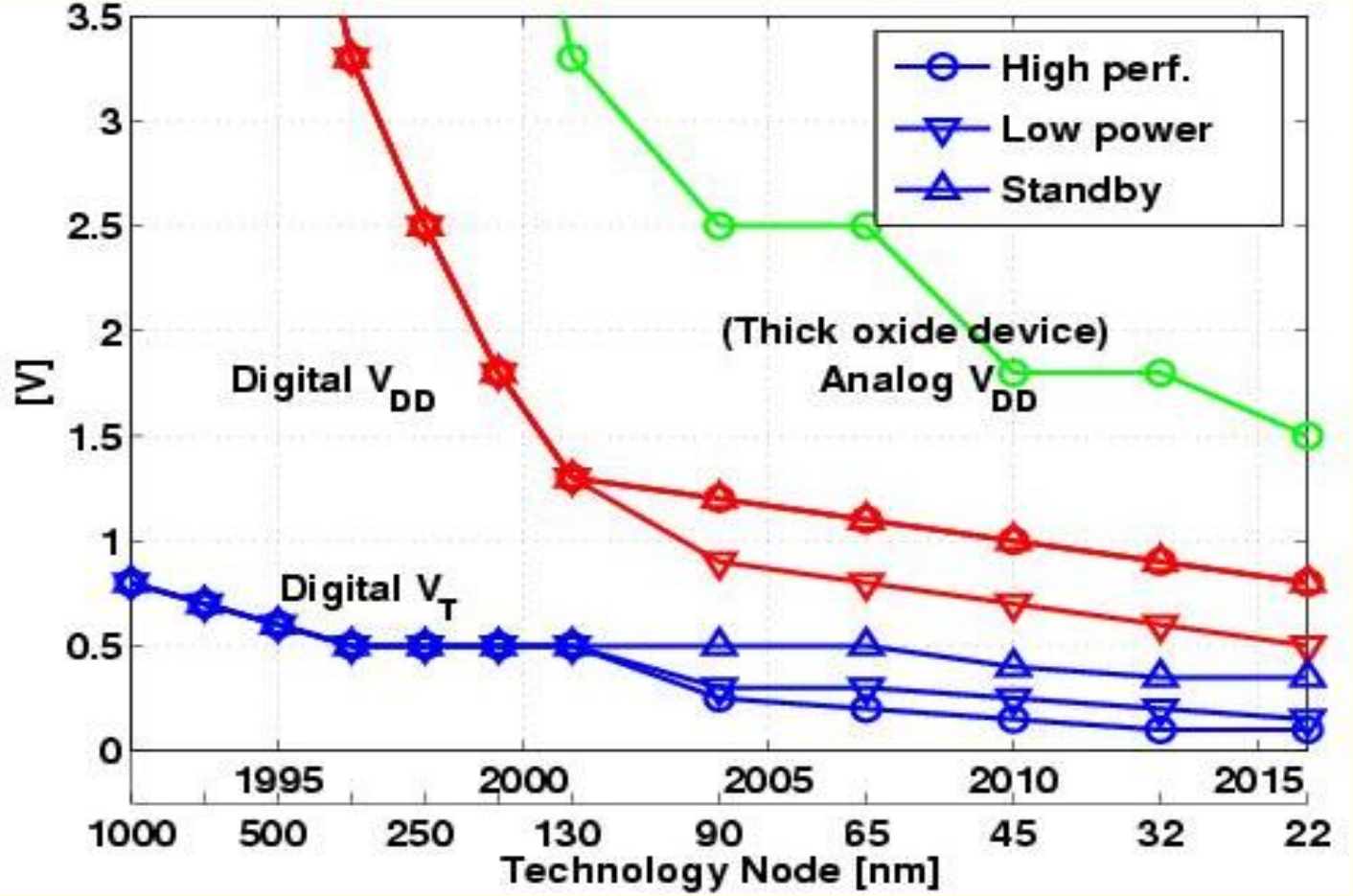


pH difference

** Love et al, "Source of sustained voltage difference between the xylem of a potted ficus benjamina tree and its soil", 2008.*

The trend toward low supply voltages

- Q1-Is there a lower bound for the supply voltage?
- Q2-What are the best technologies for ULV circuits?



Voltage scaling is slowing / stopping

http://www.cisl.columbia.edu/grads/tuku/research/

CMOS supply voltages

- **Ultra low voltage (V_{DD} ~ 100 mV @ 300 K)**

  3-parameter MOSFET model (long-channel model)

- **Low voltage**

  4-parameter MOSFET model (long-channel model + DIBL)

- **Standard voltage (VDD ~ 1 V @ 300 K)**

  5-parameter MOSFET model (long-channel model + DIBL+ saturation velocity)

References

- J. M. Rabaey, “The power wall: are we scaling it or is it just getting higher?,” EPUSP, São Paulo, Nov. 2012.
- Y. Ramadass, “Energy harvesters and energy processing circuits,” ISSCC, San Francisco, Feb. 2013.

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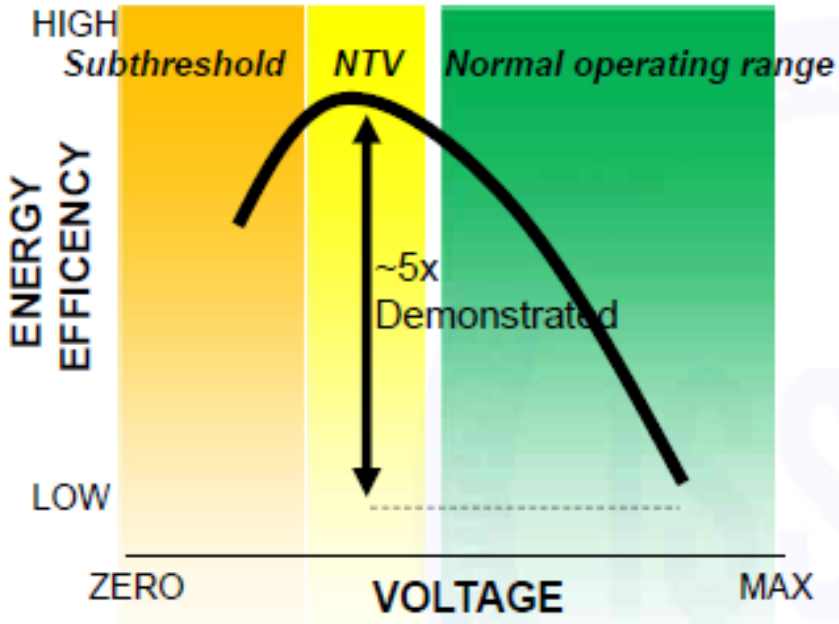
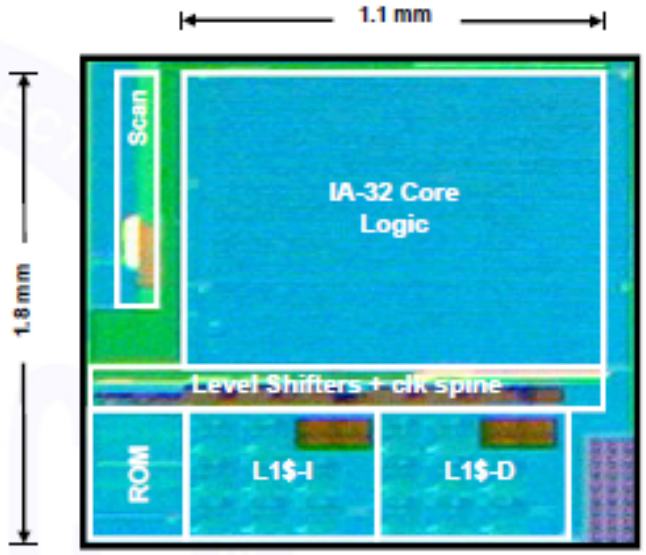
NTV Pentium® Processor





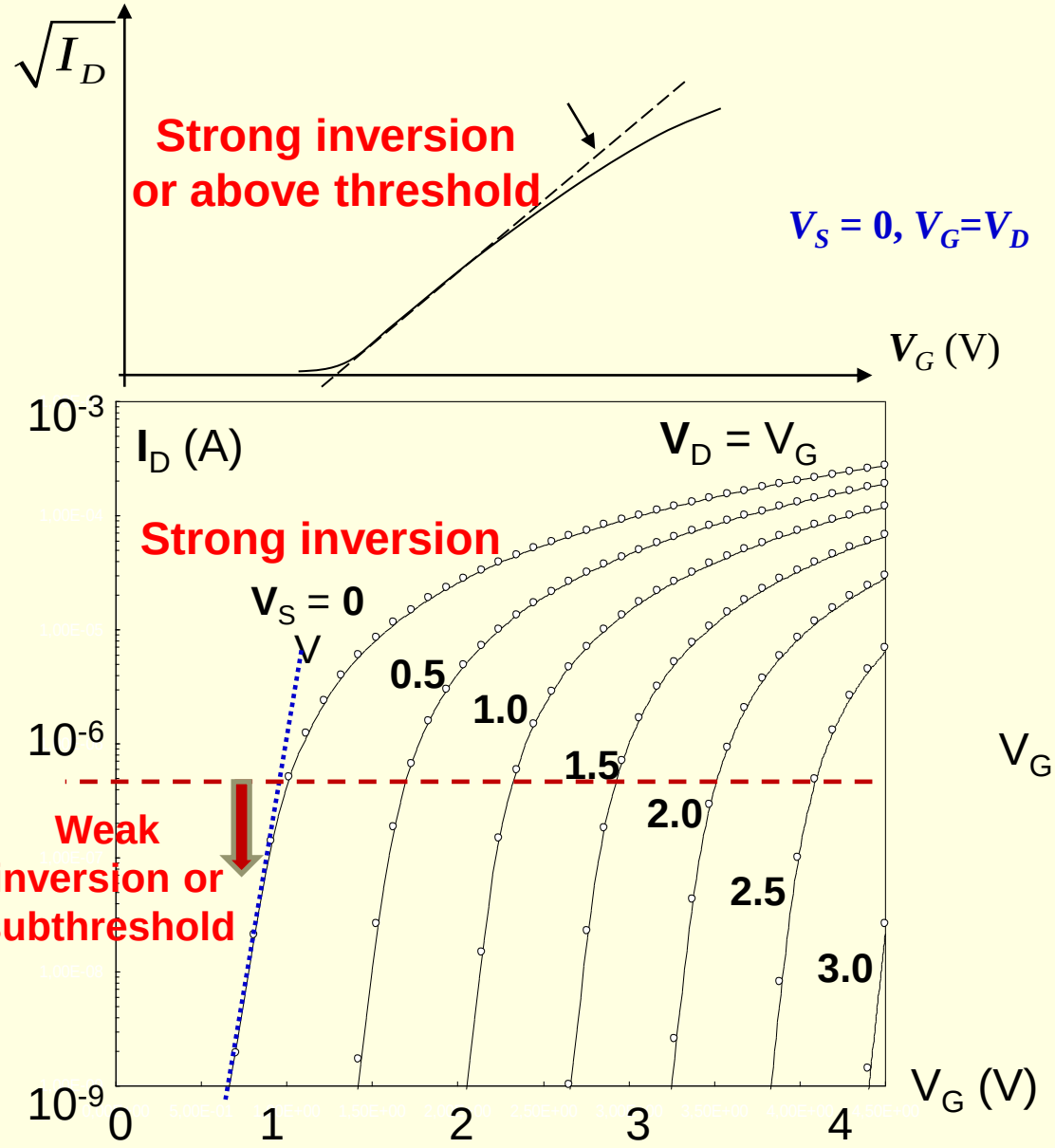
Ultra-low Power	Energy Efficient	High Performance
280 mV	0.45 V	1.2 V
3 MHz	60 MHz	915 MHz
2 mW	10 mW	737 mW
1500 Mips/W	5830 Mips/W	1240 Mips/W

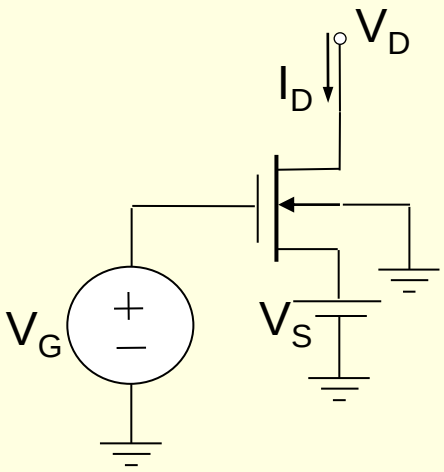
Technology	32nm High-K Metal Gate
Interconnect	1 Poly, 9 Metal (Cu)
Transistors	Core:6M
Core Area	2mm^2
Package	951 Pins FCBGA11

Wide Dynamic Range

S. Jain, S. Khare et. al. "A 280mV-to-1.2V Wide-Operating-Range IA-32 Processor in 32nm CMOS," ISSCC 2012

MOS transistor





Inversion level

WI and SI (and the all-region) currents can be written as

$$I_D = \frac{W}{L}\left[f(V_{GB}, V_{SB}) - f(V_{GB}, V_{DB})\right]$$

Denoting $\dfrac{f\left(V_{GB}, V_{S(D)B}\right)}{I_{SH}} = i_{f(r)}$

where I_{SH} is a (constant) normalization current $I_{SH} = \mu C_{ox} n \phi_t^2 / 2$

μ: carrier mobility

C_{ox}: oxide capacitance unit area

n: slope factor (= 1.05 - 1.3)

$\phi_t = \dfrac{kT}{q} (= 26\ \text{mV} @ 300\text{K})$

$i_{f(r)}$ is the forward (reverse) inversion level

$$I_D = \frac{W}{L} I_{SH}\left[i_f - i_r\right]$$

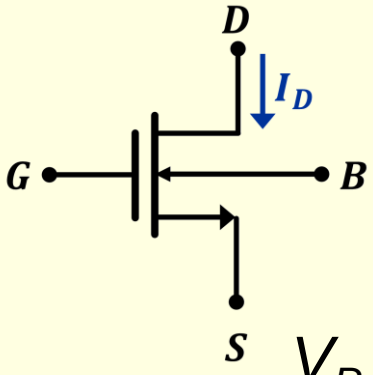
In saturation, I_D ~ *constant* and $i_r << i_f$

The 4-parameter model

$$\frac{V_P - V_{S(D)B}}{\phi_t} = \sqrt{1 + i_{f(r)}} - 2 + \ln\left(\sqrt{1 + i_{f(r)}} - 1\right)$$

$$I_D = I_S\left(i_f - i_r\right) = I_{SH}\frac{W}{L}\left(i_f - i_r\right)$$

$$V_P = \frac{V_{GB} - V_{T0} + \sigma V_{DB} + \sigma V_{SB}}{n}$$



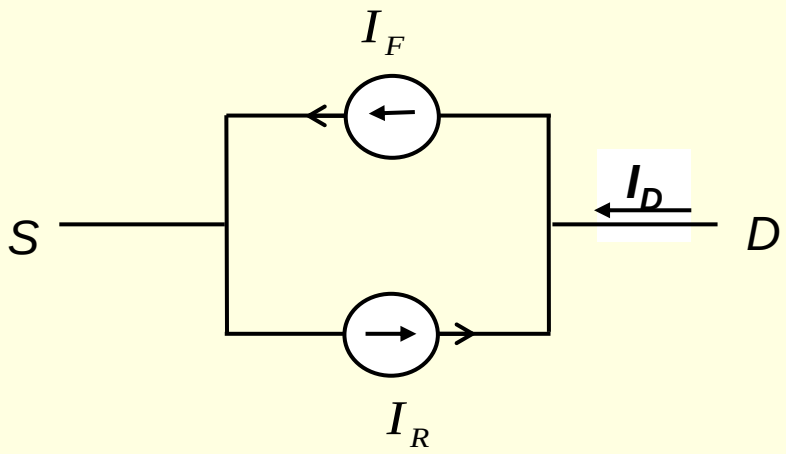
V_P : pinchoff voltage

Specific current	Threshold voltage	Slope factor	DIBL factor
I_S	V_{T0}	n	σ

MOSFET: Weak inversion (WI) model-1

$$I_D = I_F - I_R = I_0\left(e^{\frac{V_P - V_{SB}}{\phi_t}} - e^{\frac{V_P - V_{DB}}{\phi_t}}\right)$$

$$V_P \cong \frac{V_{GB} - V_{T0}}{n} \qquad I_0 = \mu C_{ox} n \phi_t^2 e^1 (W/L)$$

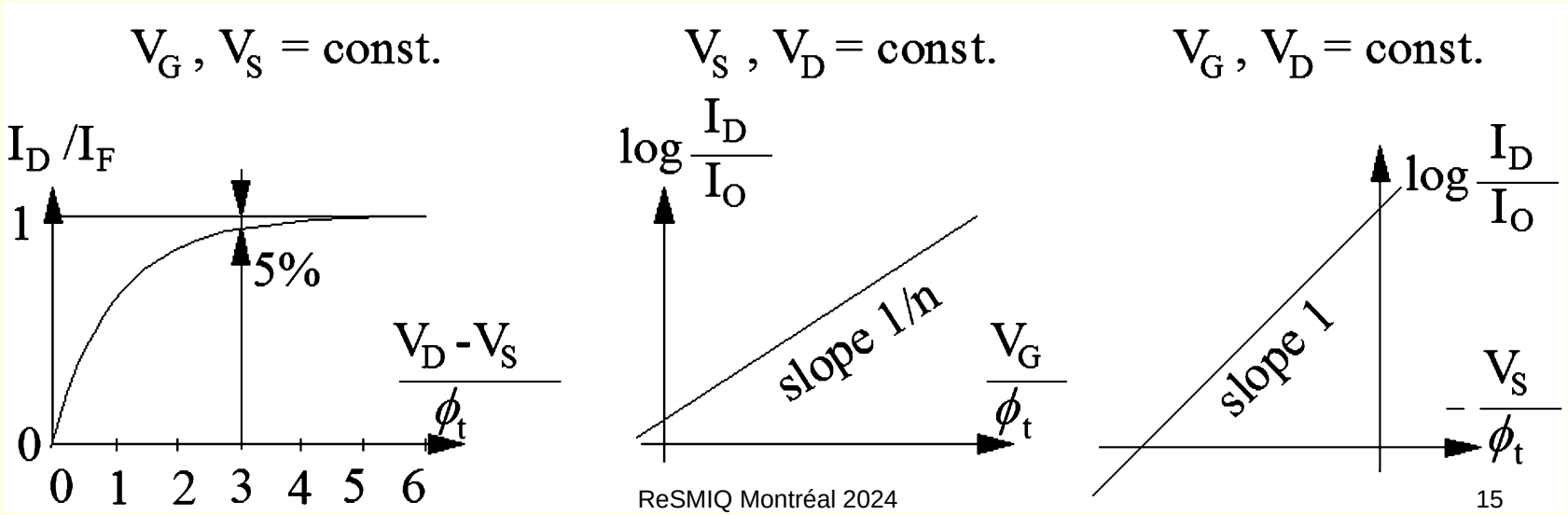


Weak inversion MOSFET model-2

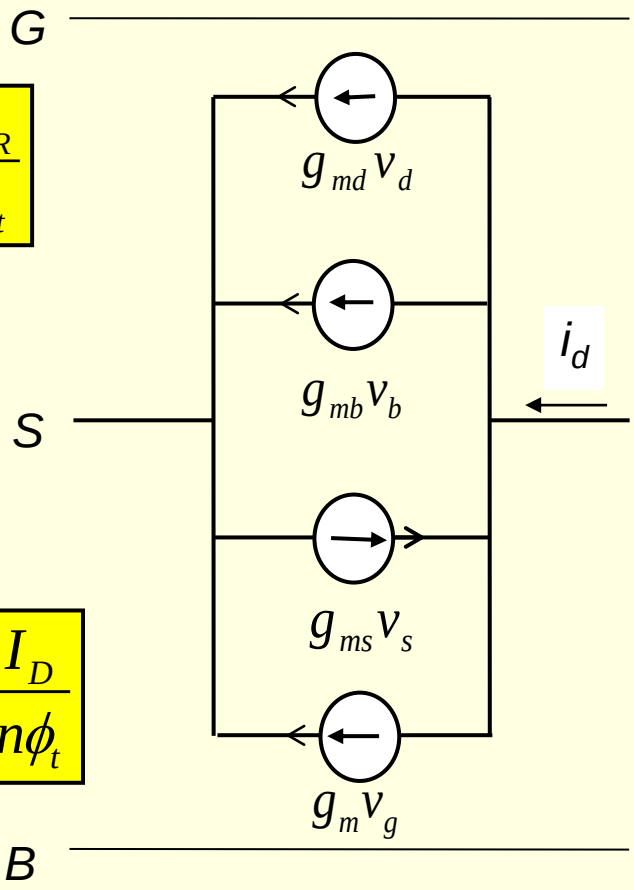
$$I_D = I_0 e^{\left(\frac{V_{GS}-V_T}{n\varphi_t}\right)}\left[1 - e^{-V_{DS}/\varphi_t}\right]$$

$$I_0 = \mu C_{ox} n \phi_t^2 e^1 (W/L)$$

$$V_T = V_{T0} + (n-1)V_{SB}$$



MOSFET: low-frequency small-signal model in weak inversion



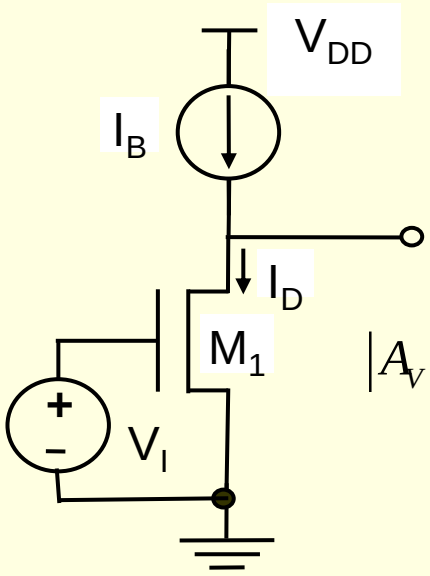
$$g_{md} = \frac{I_R}{\phi_t}$$

$$g_m = \frac{g_{ms} - g_{md}}{n} = \frac{I_D}{n\phi_t}$$

$$g_{ms} = \frac{I_F}{\phi_t}$$

$$g_{ms} = g_m + g_{mb} + g_{md}$$

Low-voltage operation of the common-source amplifier



Intrinsic gain stage

(I_B ideal current source)

$$|A_V| = \frac{g_m}{g_{md}} = \frac{g_{ms} - g_{md}}{n g_{md}} = \frac{1}{n}\left(\frac{g_{ms}}{g_{md}} - 1\right)$$

weak inversion operation

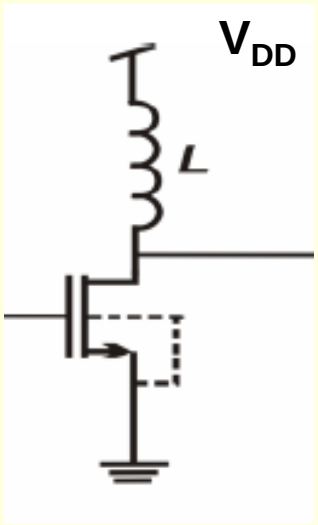
$$\frac{g_{ms}}{g_{md}} = e^{\frac{V_{DS}}{\phi_t}}$$

$$|A_V| = \frac{1}{n}\left(e^{\frac{V_{DS}}{\phi_t}} - 1\right)$$

or

$$V_{DS} = \phi_t \ln\left(1 + n|A_V|\right)$$

Low–voltage operation of the (C)MOS inverter



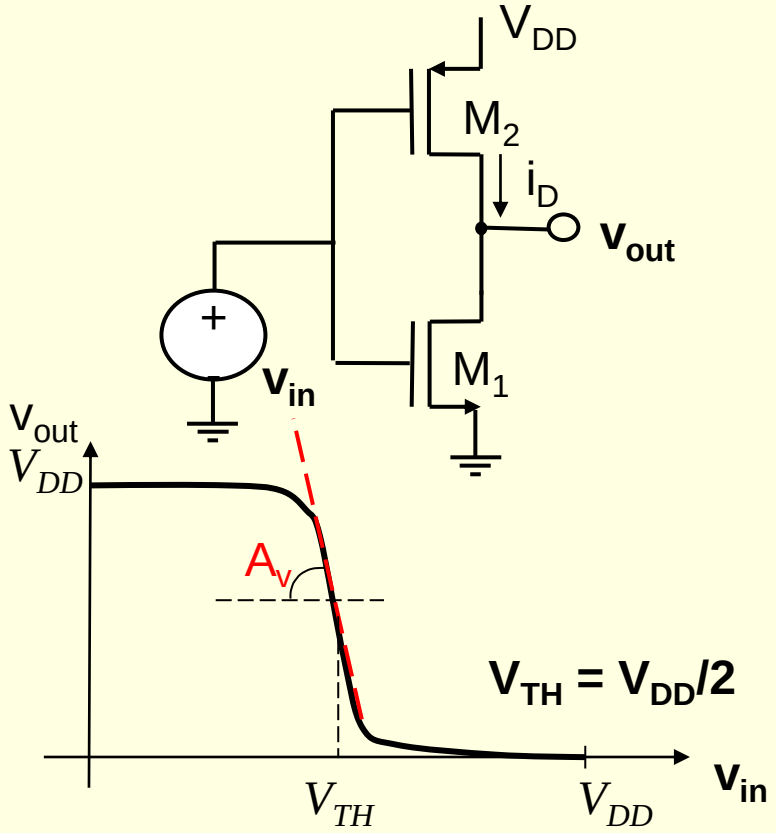
$$V_{DS} = \phi_t \ln\left(1 + n\left|A_V\right|\right)$$

Minimum supply voltage for amplification $|A_V| = 1$

'ideal' MOSFET ***n*** **= 1**

$$V_{DS} = V_{DD}$$

$$V_{DD\min} = (\ln 2)\phi_t$$

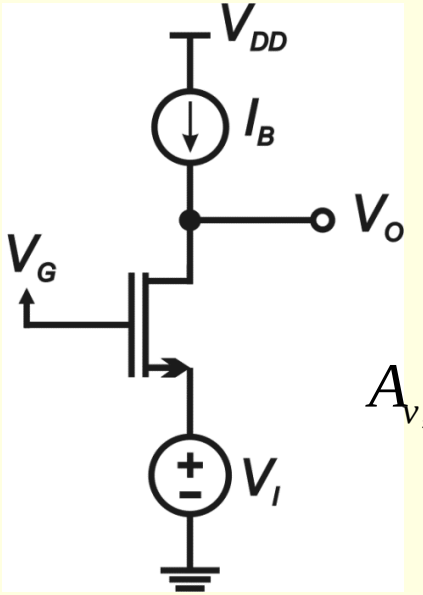


$$V_{DS} = V_{DD} / 2$$

$$V_{DD\min} = 2(\ln 2)\phi_t$$

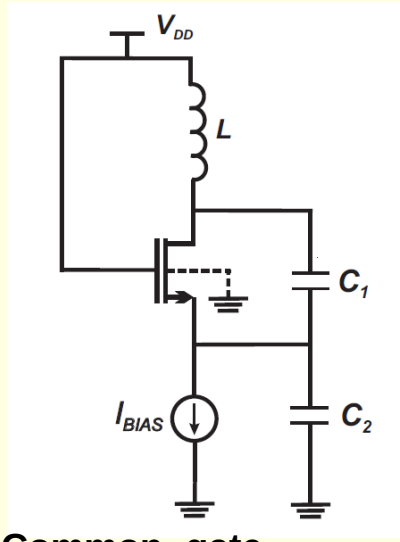
J. Meindl, IEEE JSSC, 2000

Low-voltage operation of the common-gate amplifier



$$A_{v,cg} = \frac{v_o}{v_i} = \frac{g_{ms}}{g_{md}} = e^{\frac{qV_{DS}}{kT}}$$

The common-gate amplifier provides a voltage gain of greater than unity for $V_{DS}>0$. → Very useful property for lowering the supply voltage limit for the operation of oscillators (later).



Common- gate Colpitts oscillator

References

- E. Vittoz, “Weak inversion for ultimate low-power logic”, in *Low-Power Electronics Design*, CRC Press, 2005.
- Márcio Cherem Schneider and Carlos Galup-Montoro, *CMOS Analog Design Using All-Region MOSFET Modeling*, Cambridge University Press, 2010.
- C. M. Adornes *et al*. " Bridging the Gap between Design and Simulation of Low-Voltage CMOS Circuits ," Journal of Low Power Electronics and Applications, vol. 12, issue 2, June 2022.

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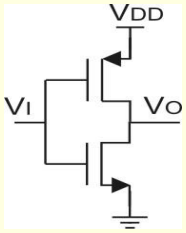
THE CMOS INVERTER IN WEAK INVERSION 1

$$I_{DN(P)} = I_{ON(P)} \cdot e^{\frac{V_{GB(BG)} - |V_{TN(P)}| - n_{N(P)} \cdot V_{SB(BS)}}{n_{N(P)} \cdot \varphi_t}} \cdot \left(1 - e^{-\frac{V_{DS(SD)}}{\varphi_t}}\right)$$



- The strength or current capability of the transistor is given by

$$I_{N(P)} = I_{ON(P)} \cdot e^{\frac{-|V_{TN(P)}|}{n_{N(P)} \cdot \varphi_t}}$$

- For the sake of simplicity let $n_N = n_P = n$. The static transfer function of the inverter is obtained from

$$I_{DN} = I_{DP}$$

$$I_{ON} \cdot e^{\frac{V_I - V_{TN}}{n \cdot \varphi_t}} \cdot \left(1 - e^{-\frac{V_O}{\varphi_t}}\right) = I_{OP} \cdot e^{\frac{V_{DD} - V_I - |V_{TP}|}{n \cdot \varphi_t}} \cdot \left(1 - e^{-\frac{V_{DD} - V_O}{\varphi_t}}\right)$$

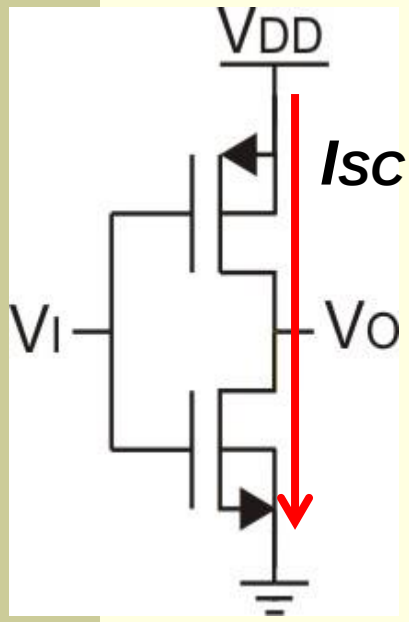
THE CMOS INVERTER IN WEAK INVERSION 2

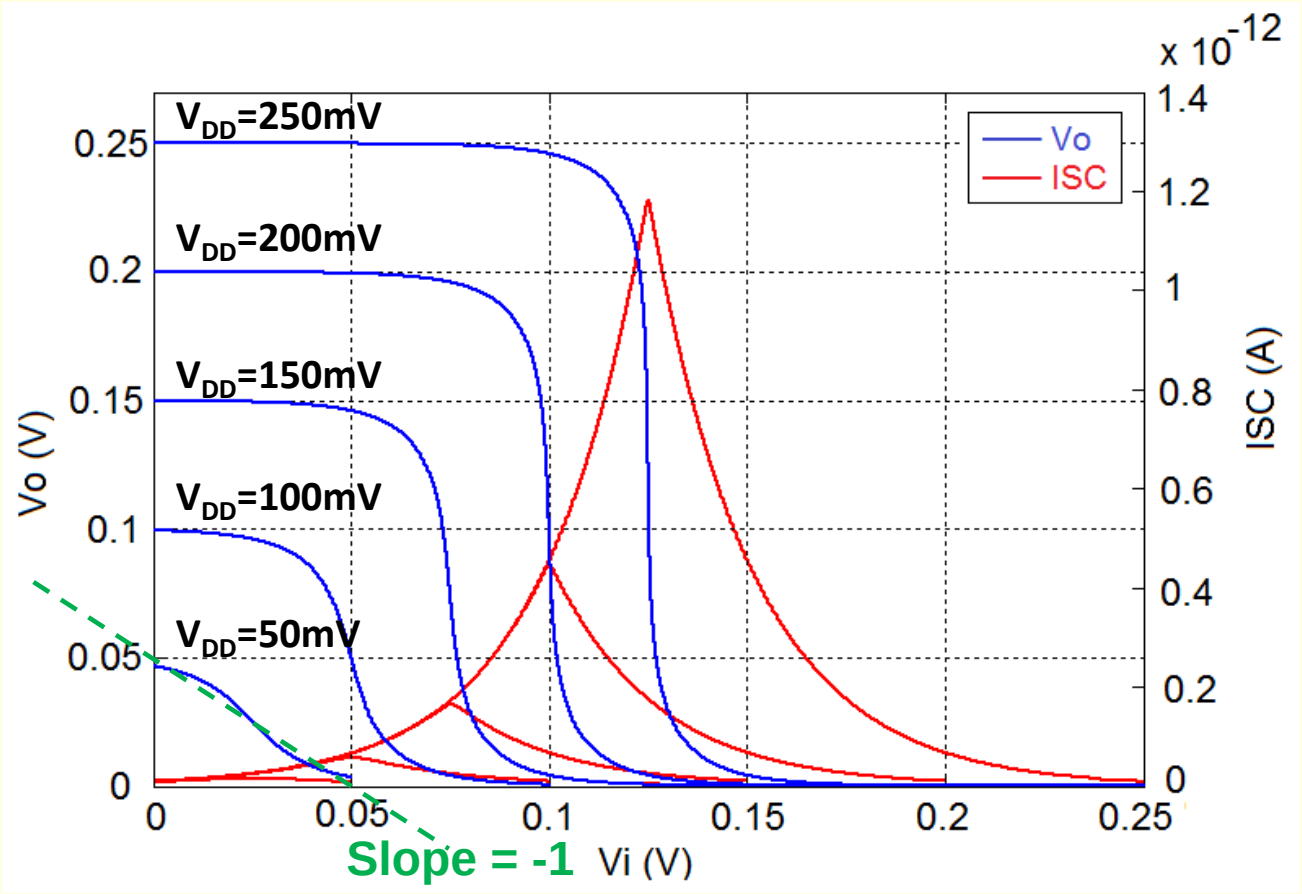
$$V_I = \frac{V_{DD}}{2} + \frac{V_{TN} - |V_{TP}|}{2} + \frac{n \cdot \phi_t}{2} \cdot \ln\left(\frac{I_{OP}}{I_{ON}}\right) + \frac{n \cdot \phi_t}{2} \cdot \ln\left(\frac{1 - e^{-\frac{V_{DD} - V_O}{\phi_t}}}{1 - e^{-\frac{V_O}{\phi_t}}}\right)$$

In the ideal case of NMOS and PMOS transistors with the same strength, i.e. $I_{ON}=I_{OP}$ and $V_{TN}=|V_{TP}|$, the VTC reduces to

$$V_I = \frac{V_{DD}}{2} + \frac{n \cdot \phi_t}{2} \cdot \ln\left(\frac{1 - e^{-\frac{V_{DD} - V_O}{\phi_t}}}{1 - e^{-\frac{V_O}{\phi_t}}}\right)$$

THE CMOS INVERTER IN WEAK INVERSION 3





Note that:

VDD	VoH (Vi = 0)	VoL (Vi = VDD)
200 mV	200 mV	0mV
50 mV	46.6 mV	3.4mV

THE CMOS INVERTER IN WEAK INVERSION 4

- The inverter threshold voltage, V_M, is defined as the voltage such that $V_I=V_O$. In the case for which the transistors have the same strength ($I_N=I_P$) then $V_M=V_{DD}/2$. If the NMOS transistor is stronger than the PMOS transistor, $V_M<V_{DD}/2$, whereas if the PMOS transistor is stronger than the NMOS transistor, $V_M>V_{DD}/2$

$$V_M \approx \frac{V_{DD}}{2} + \frac{\frac{V_{TN}-|V_{TP}|}{2} + \frac{n\cdot\phi_t}{2}\cdot\ln\left(\frac{I_{OP}}{I_{ON}}\right)}{1+\left|\frac{dV_I}{dV_O}\right|_{V_O=\frac{V_{DD}}{2}}}$$

$$\left|\frac{dV_O}{dV_I}\right|_{V_O=\frac{V_{DD}}{2}} = \frac{e^{\frac{V_{DD}}{2\cdot\phi_t}}-1}{n}$$

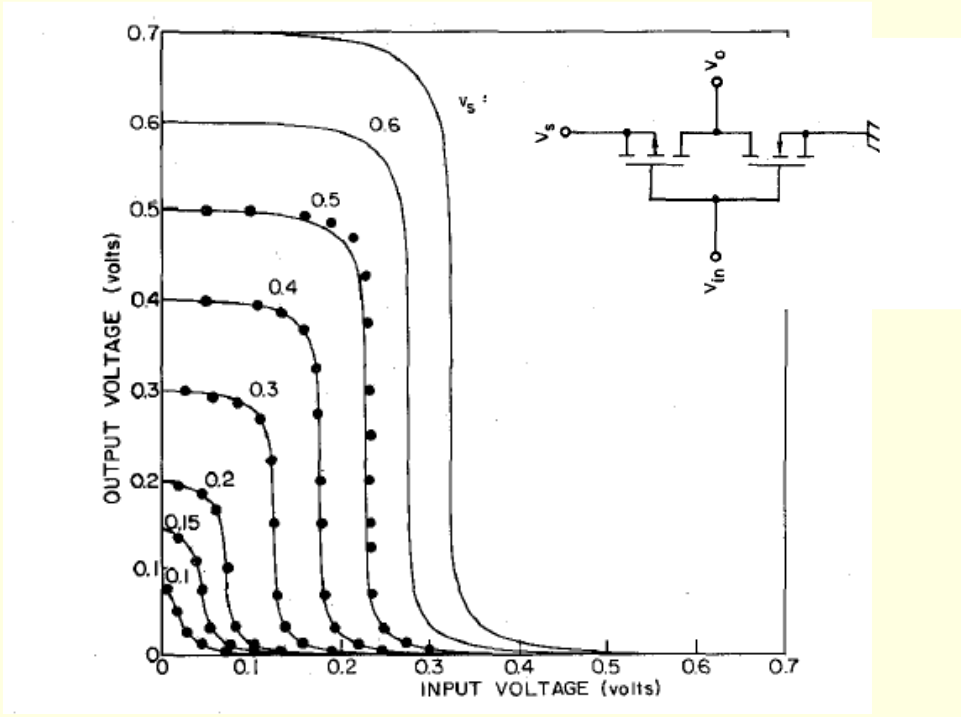
THE CMOS INVERTER IN WEAK INVERSION 5

- The minimum operating supply voltage of the inverter and any CMOS static logic gate must be at least equal to unity, *i.e.*

$$\left|\frac{dV_O}{dV_I}\right|_{V_O=\frac{V_{DD}}{2}} = 1 \qquad \left|\frac{dV_O}{dV_I}\right|_{V_O=\frac{V_{DD}}{2}} = \frac{e^{\frac{V_{DD}}{2\cdot\phi_t}} - 1}{n}$$

$$V_{DD\,\min} = 2\phi_t \ln(2) = 36\text{mV at } 300\text{K}$$

Minimum supply voltage for the CMOS inverter



CMOS inverter transfer characteristics

(Swanson and Meindl, IEEE JSSC 1972)

Prof. James Meindl:
Theoretically, the minimum supply voltage for a CMOS inverter is
2 (ln2) (kT/q) = 36 mV
at room temperature
(IEEE JSSC, 2000)

Minimum Energy per Operation

Predicted by von Neumann: kTln(2)

J. von Neumann,

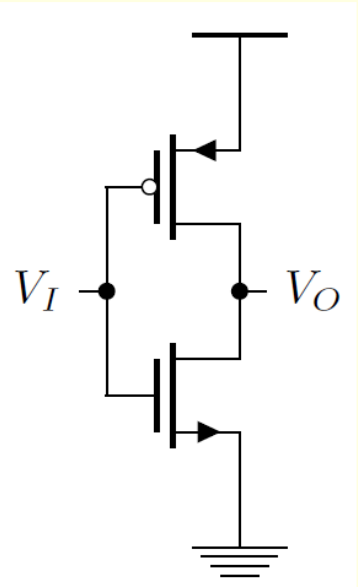
[Theory of Self-Reproducing Automata, 1966].

- Moving one electron over V_{DDmin} =2ln(2)kT/q
  - E_{min} = $QV_{DD}/2$ = q 2(ln2)kT/2q = kTln(2)
  - Also called the *Von Neumann-Landauer-Shannon* bound
  - At room temperature (300K): **Emin = 0.29 10^{-20} J**
- Minimum sized CMOS inverter at 90 nm operating at 1V
  - **E = CV_{DD}^2 = 0.8 10^{-15} J**, or 5 orders of magnitude larger!

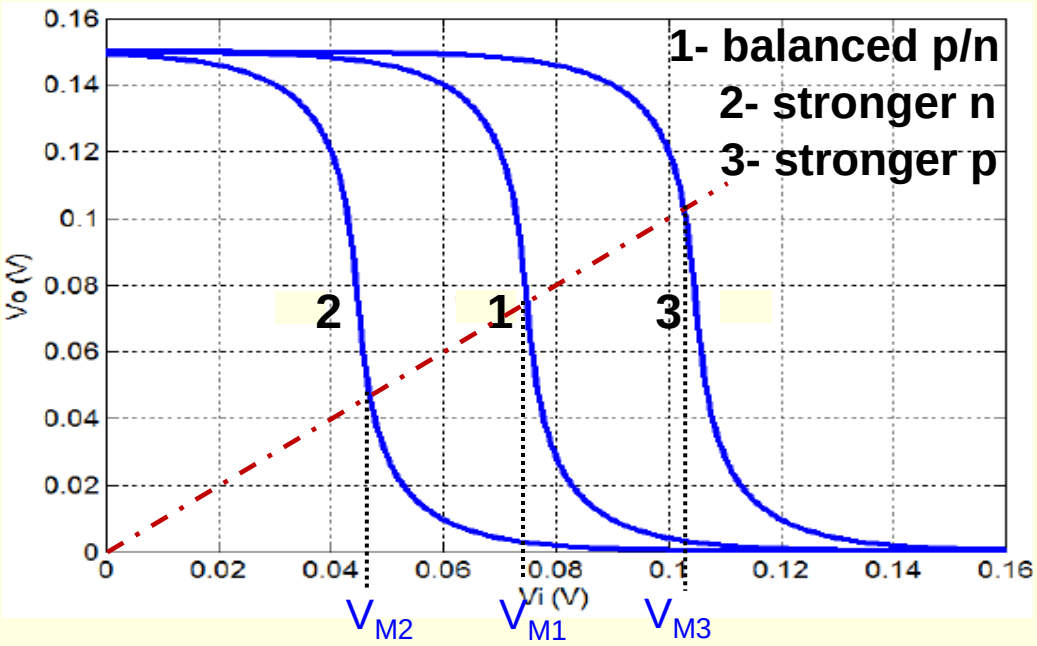
How close can one get?

from J. Rabaey, Low Power Design Essentials, Springer 2009

Imbalance in the CMOS Inverter - 1



Classical CMOS inverter

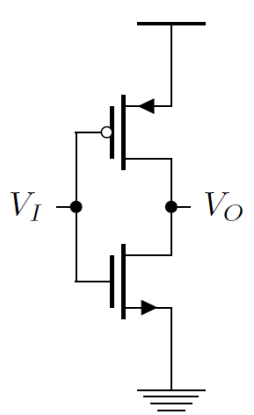


Consequences of imbalance between p/n transistors:

- **Non-centered VTC characteristic ($V_M \neq V_{DD}/2$);**
- **Unbalanced high-to-low and low-to-high transient times;**
- **Reduced noise margin;**
- **Lower gain at the inverter threshold voltage;….**

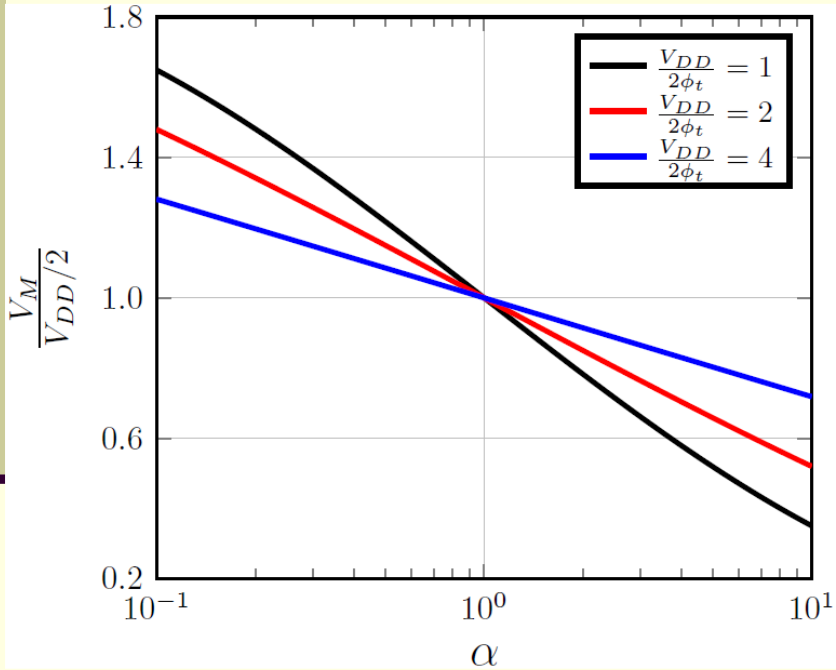
, ….

Imbalance in the CMOS Inverter[1] - 2

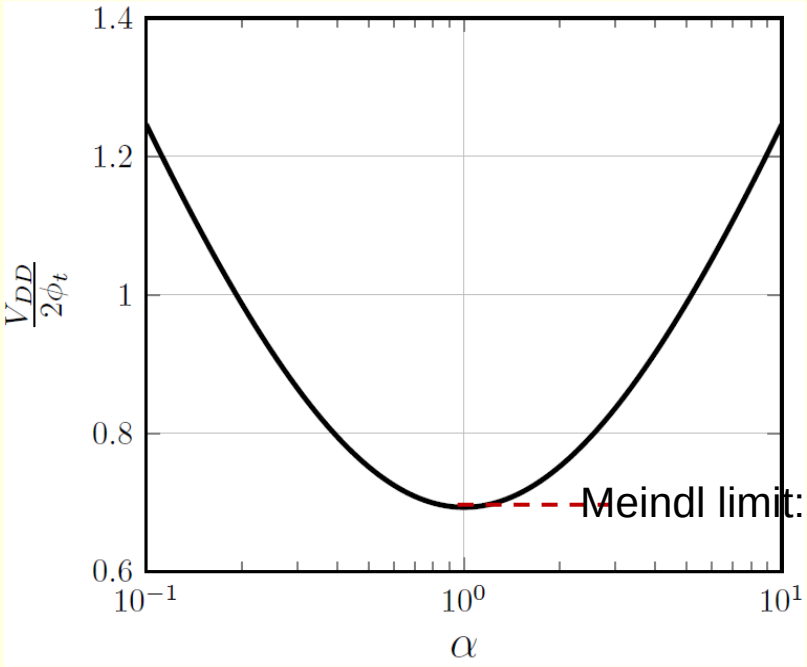


α : off current$|_{NMOS}$/ off current$|_{PMOS}$

$$\alpha = \frac{I_{0N}}{I_{0P}} = \frac{\mu_N \frac{W_N}{L_N} e^{\left(-\frac{V_{TN}}{n\varphi_t}\right)}}{\mu_P \frac{W_P}{L_P} e^{-\left(\frac{|V_{TP}|}{n\varphi_t}\right)}}$$



Inverter threshold voltage V_M versus α



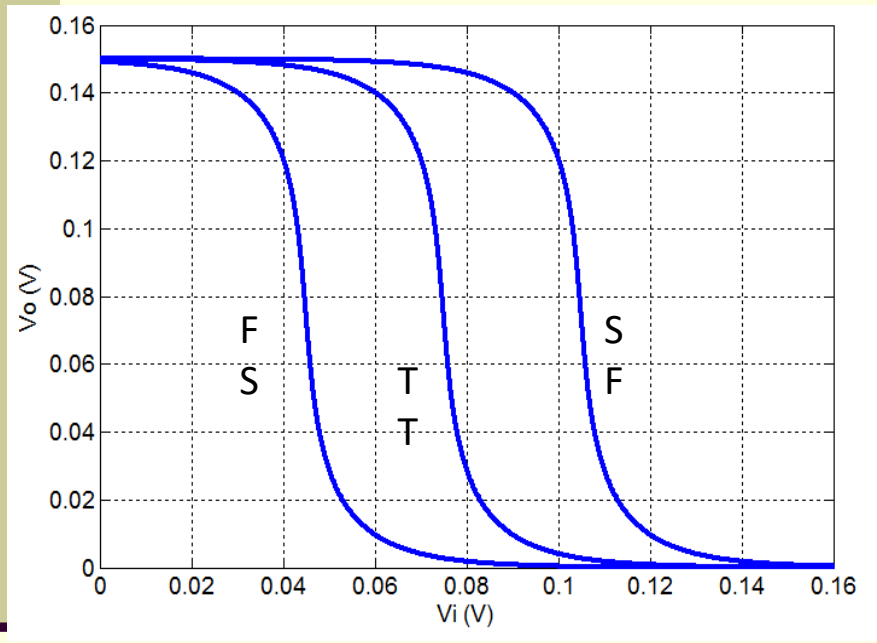
Minimum supply voltage for unity gain versus n/p imbalance (n_N=n_P=1)

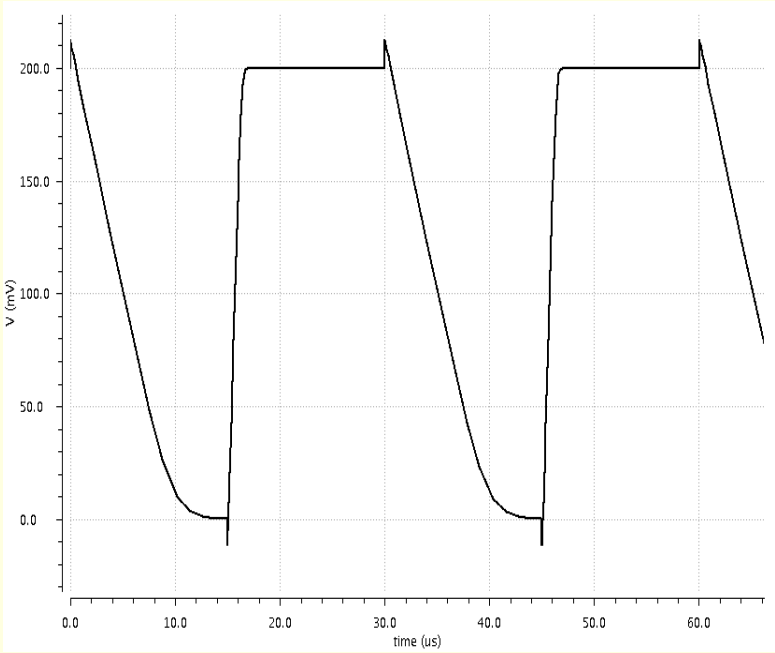
[1]C. G-Montoro, Marcio C. Schneider, T. D Fernandes, and D. G. Alves N, LASCAS 2024

BODY-BIAS COMPENSATION-1

The VTC of an inverter is affected by process parameters such as VT.

Large difference in rise and fall times due to PMOS/NMOS asymmetry.

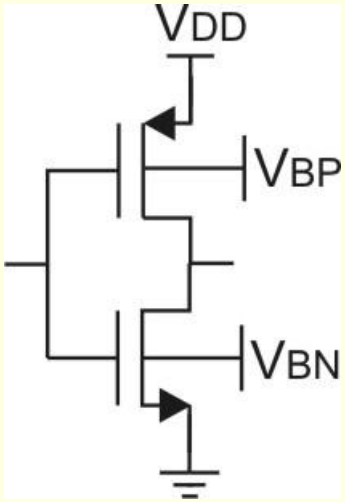




TT – Typical NMOS and PMOS
FS – Fast NMOS, Slow PMOS
SF – Slow NMOS, Fast PMOS

This asymmetry represents a waste of energy since the maximum operating frequency is given by the sum of the rise and fall times.

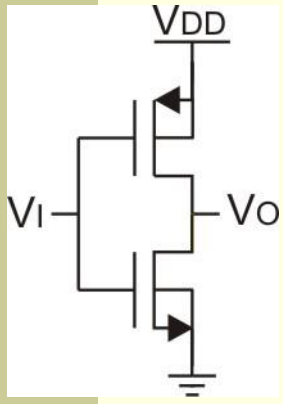
BODY-BIAS COMPENSATION-2



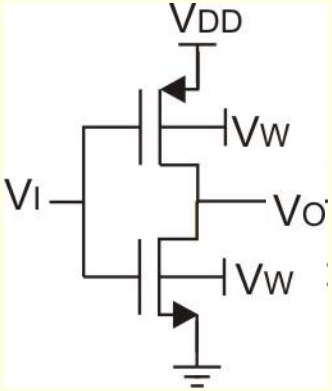
Common Techniques:
Reverse Body Bias (RBB) – $V_{BP} > V_{DD}$, $V_{BN} < GND$
Forward Body Bias (FBB) – $V_{BP} < V_{DD}$, $V_{BN} > GND$

RBB – difficult to generate bias voltages
FBB – is limited to sub-1V since two parasitic diodes are forward biased. Latch-up must be avoided.

BODY-BIAS COMPENSATION-3

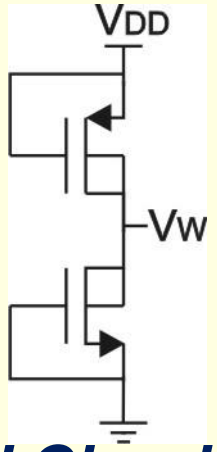


Standard inverter

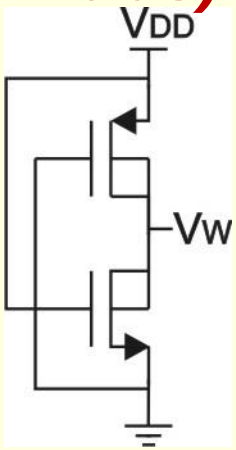


BB inverter

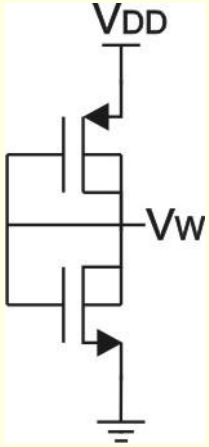
Vw generators (forward body bias)



"Off" Circuit Bryant [2001]



"On" Circuit

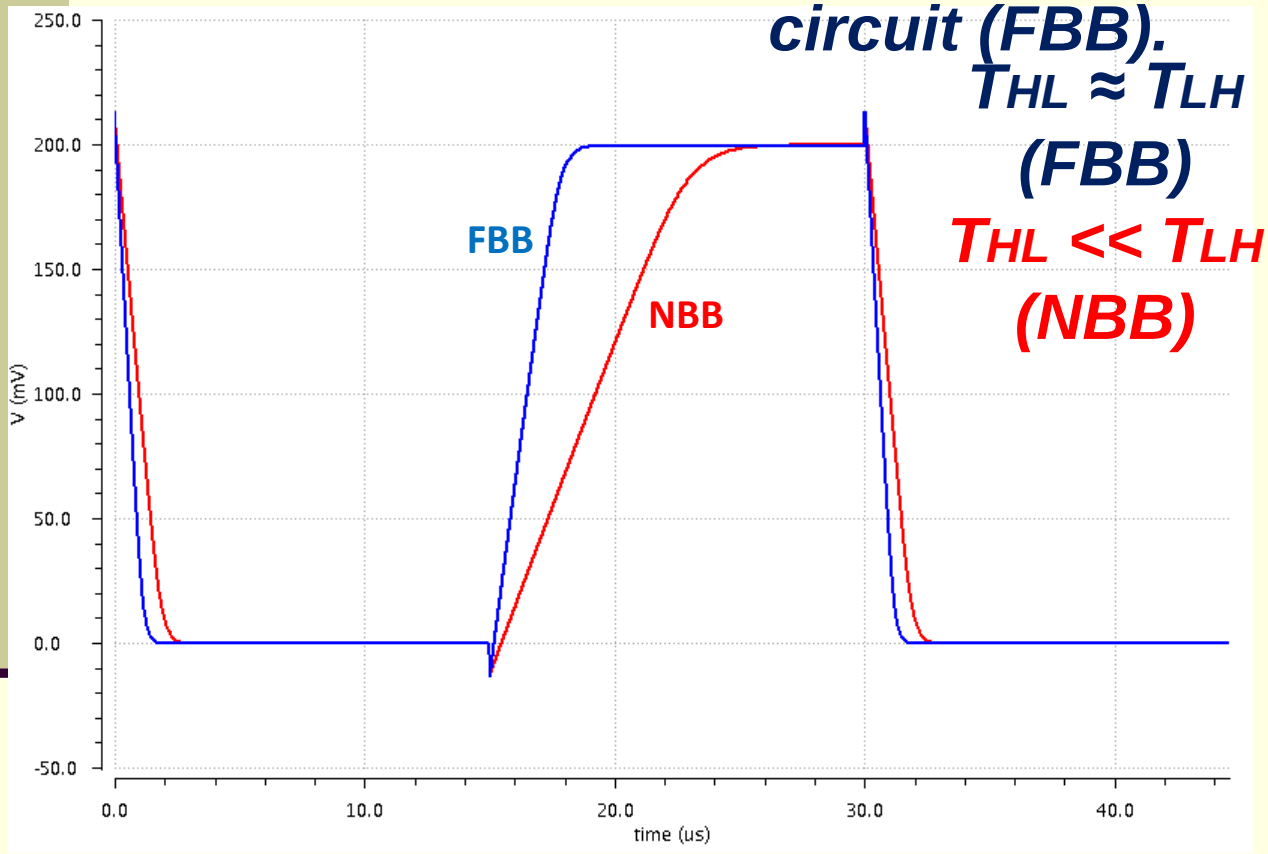


"Midway" Circuit

$V_W \rightarrow$ results from equalization of NMOS and PMOS currents

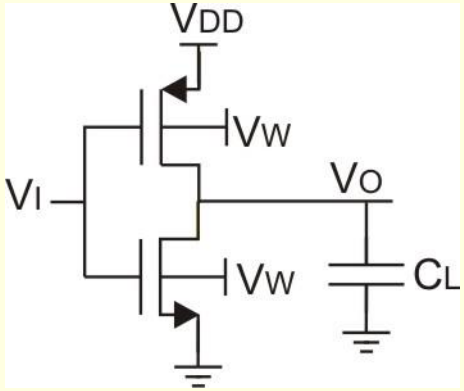
BODY-BIAS COMPENSATION-4

Inverter transient simulation without body bias (NBB) and with the "midway" compensation circuit (FBB).



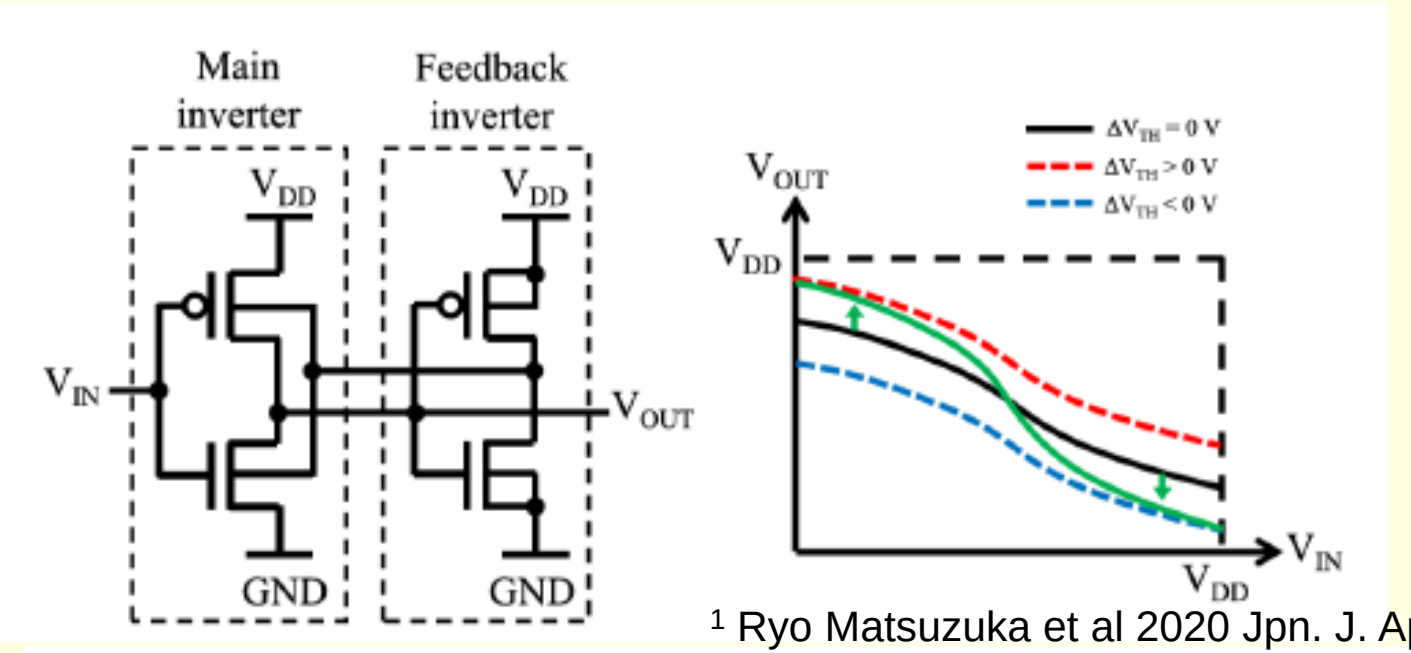
$T_{HL} \approx T_{LH}$ (FBB)

$T_{HL} << T_{LH}$ (NBB)

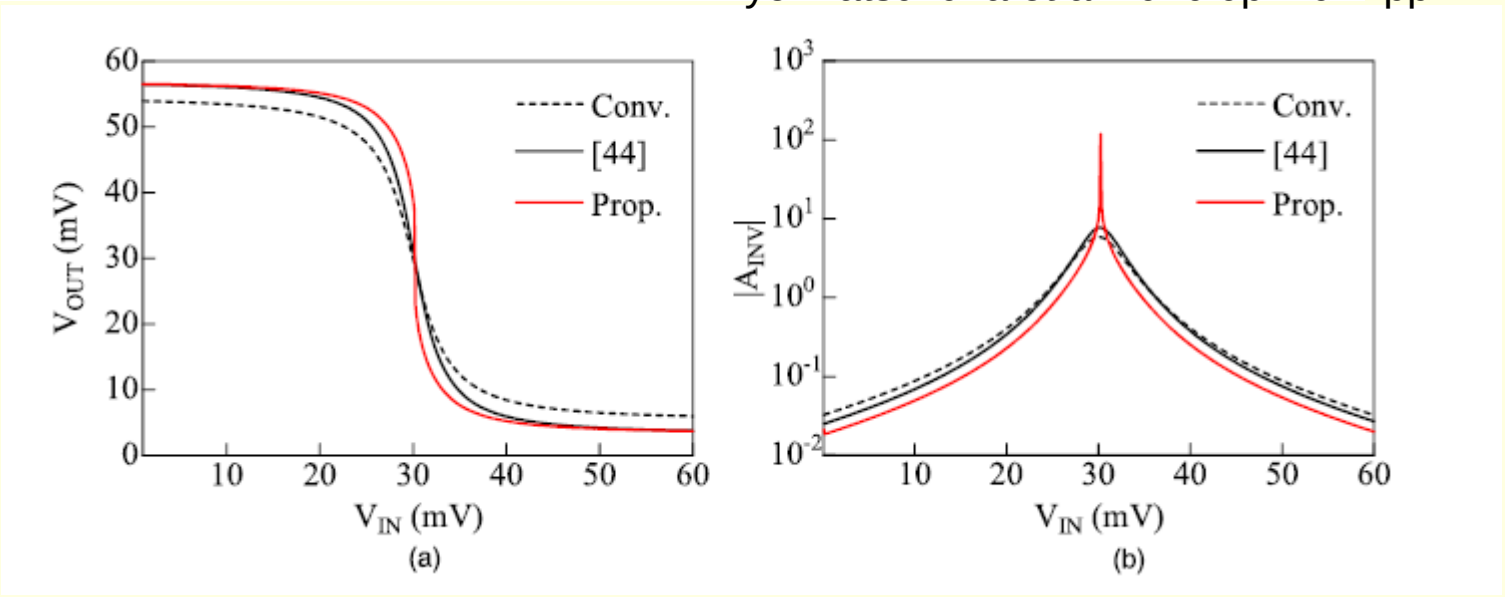


For FBB T_{HL} and T_{LH} are closer and faster than for NBB.

Gain-enhanced self-bias inverters[1]



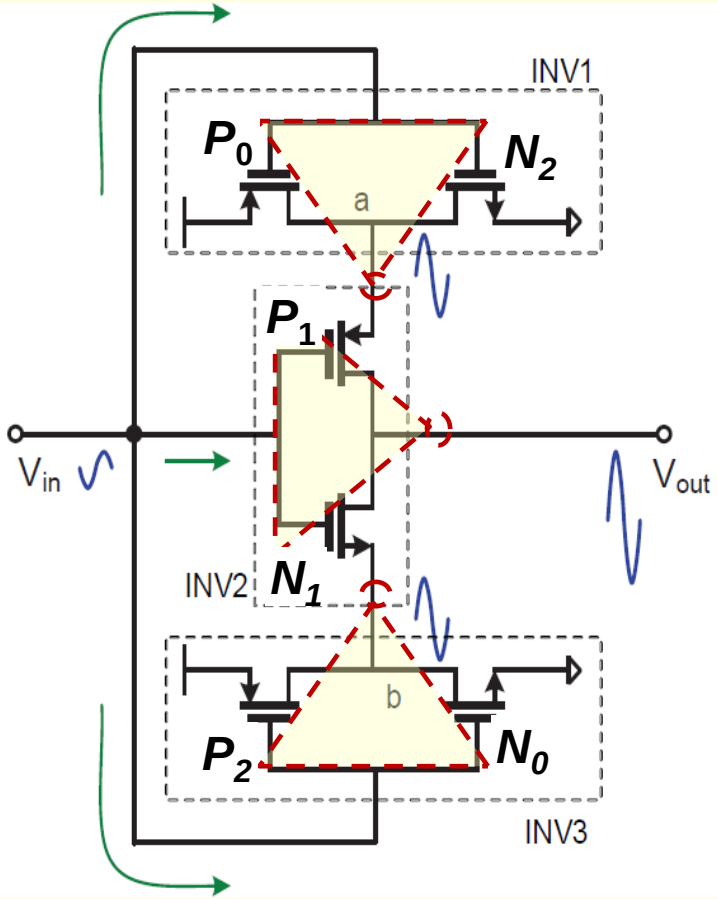
[1] Ryo Matsuzuka et al 2020 Jpn. J. Appl. Phys. 59



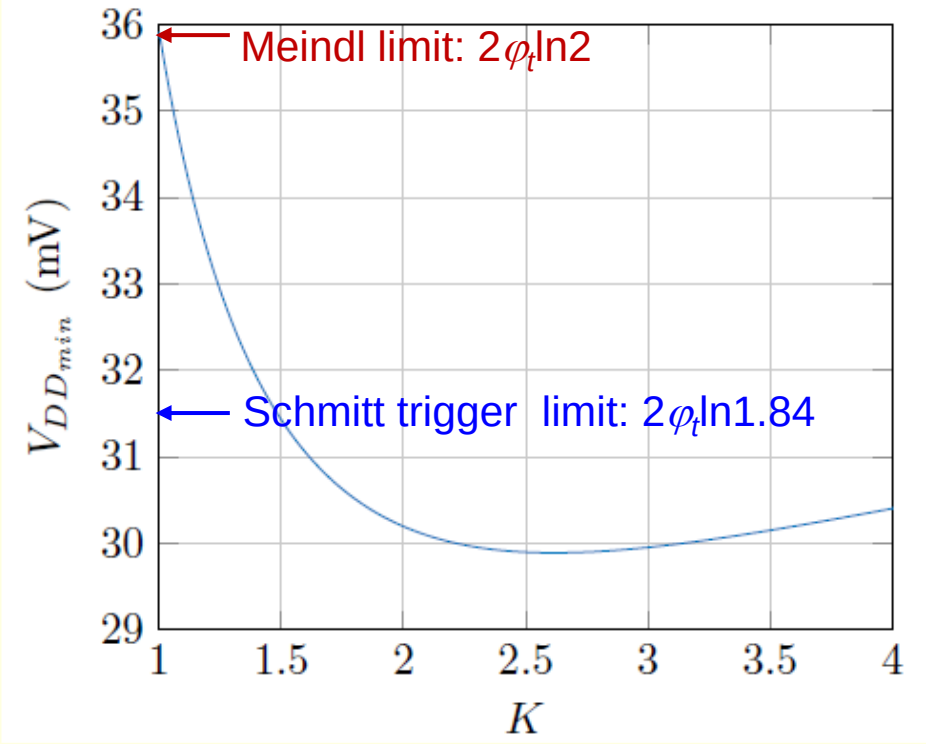
The Stacked-Inverter Gate (SIG)[1]

$$K = I_0/I_2 \text{ and } J = I_1/I_2$$

$N_i = P_i \qquad i = 0, 1, 2$



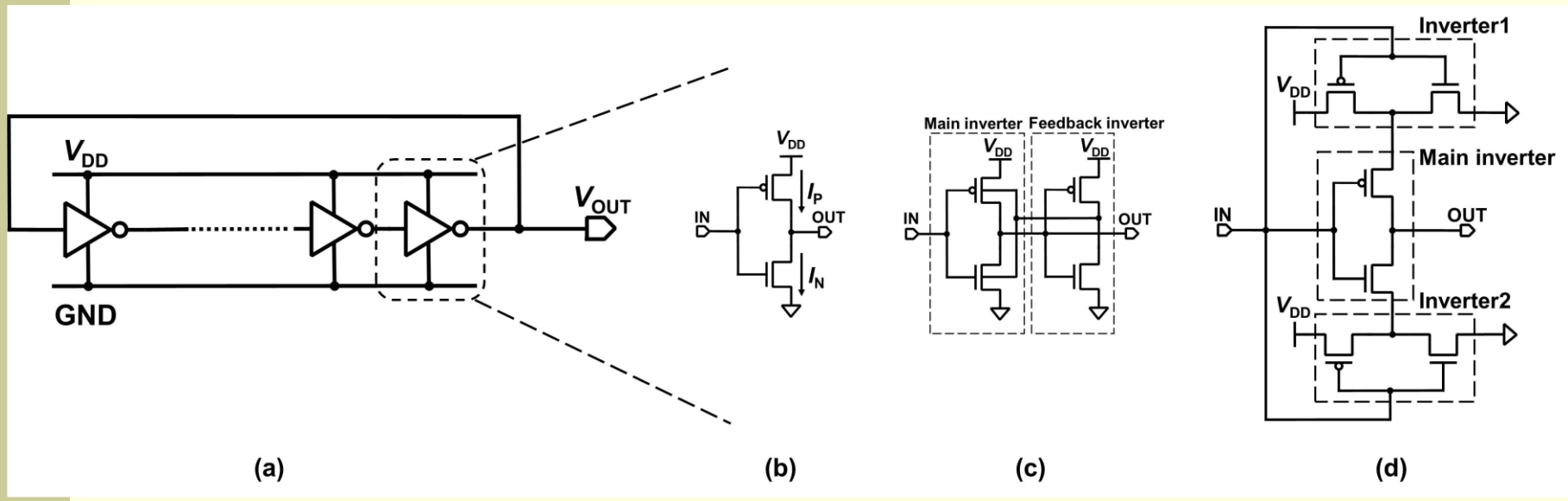
V_{DDmin} without positive feedback →
→ no hysteresis



SIG V_{DDmin} for unity gain versus K with $J = 1$

[1] Bose and Johnston ISCAS 2018

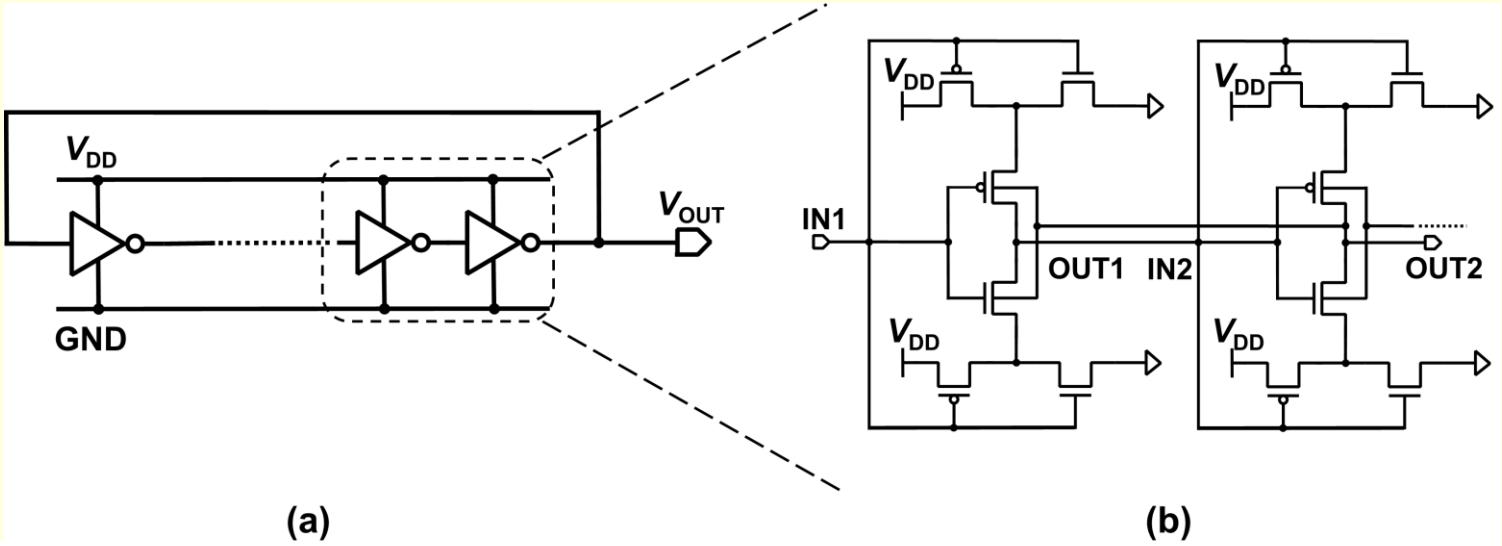
Combining techniques[1]-1

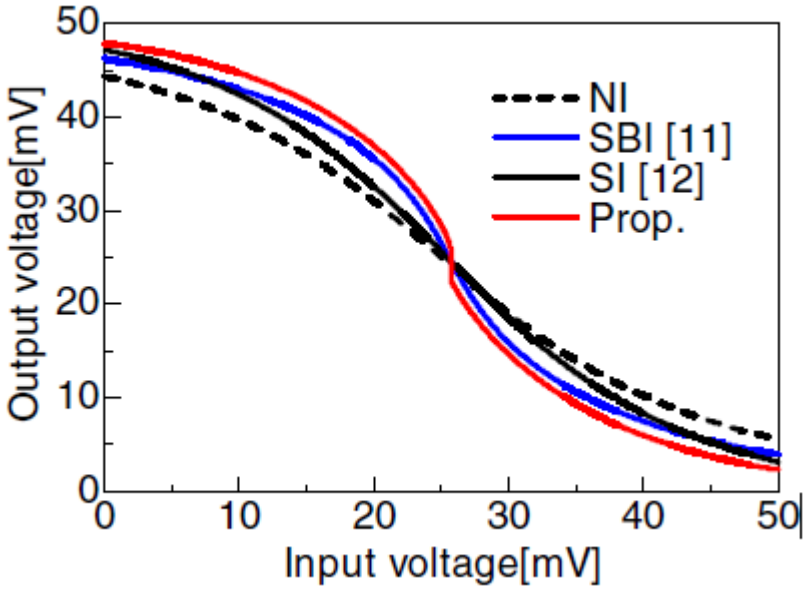


(a) ROSC, (b) normal inverter (NI), (c) self-bias inverter (SBI) and (d) stacked inverter (SI).

[1] M. Ahmed *et al. IEEE Access,* vol. 12, 2024

Combining techniques[2]-2

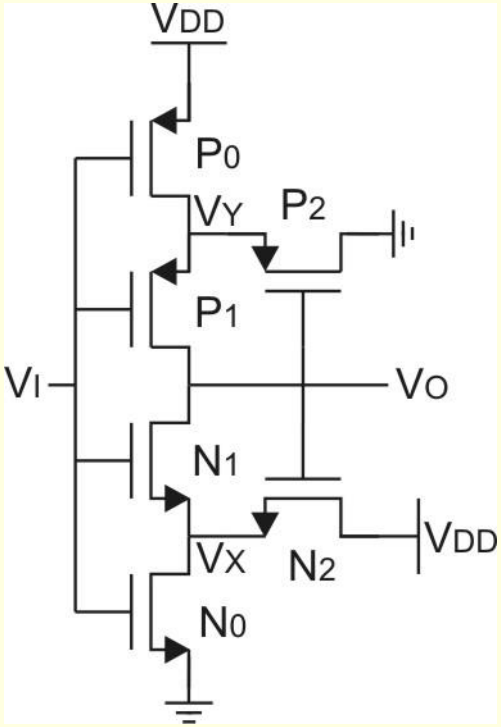




(NI) normal inverter
(SBI) self-bias inverter
(SI) stacked inverter

[2] M. Nishi *et al.* in 2020 NEWCAS

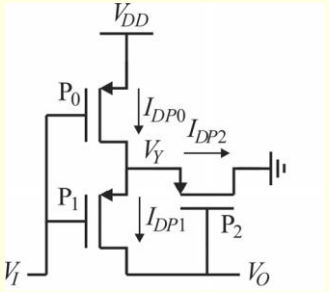
The CMOS Schmitt trigger

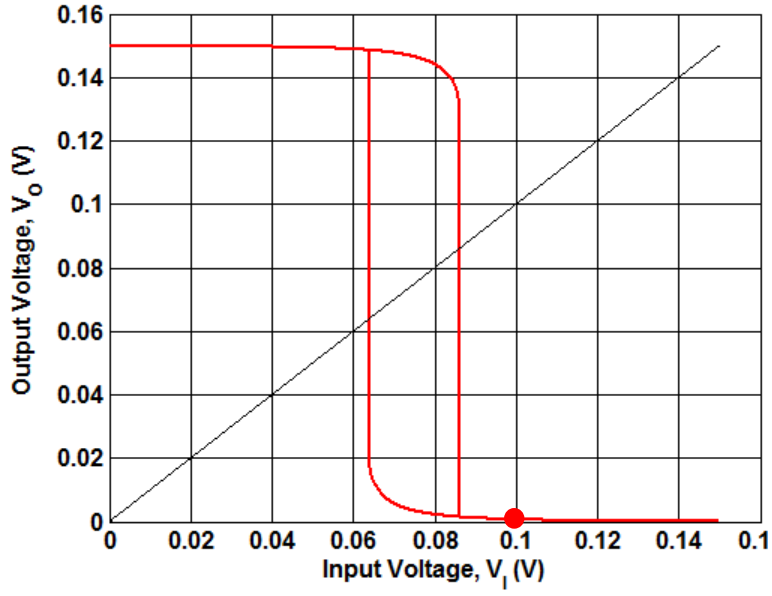


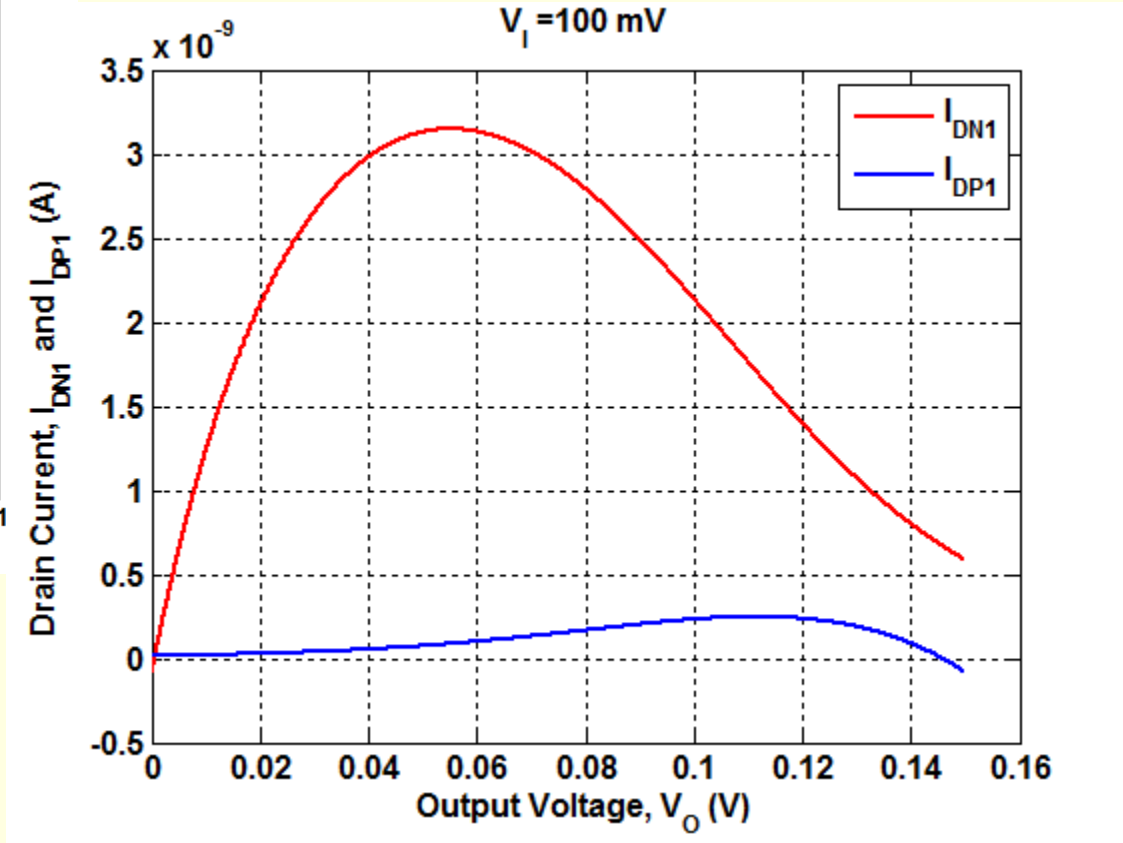
- *2 internal nodes (VX and VY)*
- *Feedback transistors (P2/N2) controlled by the output*
- *Hysteresis dependent on VDD & relative transistor strength*
- *Modeled in strong inversion but only recently (2017) in weak inversion*
- *For symmetric operation, corresponding NMOS and PMOS MOSFETs have the same current capability.*

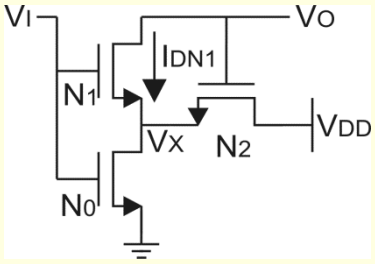
6 transistors (6T) Schmitt Trigger

Schmitt Trigger operation 1

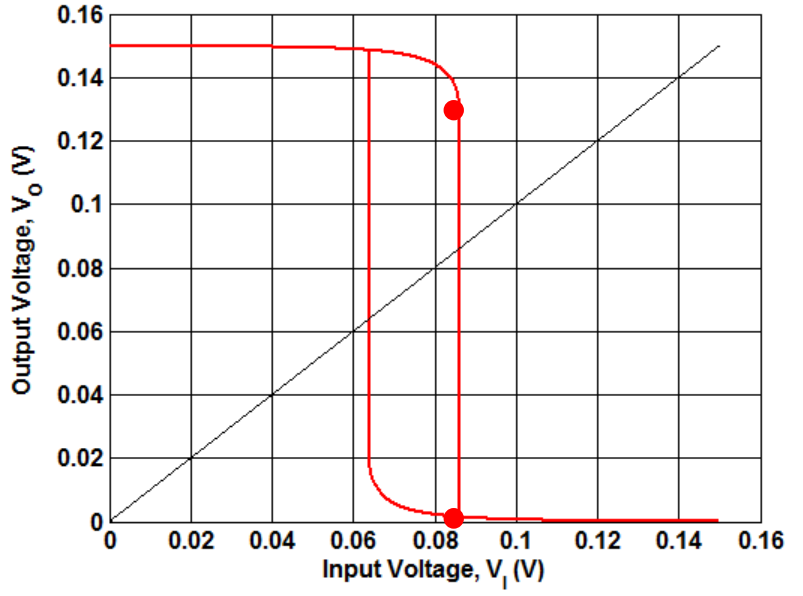


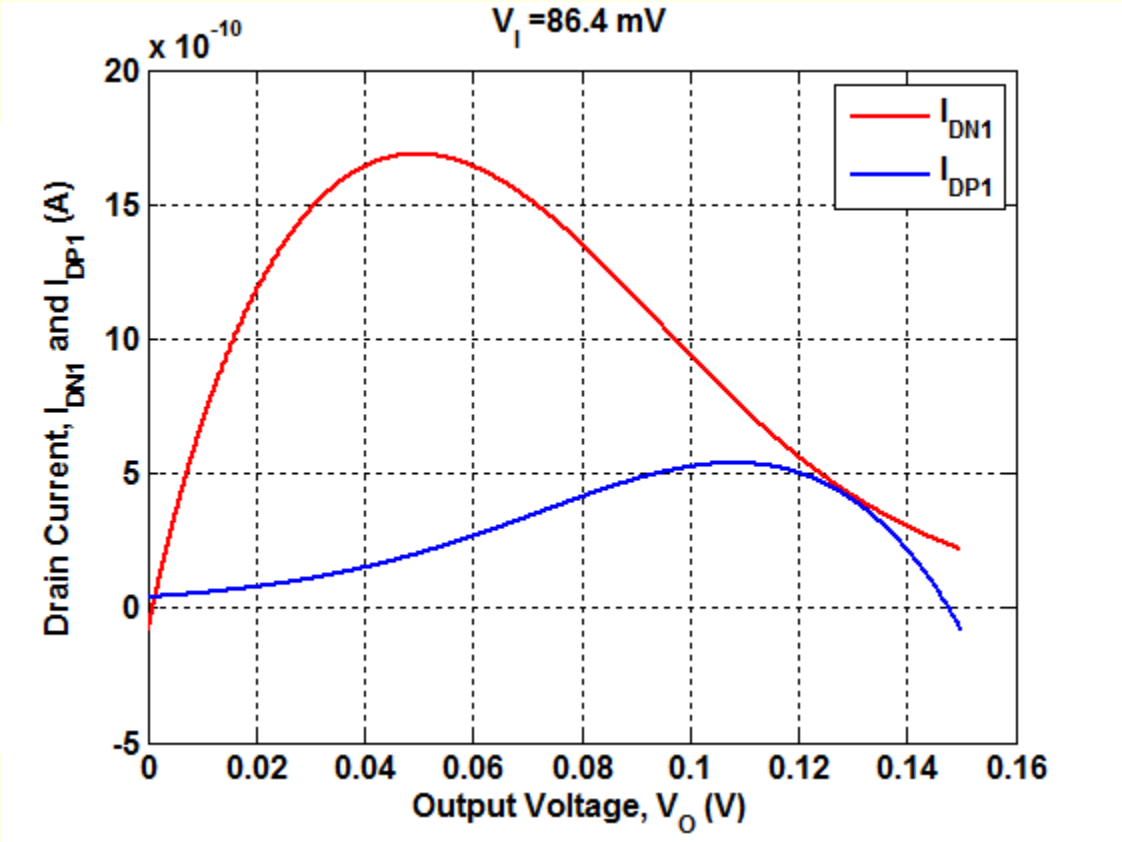




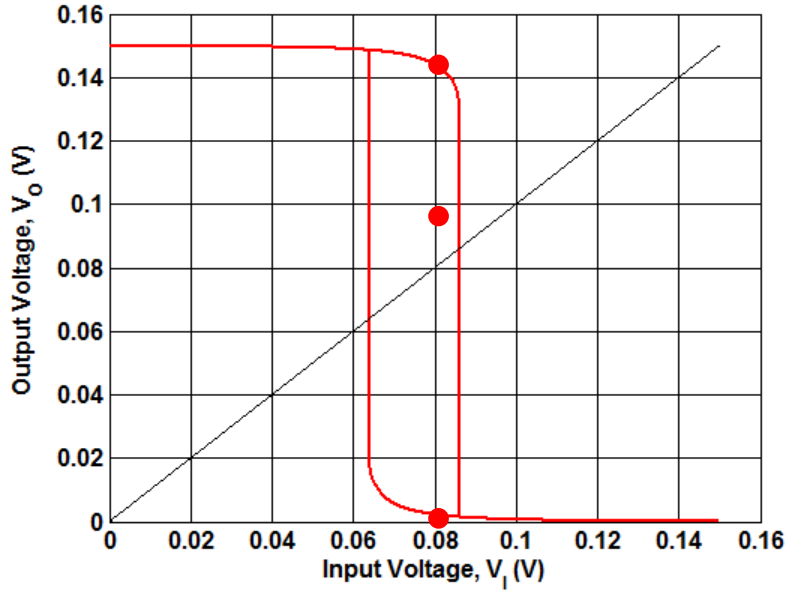


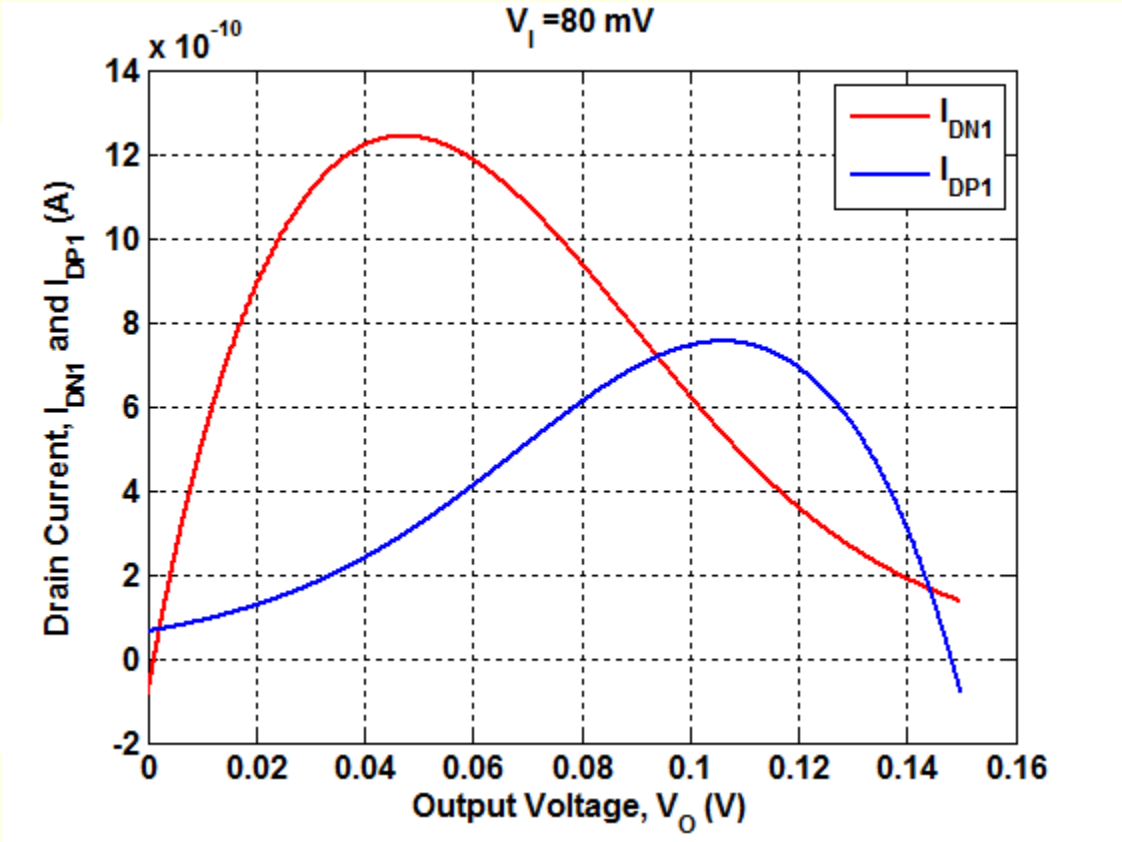
Schmitt Trigger operation 2



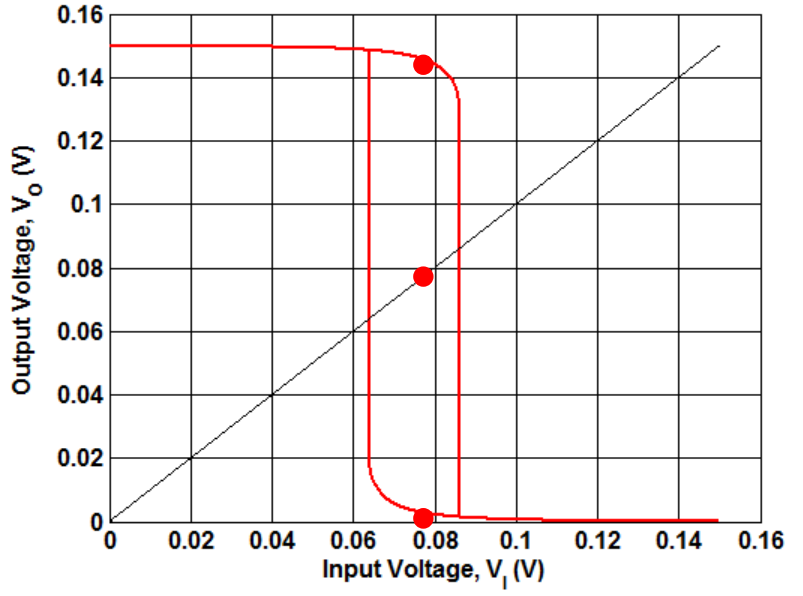


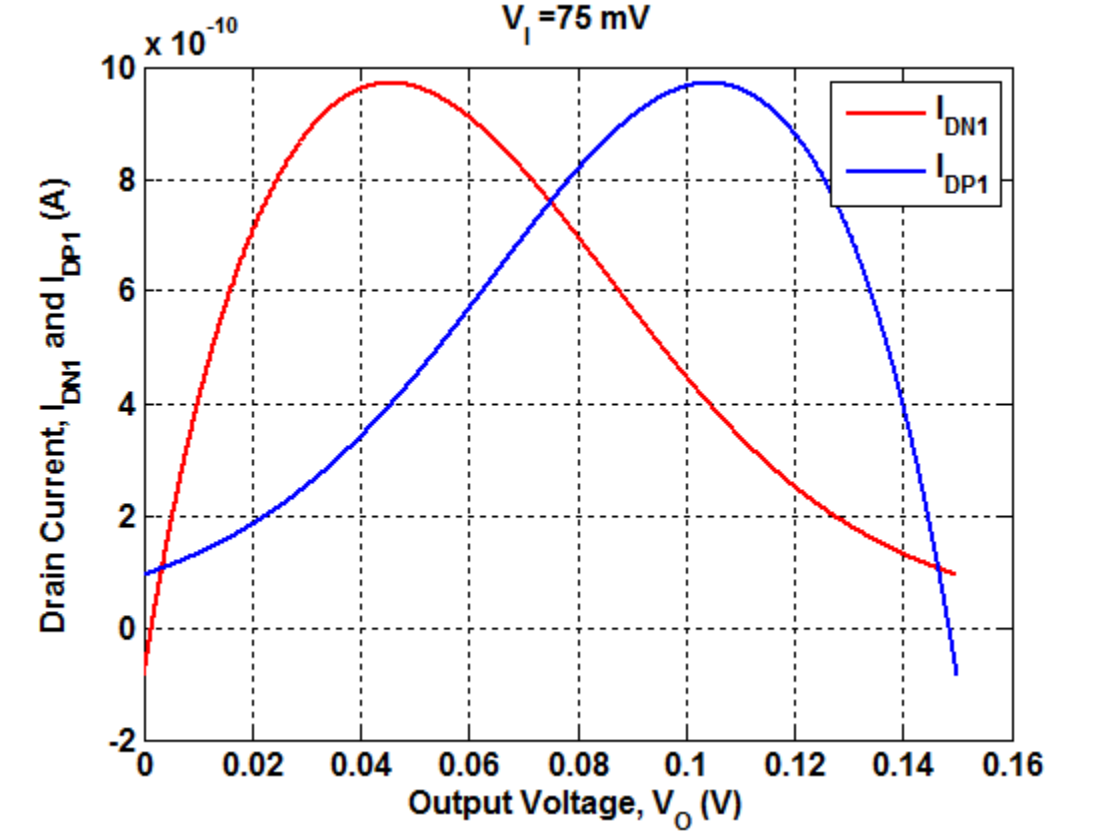
Schmitt Trigger operation 3



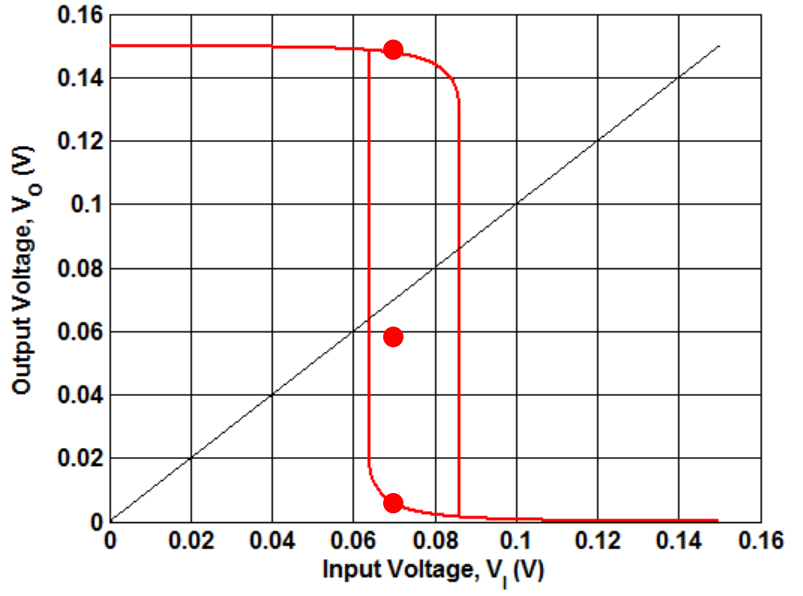


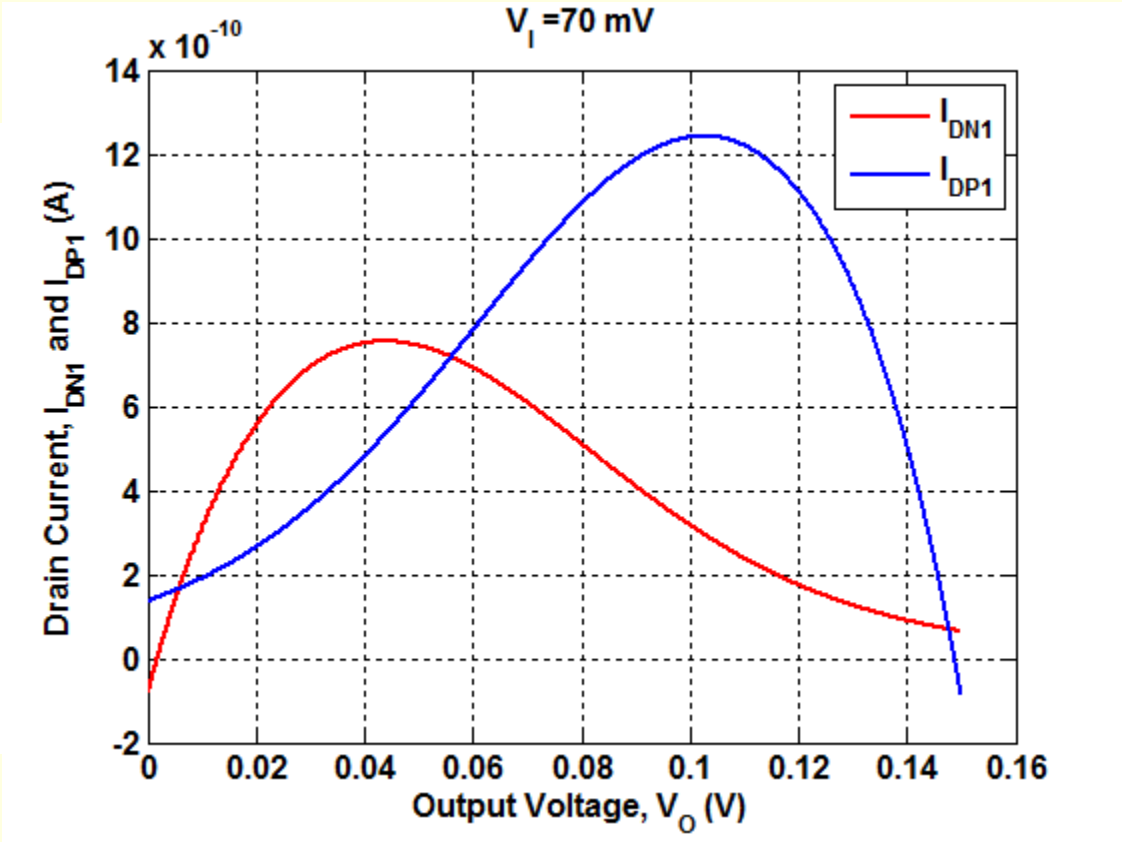
Schmitt Trigger operation 4



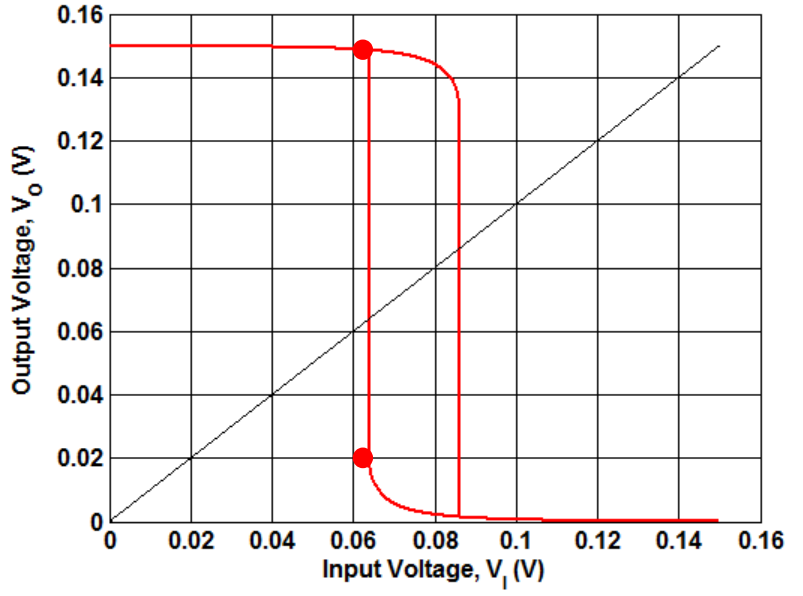


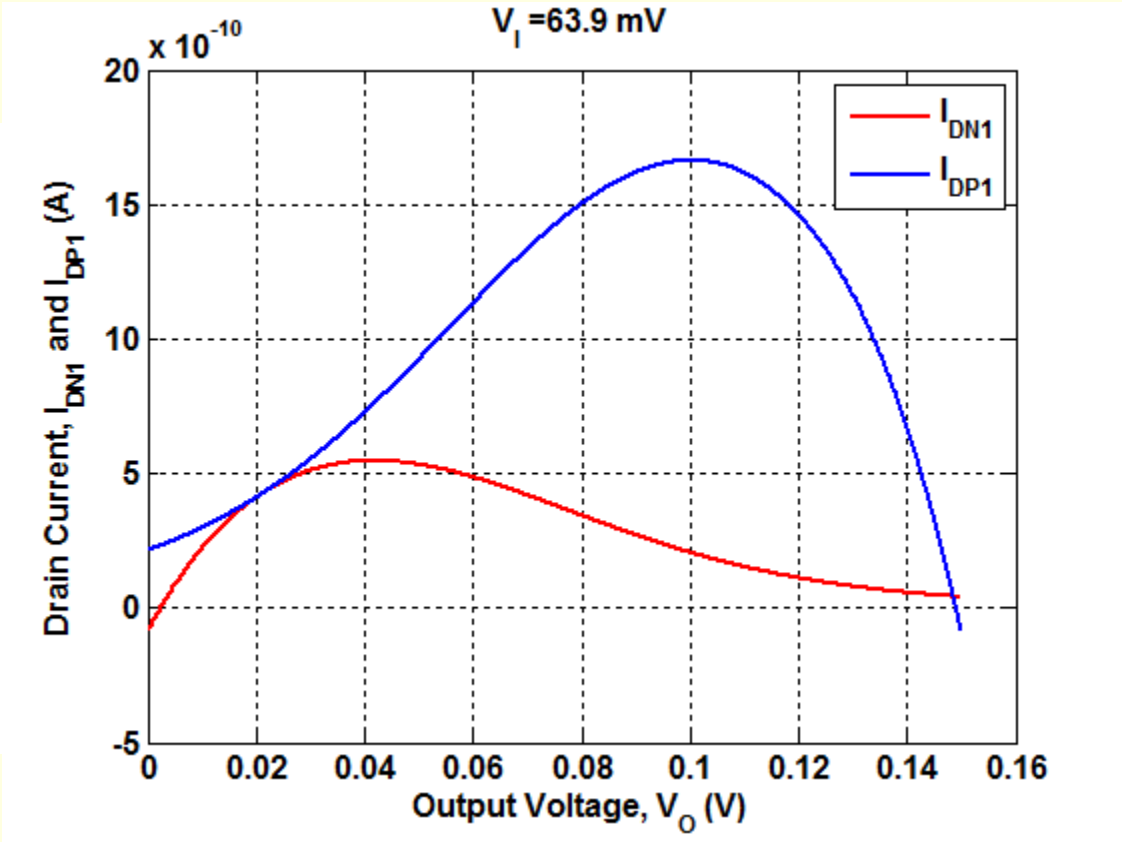
Schmitt Trigger operation 5



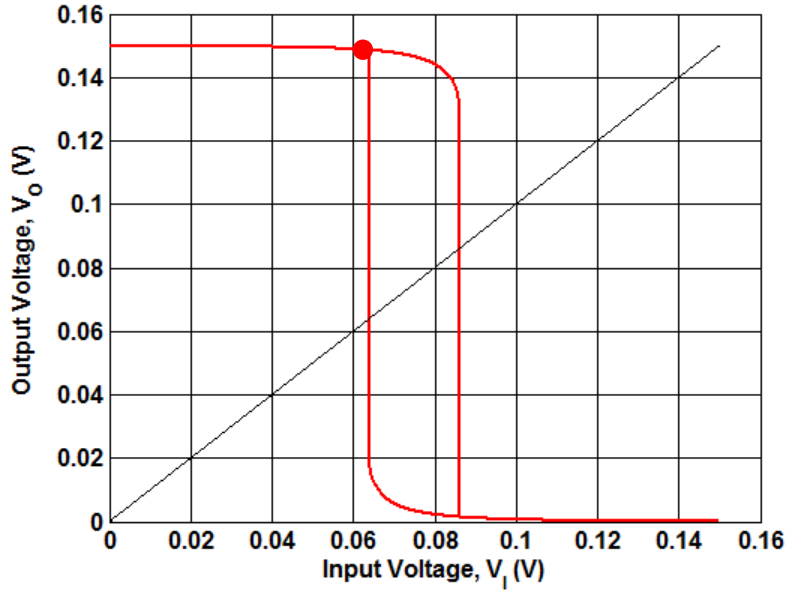


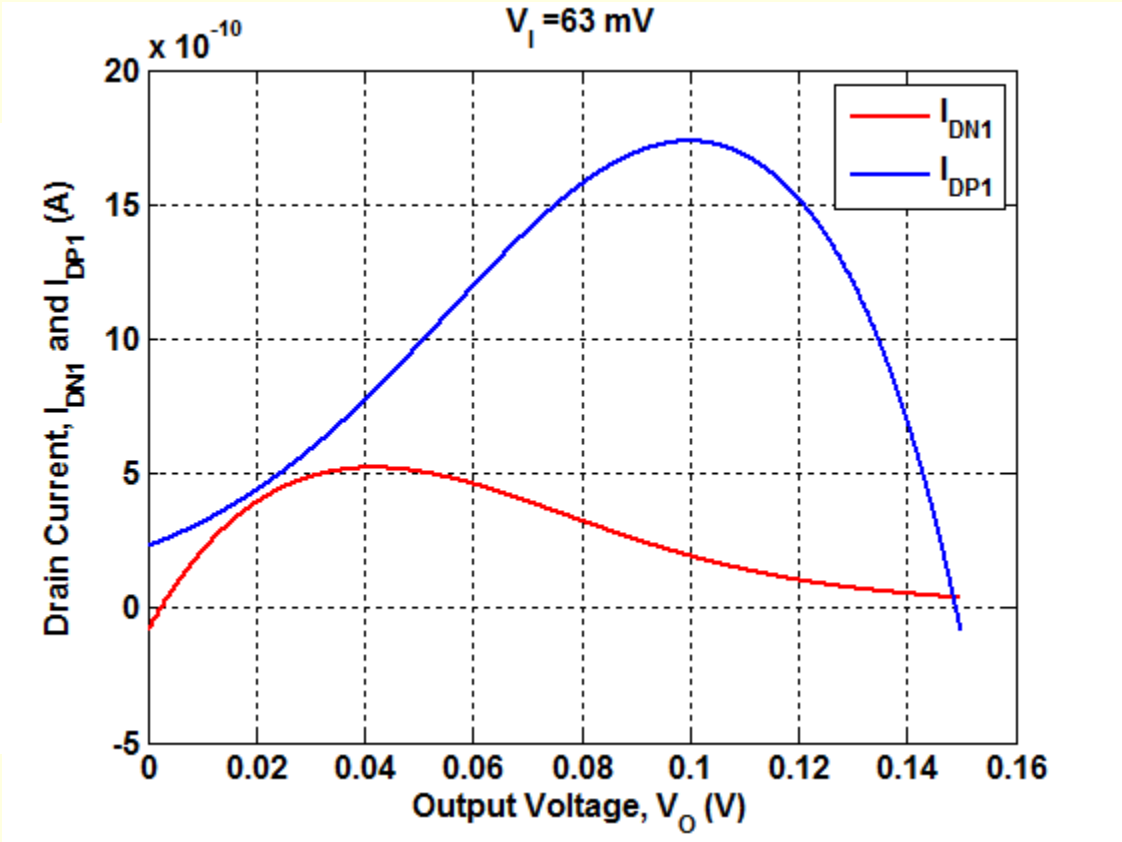
Schmitt Trigger operation 6



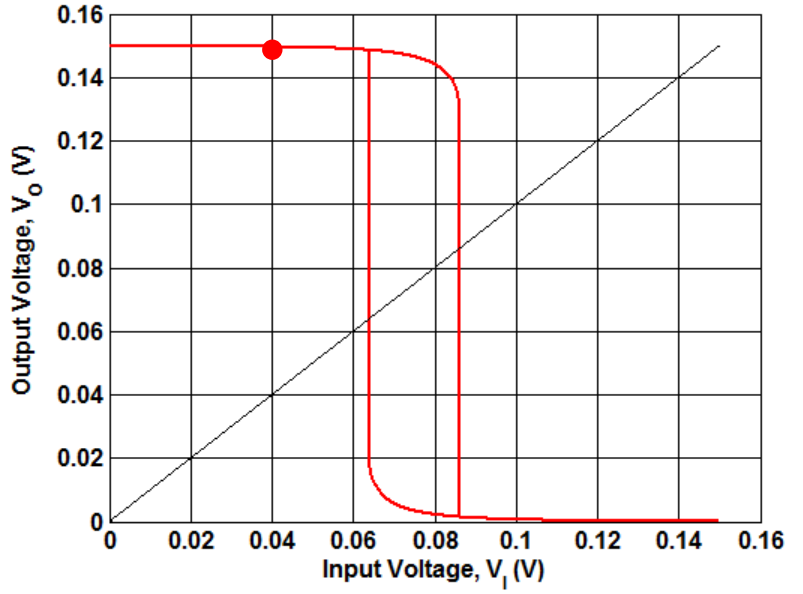


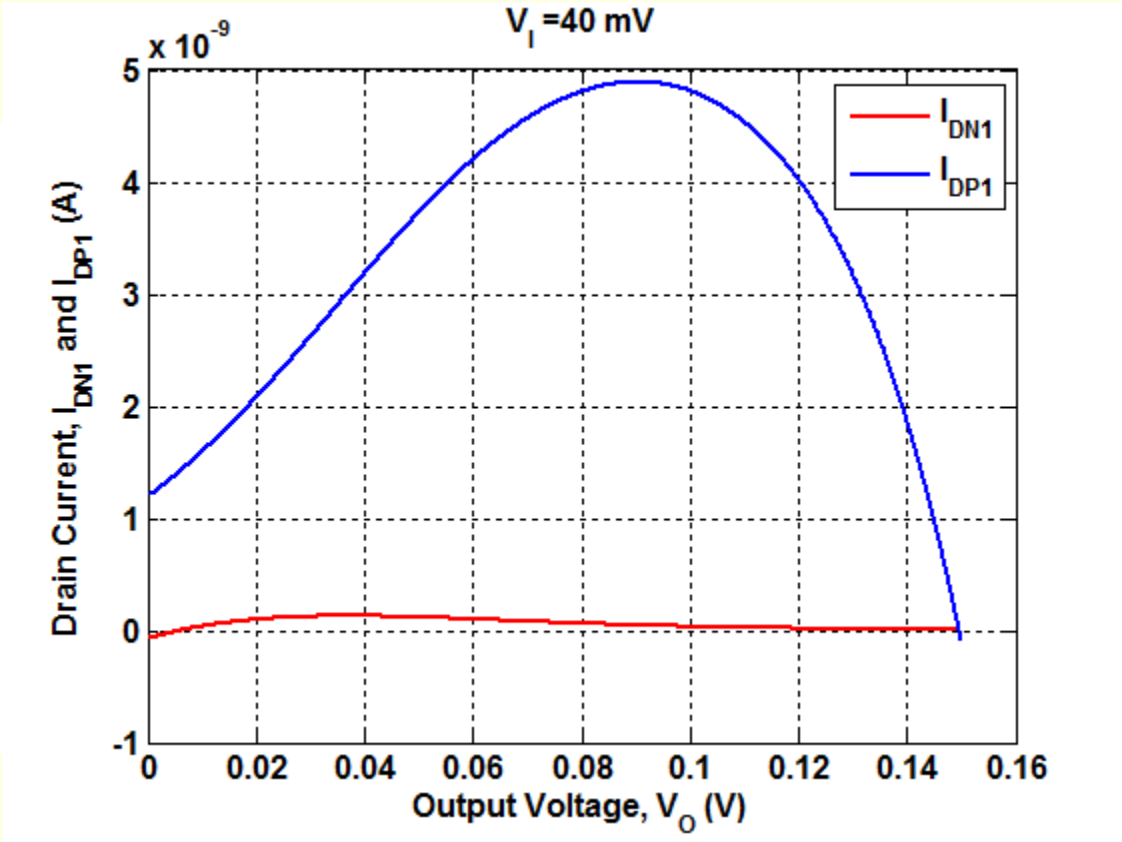
Schmitt Trigger operation 7



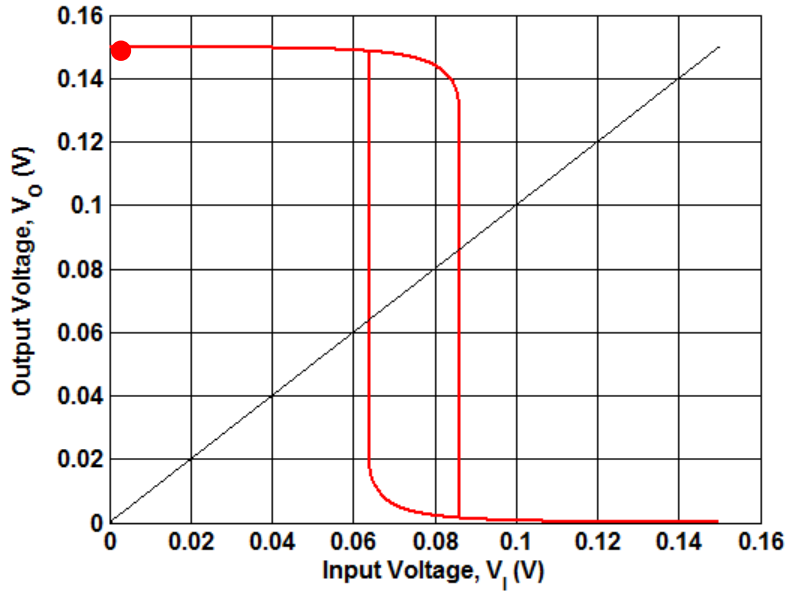


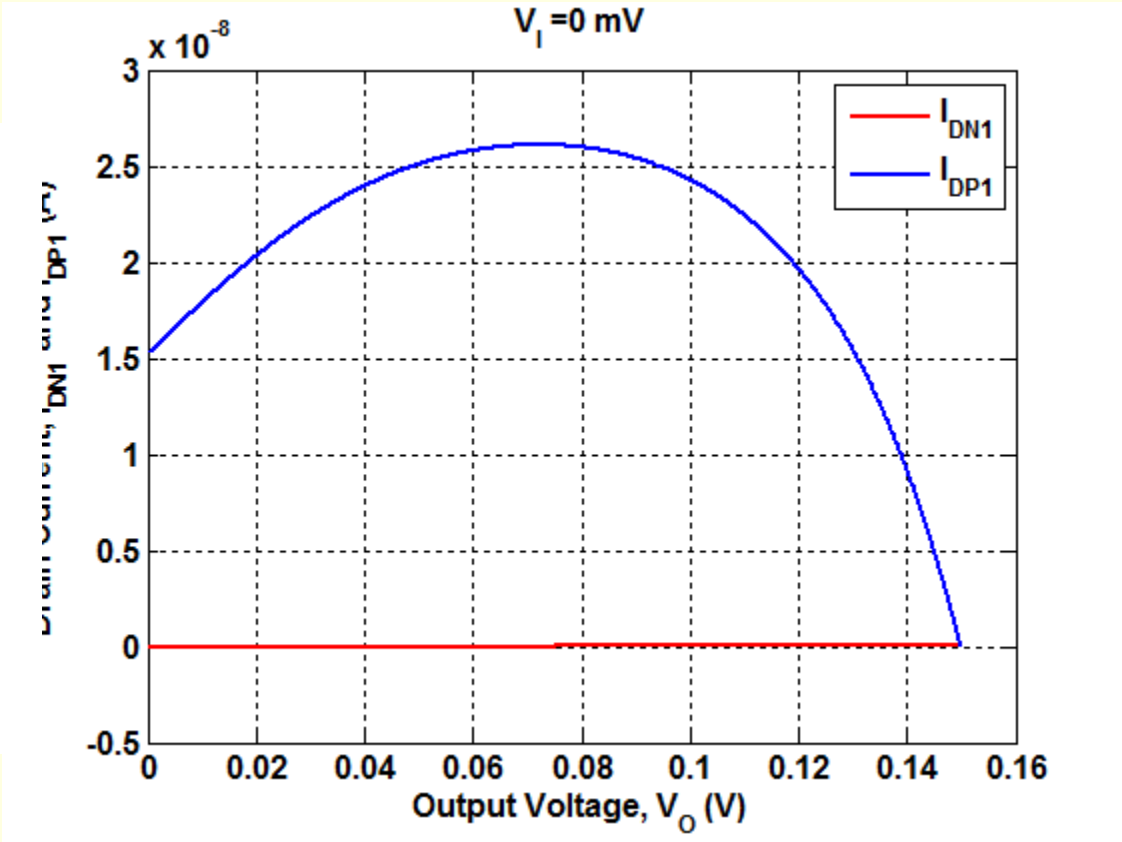
Schmitt Trigger operation 8





Schmitt Trigger operation 9

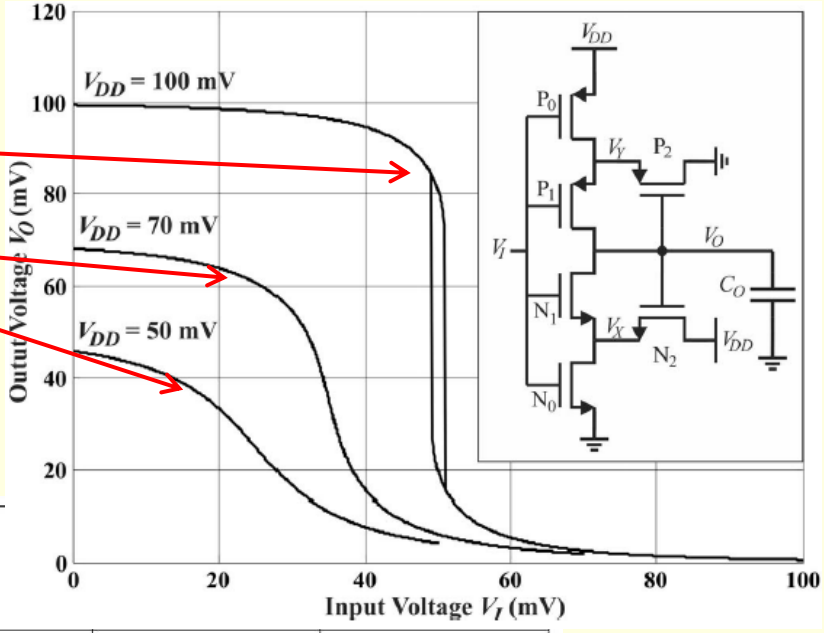


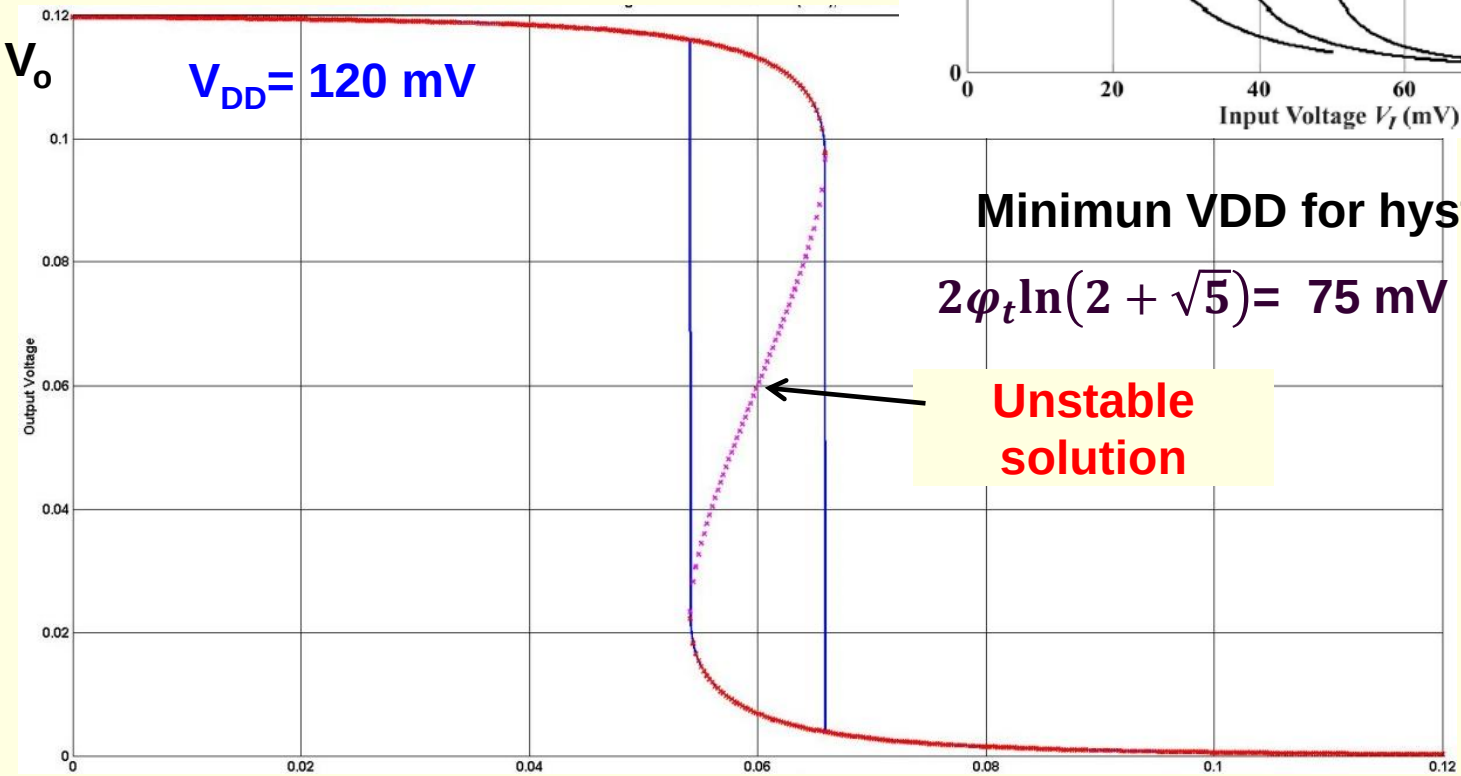


The 6-T Schmitt trigger

Hysteresis mode

Amplifier mode





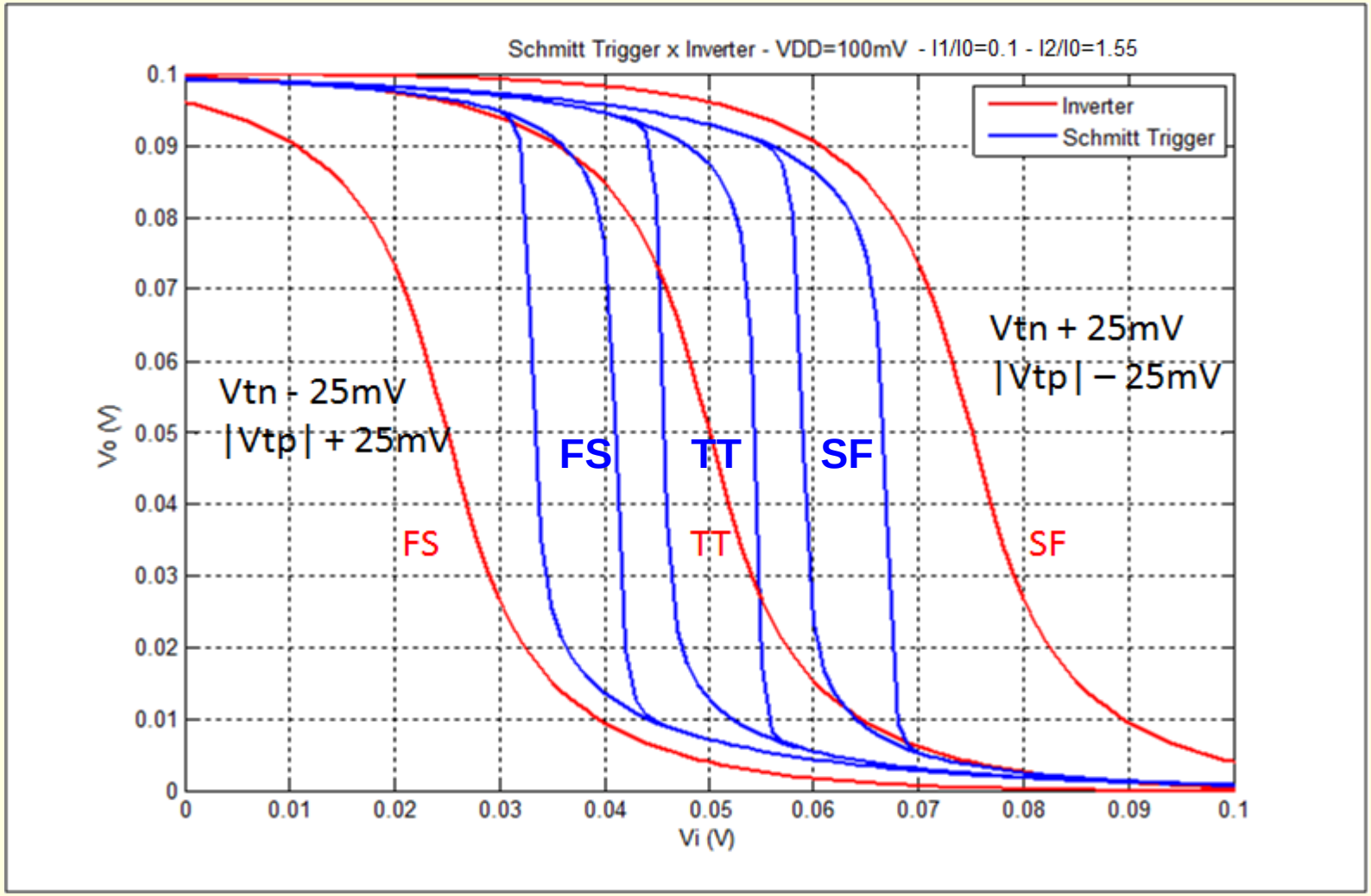
Minimun VDD for hysteresis

$2\varphi_t \ln(2+\sqrt{5})$= 75 mV at 300 K

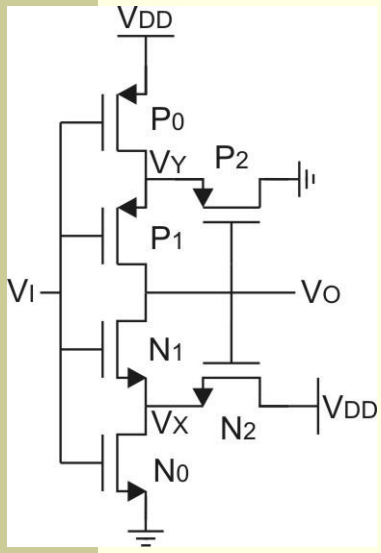
Unstable solution

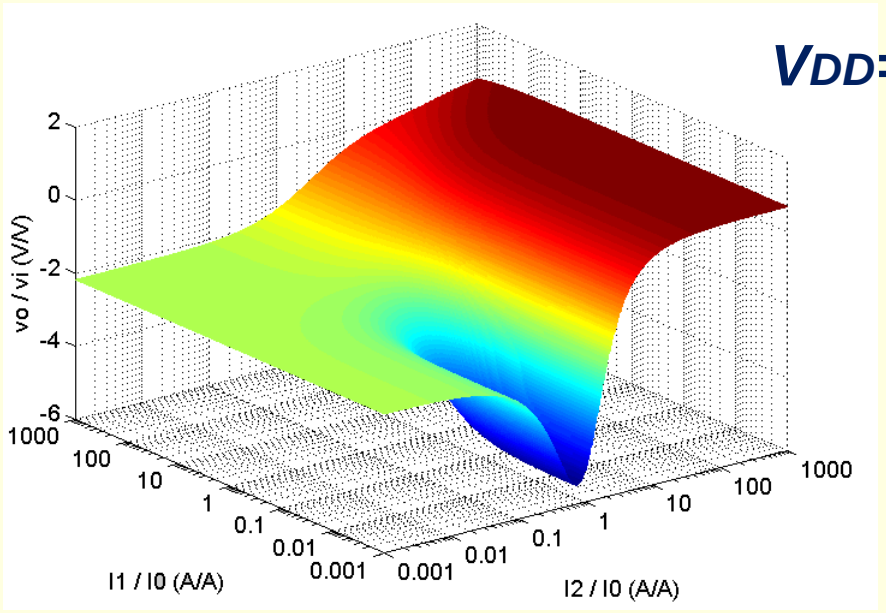
ST sensitivity to p/n imbalance

ST inverter is less sensitive to process parameters (V_T) spreading than the standard inverter.



SCHMITT TRIGGER as an amplifier





VDD=60mV

VDD (mV)	I2/I0 opt (A/A)
100	1.5479
90	1.3110
80	1.0973
75	0.9987
70	0.9051
60	0.7324
50	0.5774
40	0.4384
36	0.3869
31	0.3333

$$\left.\frac{I_1}{I_0}\right|_{OPTIMUM} = 0$$

$$\left.\frac{I_2}{I_0}\right|_{OPTIMUM} = \frac{\sqrt{1+e^{\frac{V_{DD}}{2\phi_t}}-e^{-\frac{V_{DD}}{2\phi_t}}}-1}{1+e^{-\frac{V_{DD}}{2\phi_t}}}$$

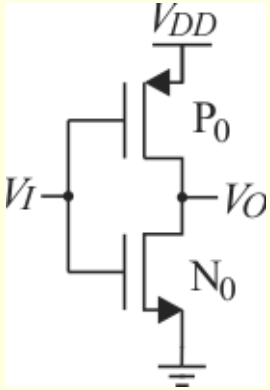
Result in highest possible gain for a given VDD

$I_{O,1,2}$ is the current strength of $N_{0,1,2}$ and $P_{0,1,2}$

The ST as an ULV Logic Inverter-1

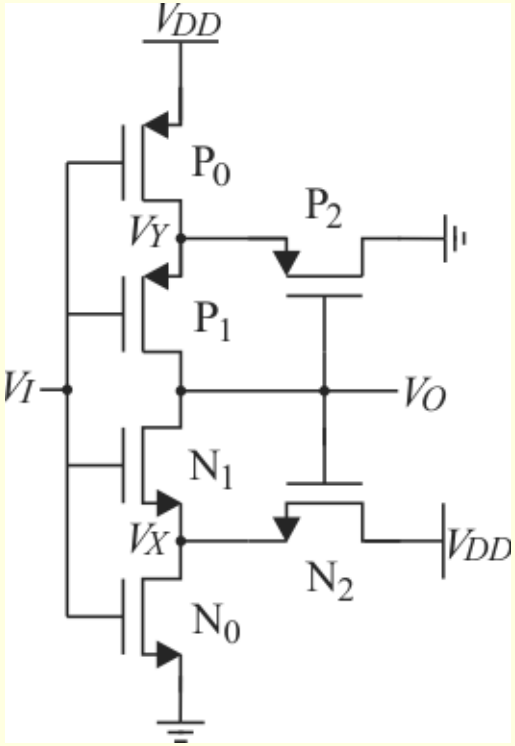
Conventional Inverter x Schmitt trigger

The conventional inverter is the ST with $I_2 = 0$.



$$V_{DD\min} = 2\phi_t \cdot \ln(2) = 35.9\ \text{mV, at 300K}$$

Swanson & Meindl 1972

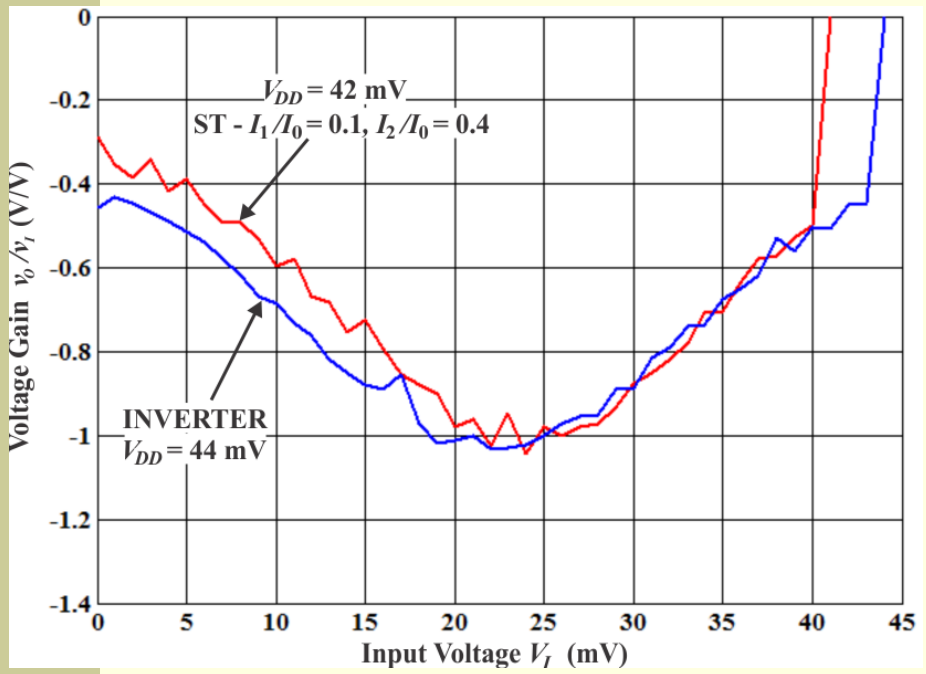


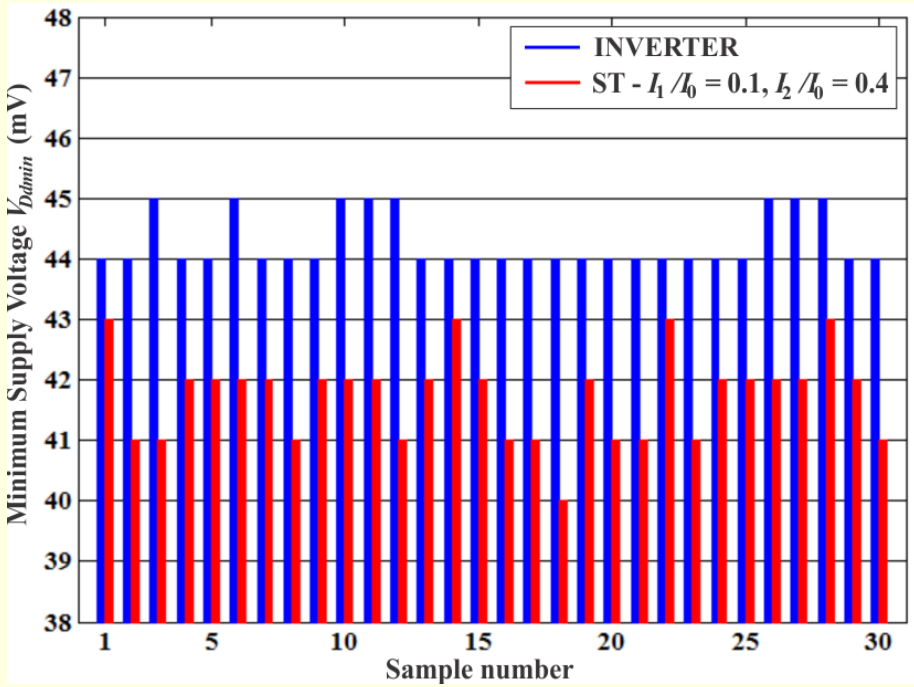
$$V_{DD\min} = 2\phi_t \cdot \ln\left(\frac{8+\sqrt{73}}{9}\right) = 31.5\ \text{mV, at 300K}$$

Pasini et al 2017

The ST as an ULV Logic Inverter-2

Conventional Inverter x Schmitt trigger – Experimental Results

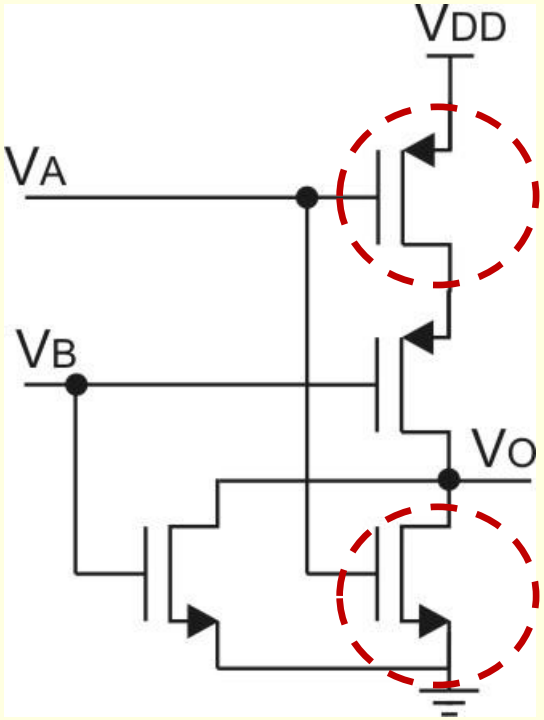




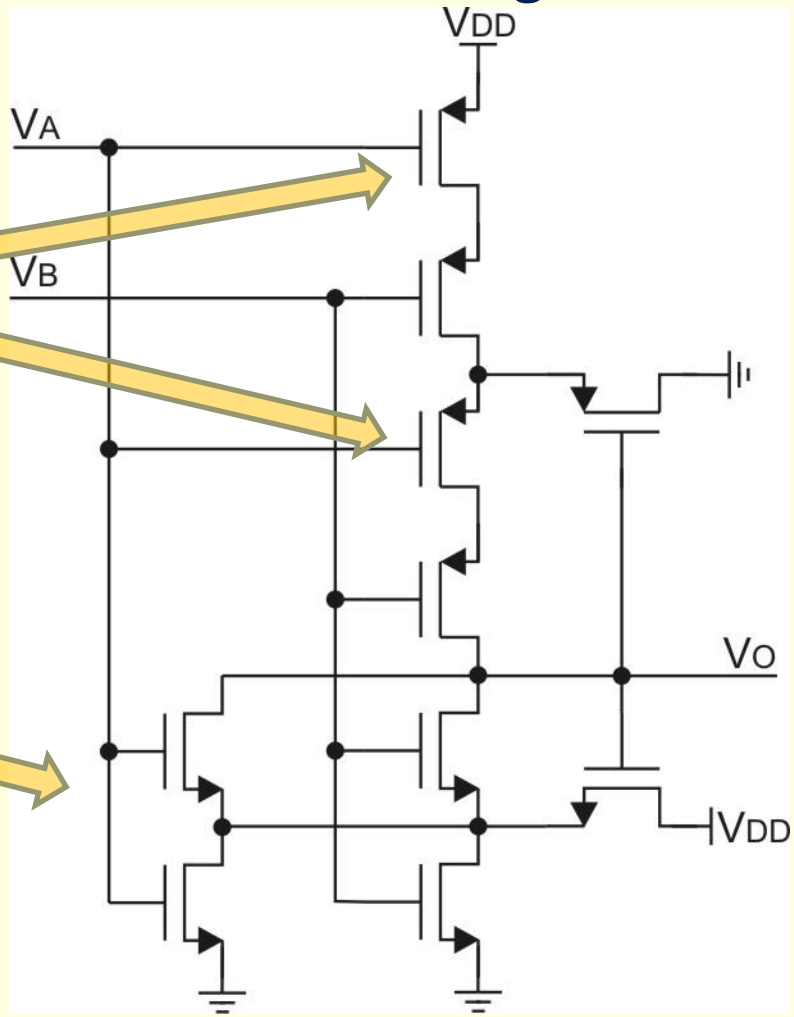
Voltage gain transfer

6-T Schmitt trigger logic

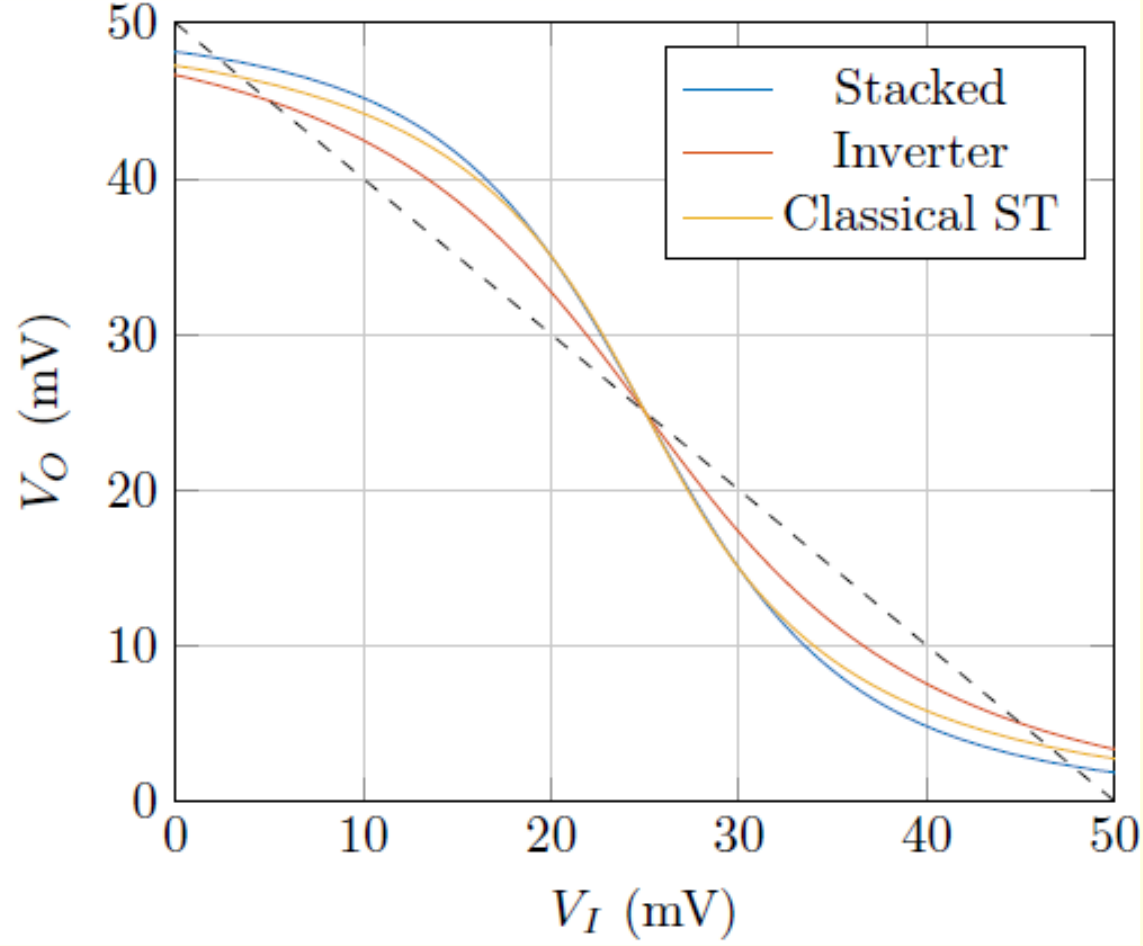
NOR gate



ST-NOR gate

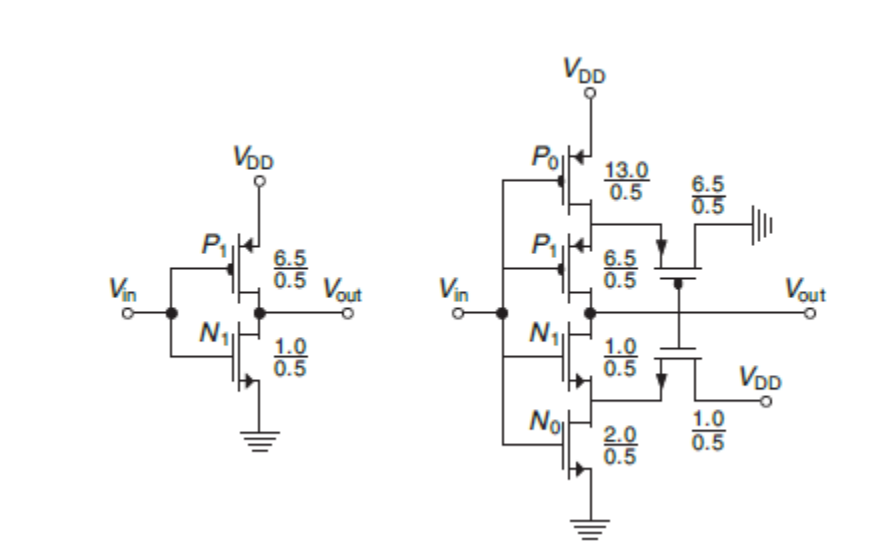


Inverter, SIG, and standard ST

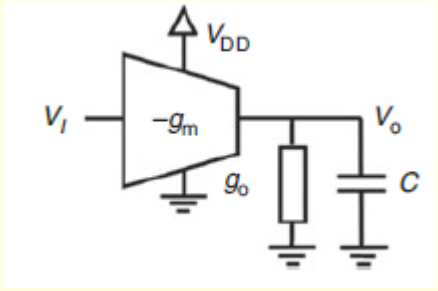


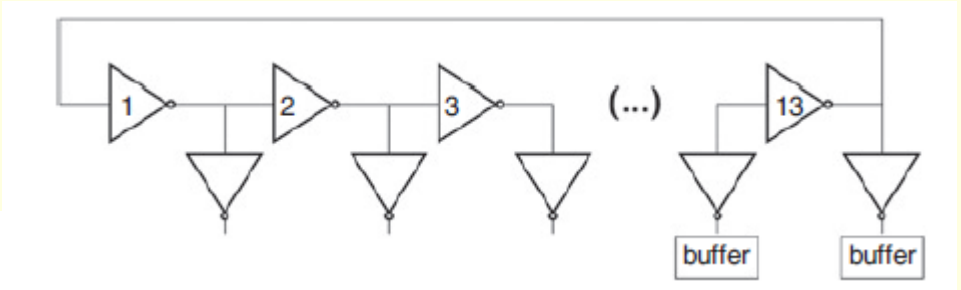
|Voltage gain|: Stacked Inverter >Standard ST>Inverter

Ultra-low-voltage CMOS ring oscillators-1



W/L PMOS and NMOS transistors to balance the current strengths of the transistors for a supply voltage of 60 mV. The four types of ROs : INV (standard inverters), INVB (standard inverters, substrates to the gate), ST (conventional ST), and STB (conventional ST, substrates to gates)

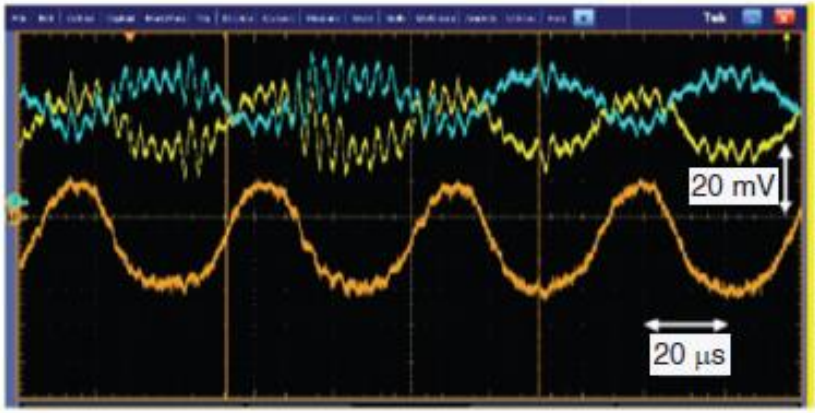




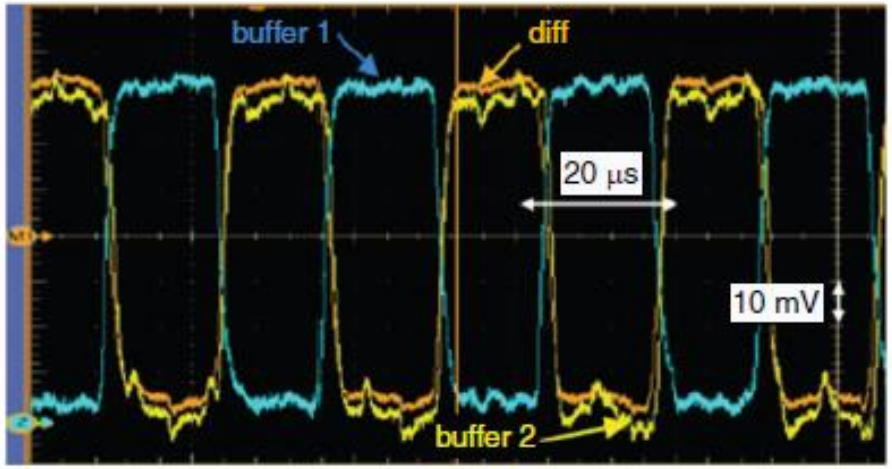
$$\omega_{osc} C / g_o = \tan(\pi/N)$$

$$g_m / g_o = \sqrt{1 + \tan^2(\pi/N)} \approx 1 + \frac{1}{2}(\pi/N)^2$$

Ultra-low-voltage CMOS ring oscillators[1]-2



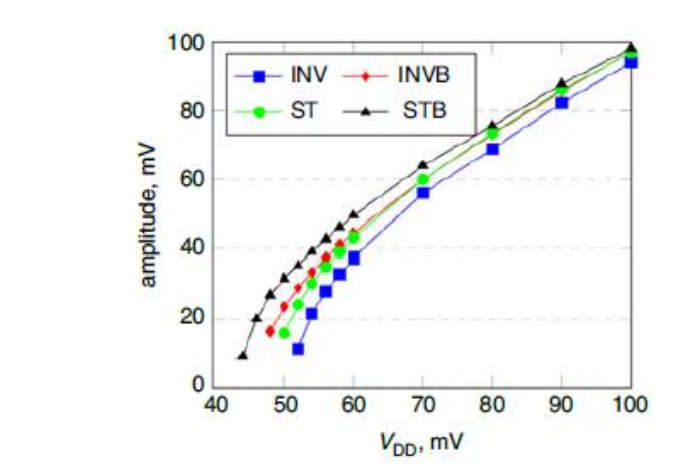
Waveforms of the buffer outputs (top) and differential output voltage of the buffers (bottom) for the ST with the gates connected to the substrates and V_{DD} = 48mV



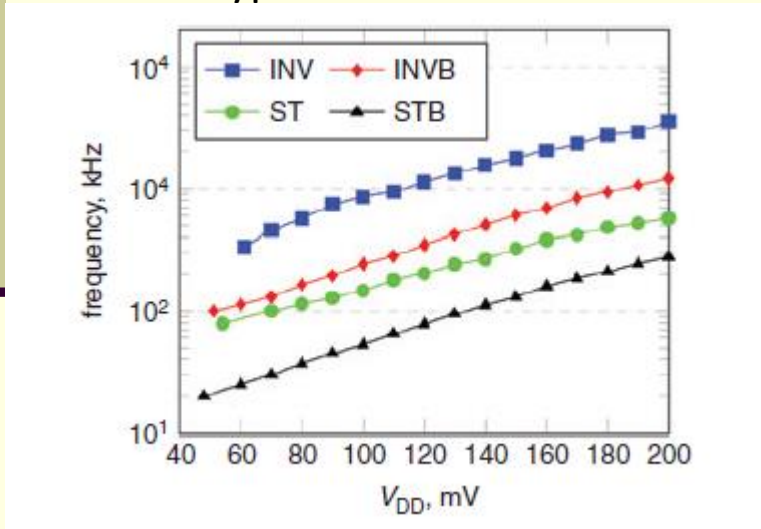
Single and differential output voltages for the STB, with V_{DD} = 80mV. Differential output (diff.) is 20 mV/div

[1]J. Ferreira and C. Galup-Montoro, "Ultra-low-voltage CMOS ring oscillators," Electronics Letters, March 2019.

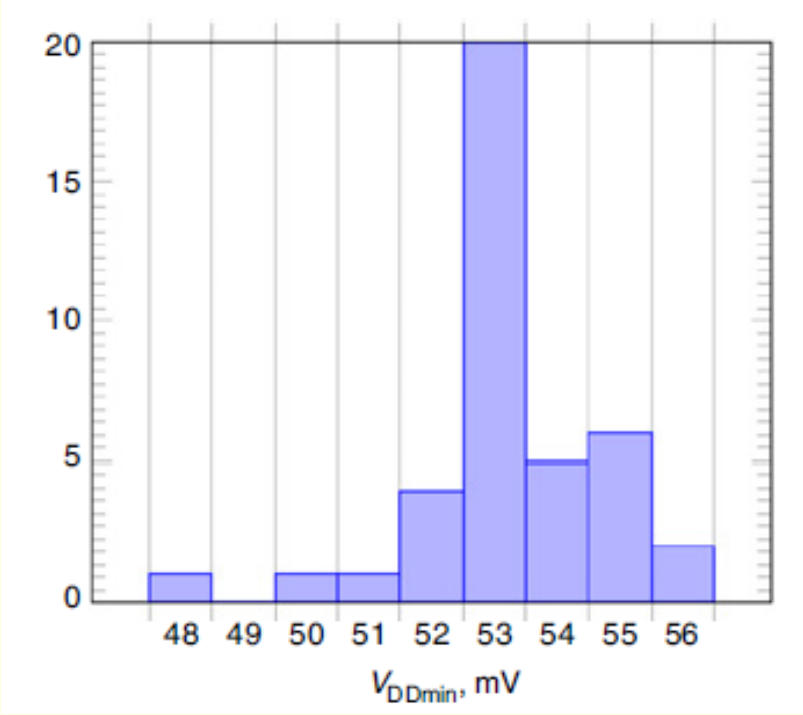
Ultra-low-voltage CMOS ring oscillators-3



The peak-to-peak amplitude of oscillation for four types of ROs



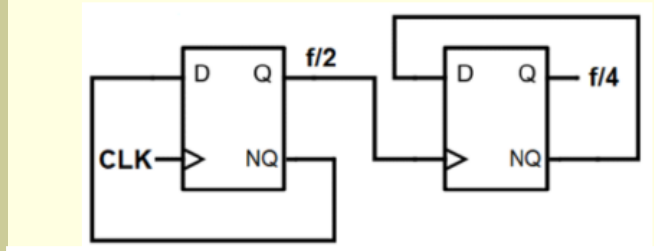
Measured oscillation frequency as a function of the supply voltage

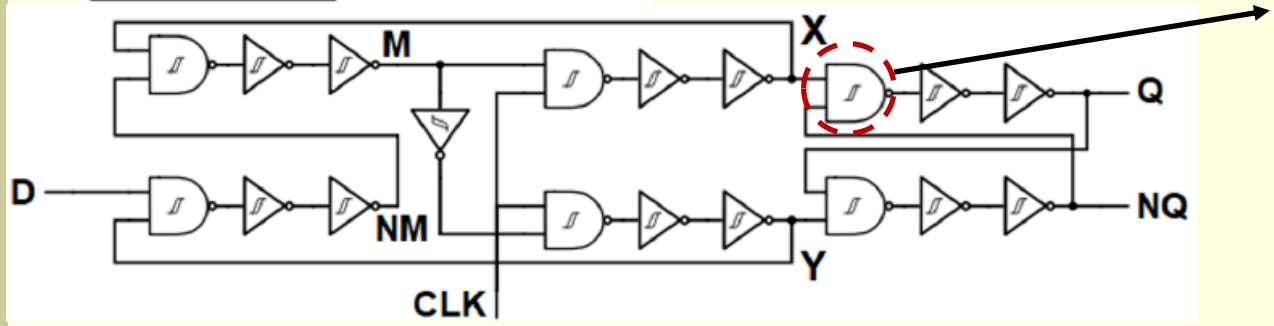


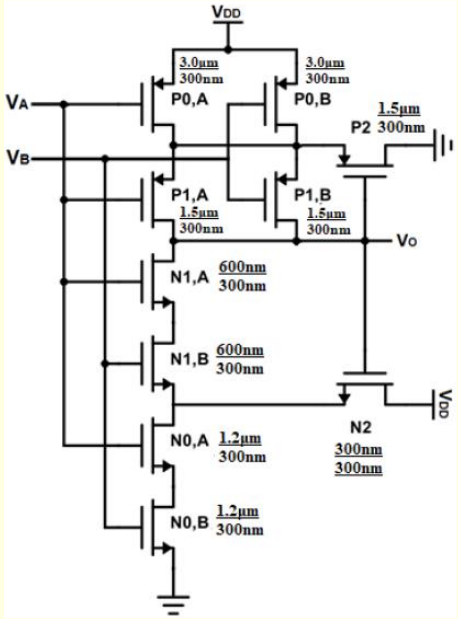
Histogram of the minimum supply voltage for the start-up of the STB oscillator (40 samples)

ST-Based Divide-by-Two Frequency Divider[1, 2]

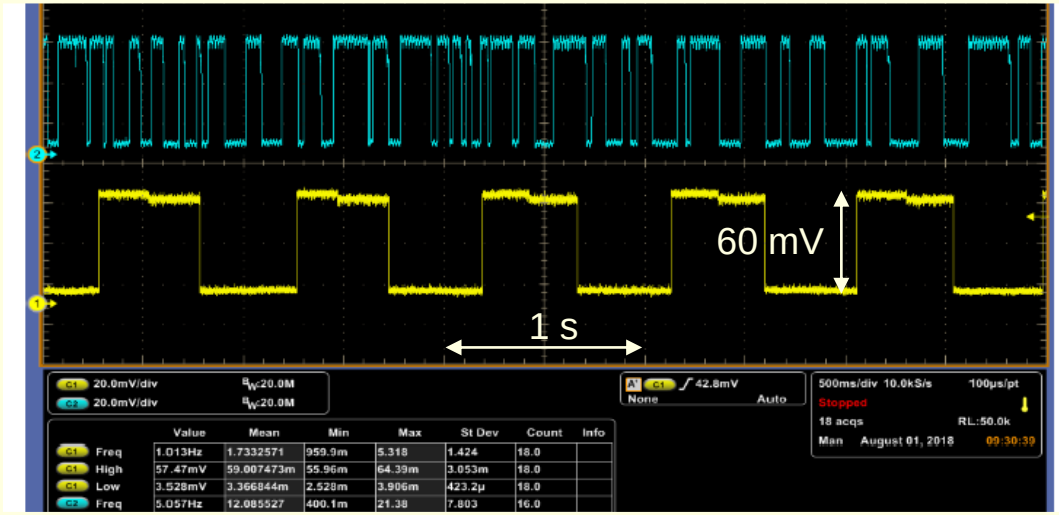
ST-based frequency divider with 2 stages





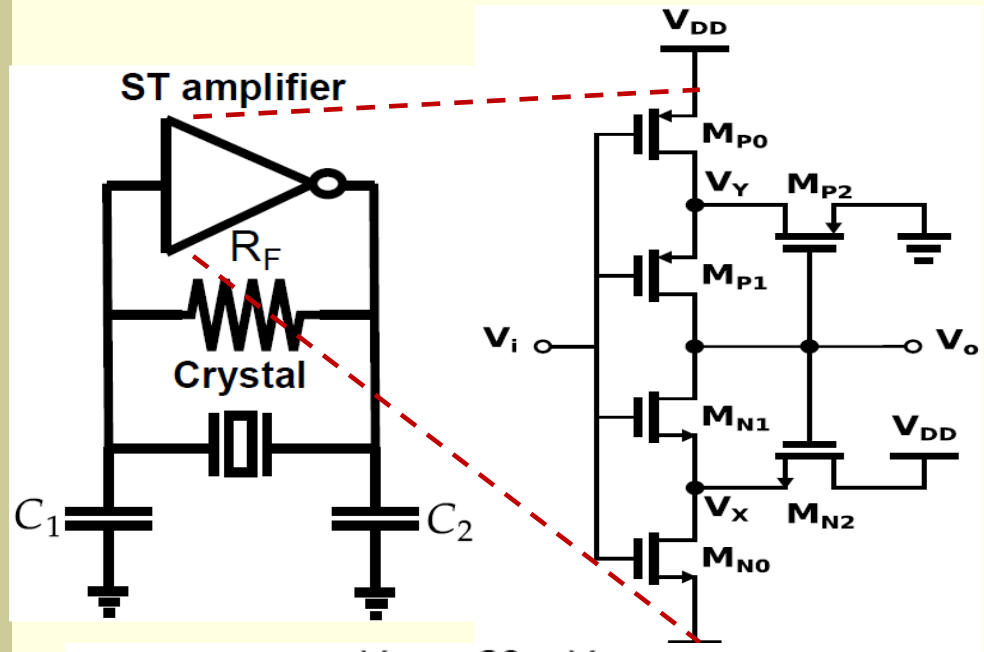


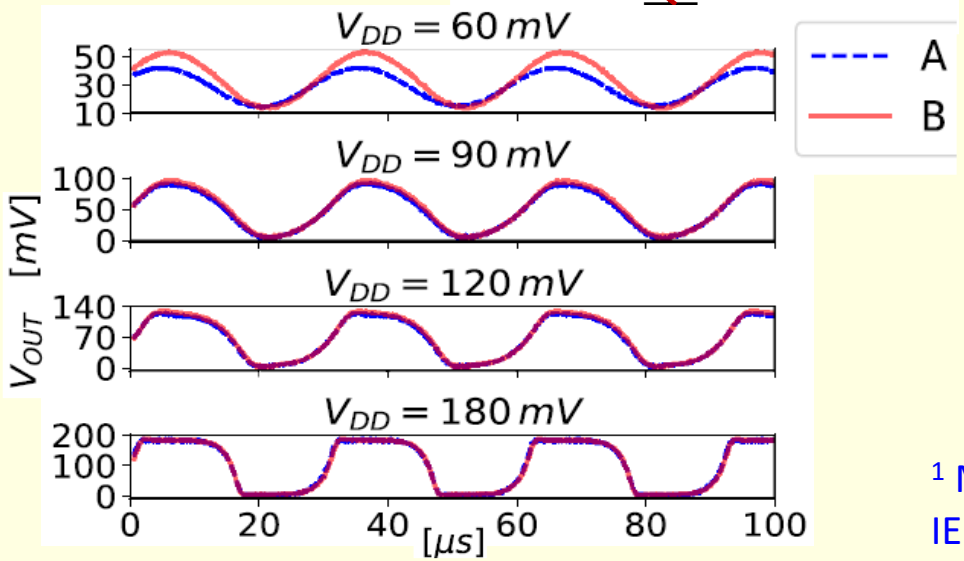
Output signals of frequency divider (2^{15}) at f_{in}= 32768 Hz, V_{DD}=76 mV.
Classical logic: upper wave
ST logic: lower wave



[1] D.G. Alves Neto, C. Galup-Montoro, ISCAS 2020
[2] N. Lotze, Y. Manoli, JSSC 2012

ST Pierce Oscillator[1]

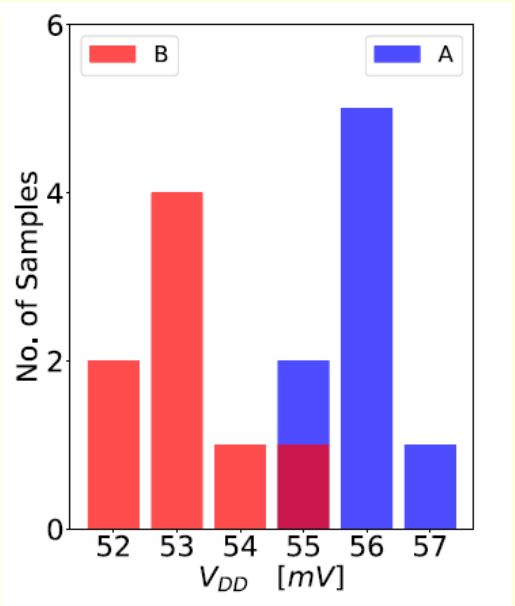




Waveforms of oscillators A and B

130 nm CMOS

Parameter	Oscillator A	Oscillator B
Crystal part number	ABS07W-32.768kHz-D1	AB38T-32.768kHz-12.5pF-E-7
$C_1 = C_2\ [pF]$	6	25
$C_3\ [pF]$	1.15	1.60
$R_F\ [G\Omega]$	5	5



Minimum supply voltage for starting up

[1] M.Siniscalchi, F. Silveira, C. Galup-Montoro, IEEE TCAS-I, 2020.

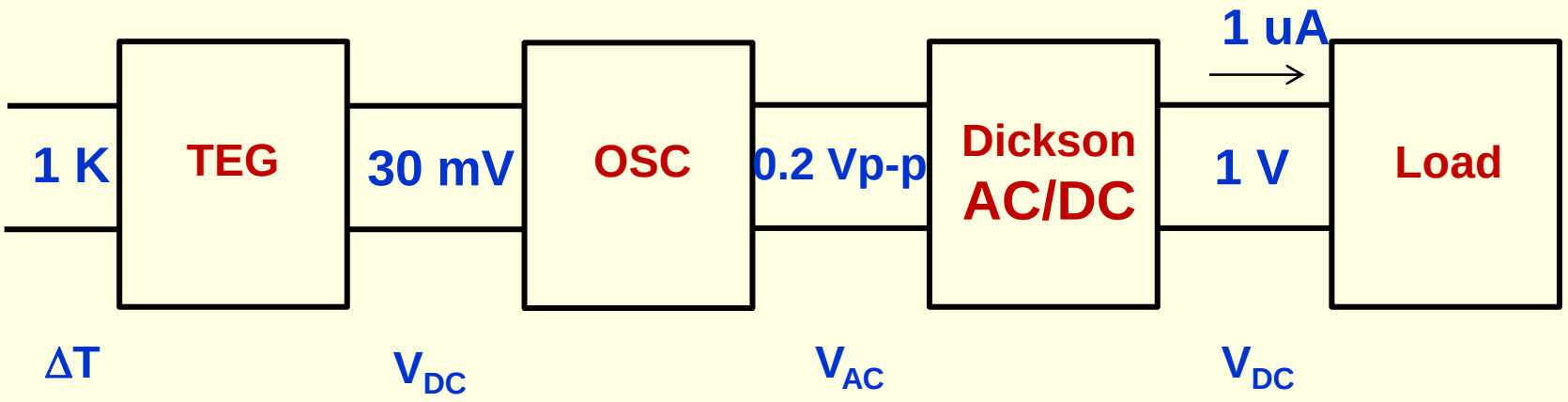
References

- R. M. Swanson and J. D. Meindl, “Ion-implanted complementary MOS transistors in low voltage circuits,” *IEEE J. Solid State Circuits*, vol. 7, pp. 146-153, Apr. 1972.
- J. D. Meindl and A. J. Davis, “*The* fundamental limit on binary switching energy for terascale integration (TSI),” *IEEE J. Solid-State Circuits*, vol. 35, no. 10, pp. 1515-1516, Oct. 2000.
- E. Vittoz, “Weak inversion for ultimate low-power logic”, in *Low-Power Electronics Design*, CRC Press, 2005.
- N. Lotze and Y. Manoli, “A 62mV 0.13um CMOS standard-cell-based design technique using Schmitt-Trigger logic”, *IEEE Journal of Solid-State Circuits*, Jan 2012.
- L. A. P. Malek *et al*., Ultra-Low Voltage CMOS Logic Circuits, *2014 Argentine Conference on Micro-Nanoelectronics, Technology and Applications (EAMTA)*, Mendoza, Argentina 2014.
- L. A. P. Melek *et al.*, “Analysis and design of the classical CMOS Schmitt trigger in subthreshold operation”, *IEEE Trans. Circuits and Systems-I: Reg. Papers*, April 2017.
- L. A. P. Melek *et al.* , "Operation of the Classical CMOS Schmitt Trigger as an Ultra-Low-Voltage Amplifier," IEEE Transactions on Circuits and Systems II-Express Briefs, Sep. 2018.

Outline

- 1. Introduction
- 2. Subthreshold MOSFET model
- 3. Ultra-low-voltage (ULV) CMOS digital circuits
- 4. ULV LC tank oscillators
- 5. ULV rectifiers and voltage multipliers

An important application of ULV oscillators

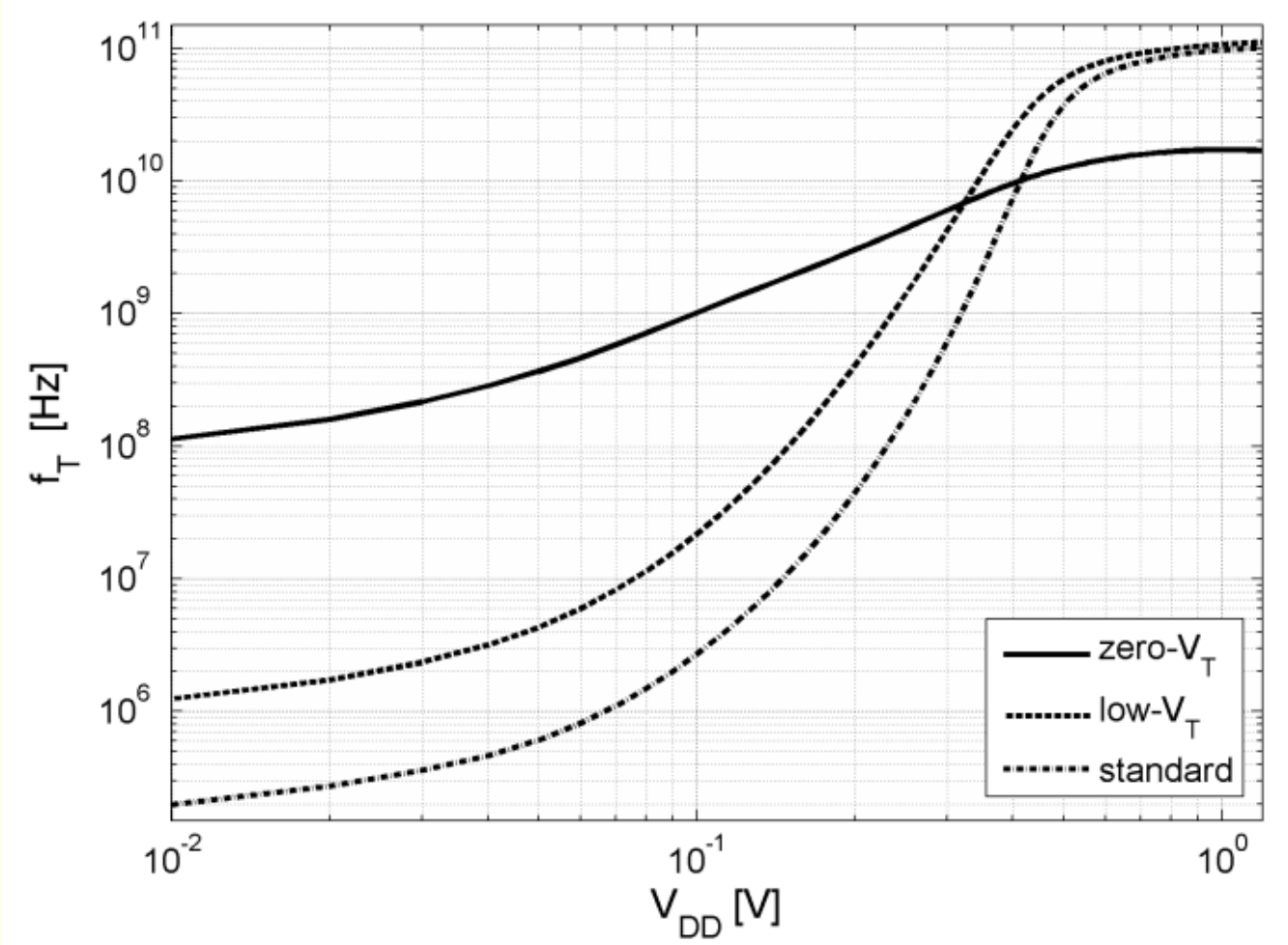


TEG – thermoelectric generator

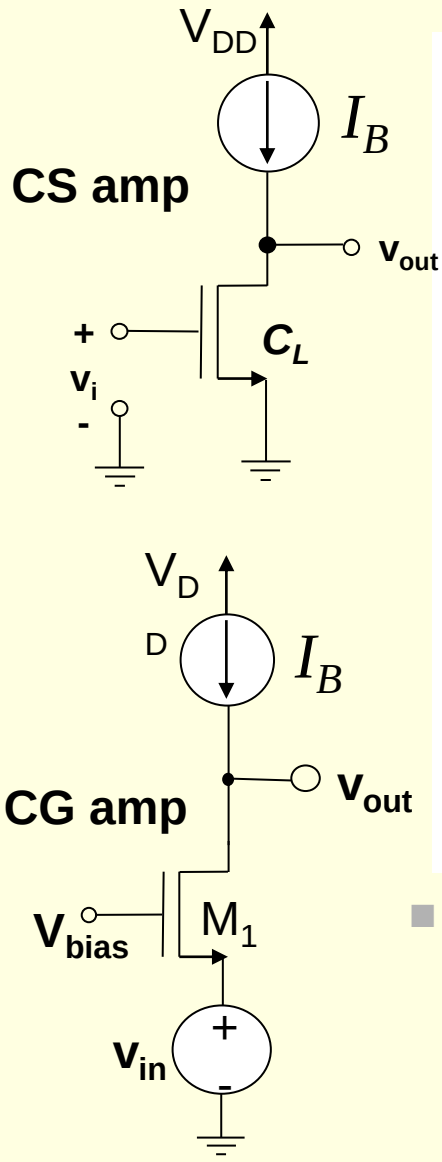
OSC – oscillator

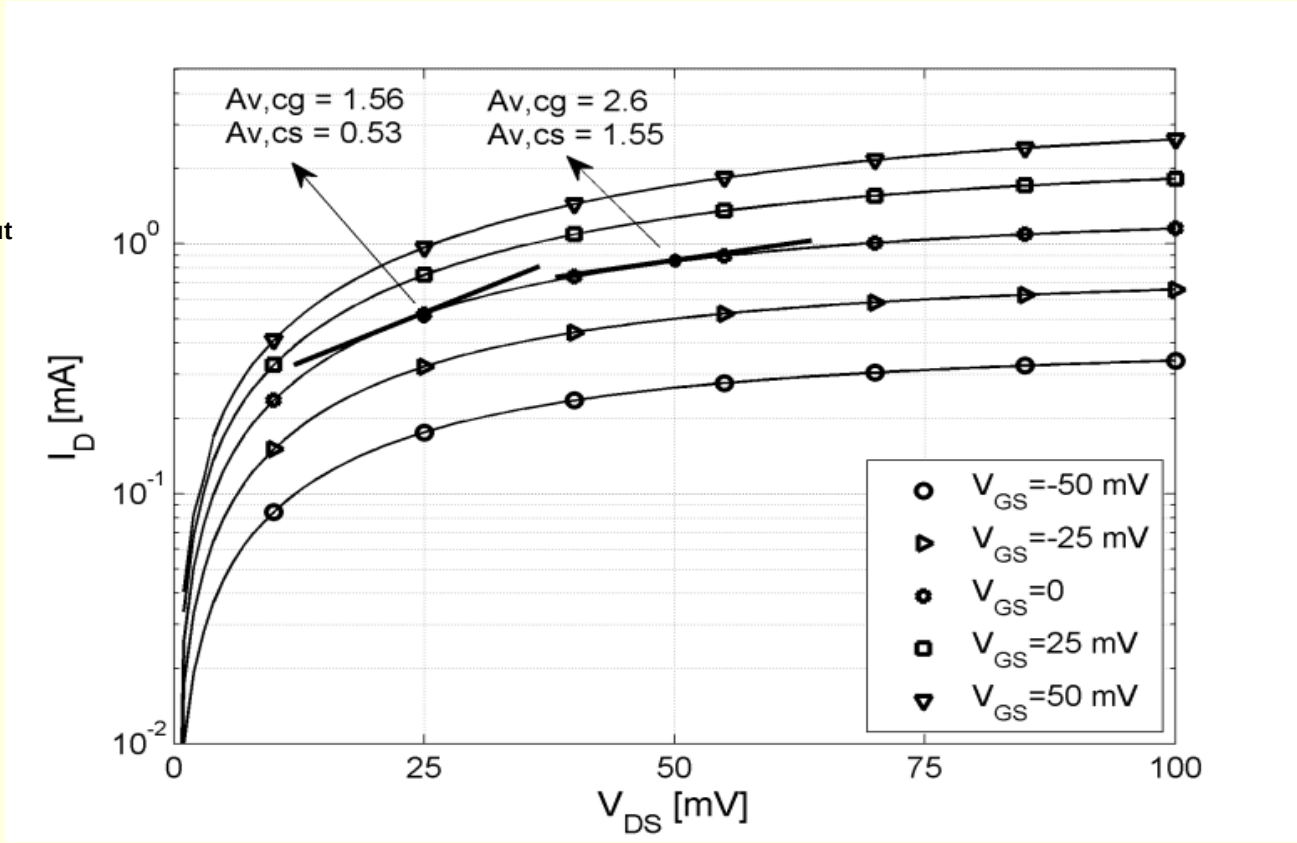
Zero-VT MOSFETs-1

2 – high g_m/C (f_T) for low voltages



Zero-VT MOSFETs-2





- I_D x V_{DS} (V_S=V_B) characteristics for a zero-VT transistor with W/L=2500µm/420nm. For V_{GS}= 0 V and V_{DS}= 25 mV the values of the common-gate and common-source gains are 1.56 and 0.53, respectively (moderate inversion operation).

The pioneer of zero-VT MOSFETs and ULV digital

Cryogenic Ultra Low Power CMOS

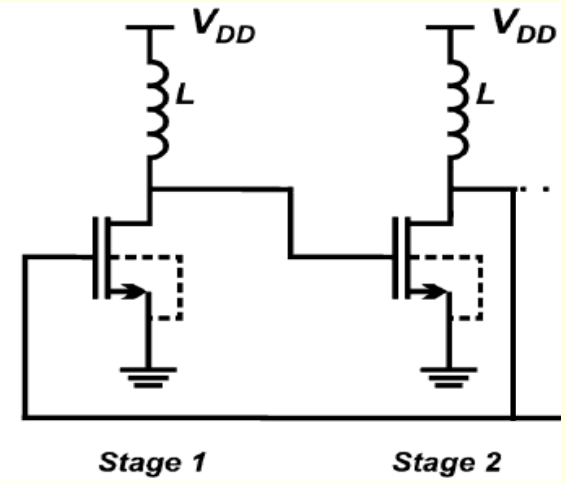
James B. Burr

Department of Electrical Engineering, Stanford University, Stanford CA 94305
burr@mojave.stanford.edu

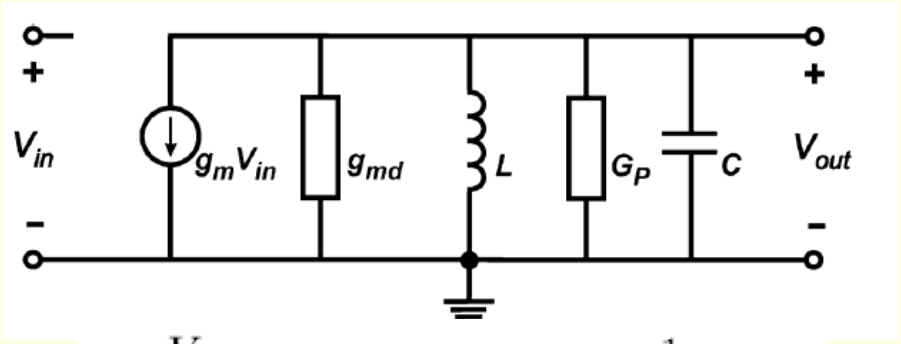
This paper reports 7-stage 1.5um zero Vt CMOS ring oscillators operating at 170MHz/V down to VDD = 70mV at room temperature, and 360MHz/V down to VDD = 27mV at 77degK.

Stanford's Space, Telecommunications, and Radioscience Laboratory has been working on an energy-efficient CMOS technology since December 1990 which can achieve good performance at extremely low supply voltages. Early theoretical work predicted minimum energy at supply and threshold voltages around 120mV at room temperature.

Inductive ring (X-coupled) oscillator - 1



Cross-coupled LC oscillator



$$\frac{V_{out}}{V_{in}} = -\frac{g_m}{g_{md}+G_P}\frac{1}{1-j\tan\phi}$$

$$\tan\phi = \frac{1-LC\omega^2}{\omega L(g_{md}+G_p)}$$

=–1

Criterion for oscillation (Barkhausen)

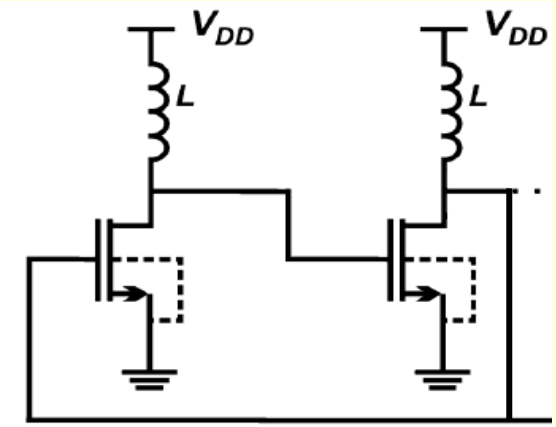
$\phi=0$ & $V_{out}/V_{in}=-1$

$$\omega^2 LC = 1$$

$$\frac{g_m}{g_{md}+G_P} = 1$$

What´s the minimum V_{DD} for oscillation?

Inductive ring oscillator - 2



Cross-coupled LC oscillator

Oscillation frequency $\omega^2 LC = 1$

Voltage gain $\dfrac{g_m}{g_{md} + G_P} = 1$

What´s the minimum V_{DD} for oscillation?

Recall that $g_m = \dfrac{g_{ms} - g_{md}}{n}$

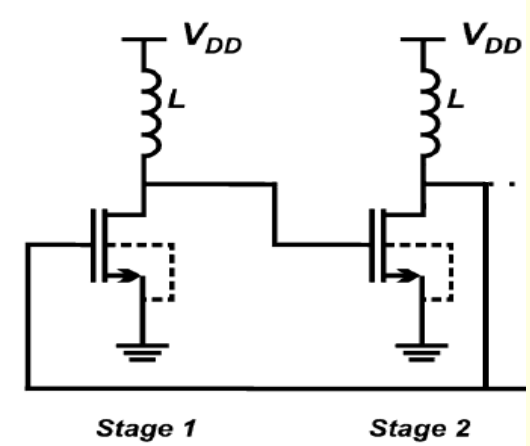
Voltage gain=1 ⇒ (i) $\dfrac{g_{ms}}{g_{md}} = 1 + n\left(1 + \dfrac{G_P}{g_{md}}\right)$

In weak inversion ⇒ (ii) $\dfrac{g_{ms}}{g_{md}} = e^{V_{DS}/\varphi_t} = e^{V_{DD}/\varphi_t}$ since $V_G = V_D = V_{DD}$

$$V_{DD,\min} = \varphi_t \ln\left[1 + n\left(1 + \frac{G_P}{g_{md}}\right)\right] = \varphi_t \ln\left[1 + n\right] \quad \text{for} \quad \frac{G_P}{g_{md}} << 1$$

Similar to the result (1/2) of the CMOS inverter

Inductive ring oscillator - 3



Questions:

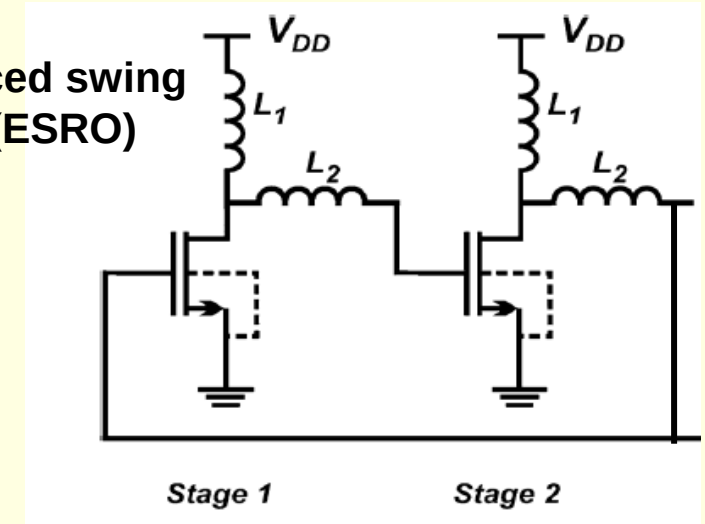
1. How to reduce $V_{DD,min}$?

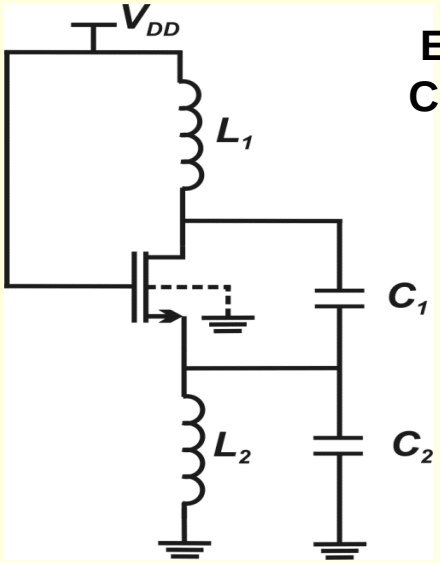
2. How to increase the V_{DD}-limited voltage swing?

Introduce voltage gain from drain to gate

Change topology, e. g., take advantage of CG gain

Enhanced swing IRO (ESRO)

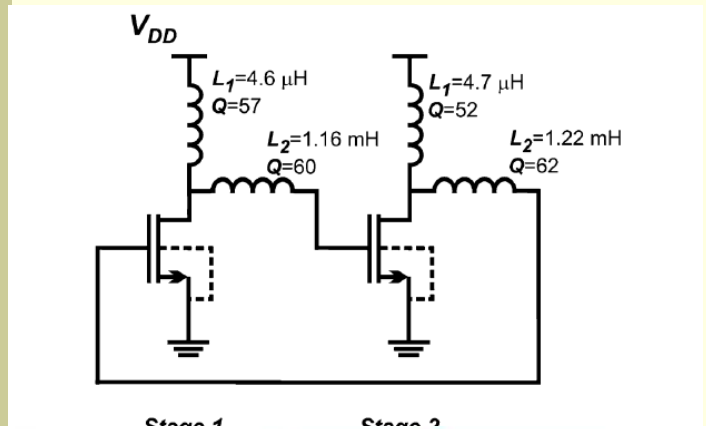


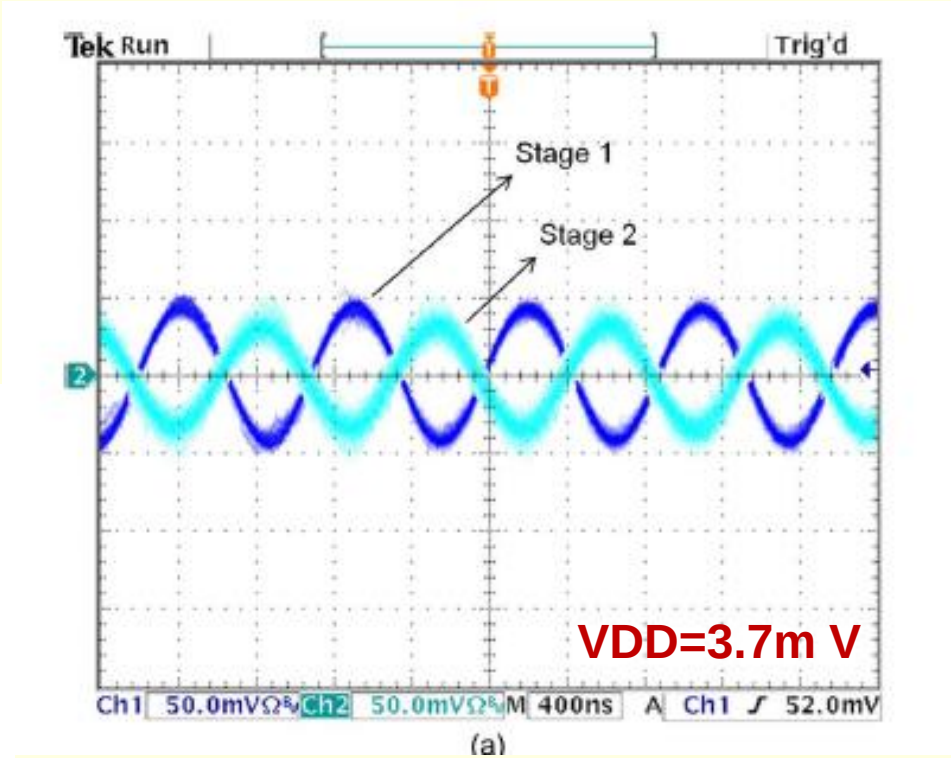


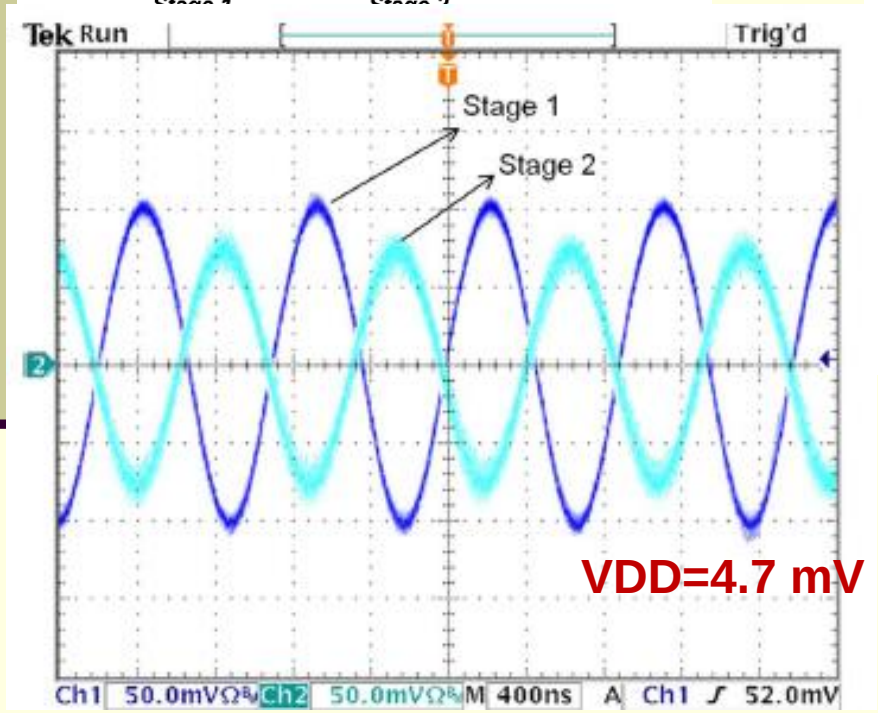
Enhanced swing Colpitts oscillator (ESCO) *

* T. W. Brown et al, *IEEE JSSC*, Aug. 2011.

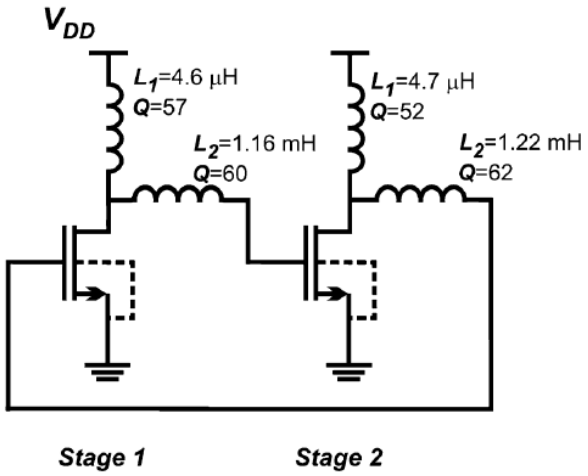
Enhanced swing IRO (ESRO)-1







Enhanced swing IRO (ESRO)-2



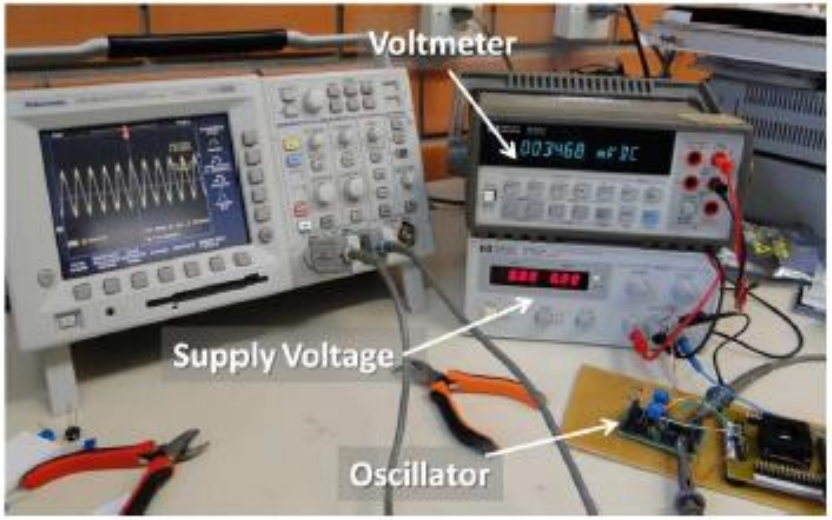


Fig. 13. Picture showing the discrete prototype of the enhanced swing inductive-load oscillator and test equipment.

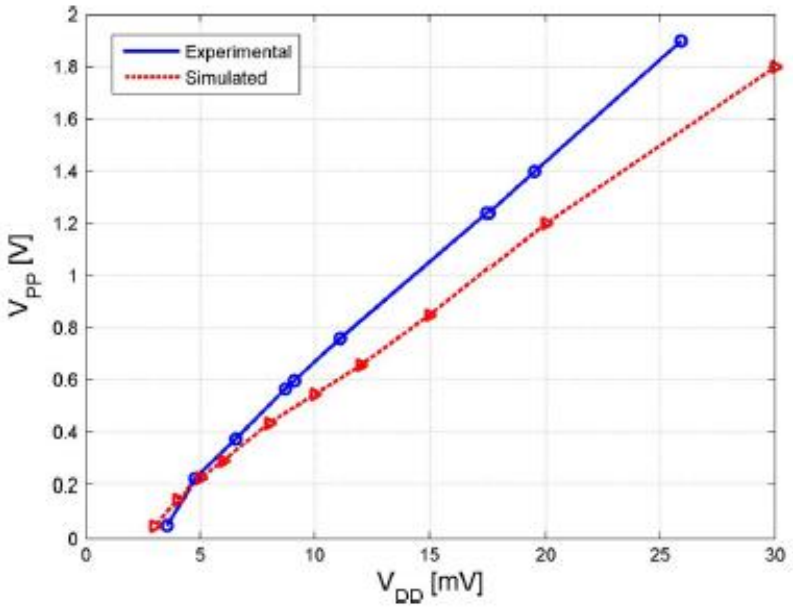
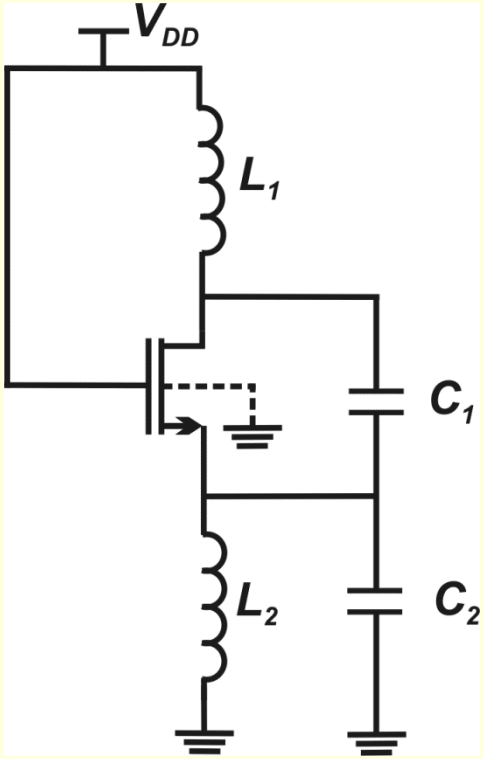
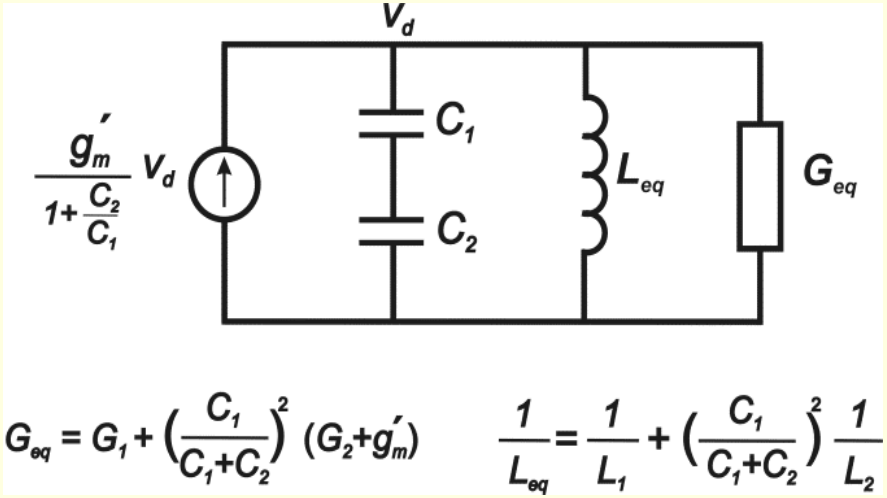


Fig. 12. Simulated (dotted line) and experimental (solid line) peak-to-peak gate voltage versus supply voltage of the ES inductive-load ring oscillator.

ESCO: small-signal model



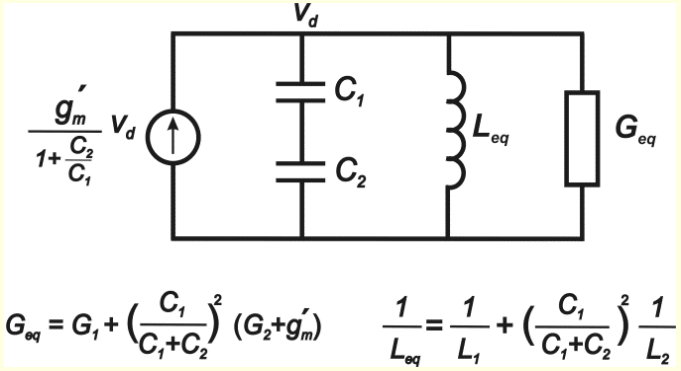


$$v_s \cong \frac{v_d}{1+\frac{C_2}{C_1}} \rightarrow g_{ms} v_s - g_{md} v_d \cong g_m' v_s$$

$$g_m' = g_{ms} - \left(1+\frac{C_2}{C_1}\right) g_{md}$$

ESCO: start-up condition

$$g_{ms} > \left(1+\frac{C_2}{C_1}\right) g_{md} + \frac{C_1}{C_2} G_2 + \left(2+\frac{C_1}{C_2}+\frac{C_2}{C_1}\right) G_1$$



Optimum value of capacitors to minimize g_{ms} (for the conventional Colpitts $g_{md} = G_2 = 0$!)

$$\frac{C_2}{C_1} = \sqrt{\frac{G_1+G_2}{g_{md}+G_1}}$$

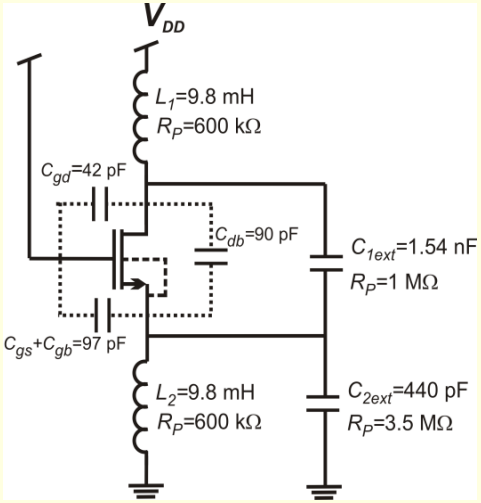
For ideal inductors (and capacitors) $G_1 = G_2 = 0$

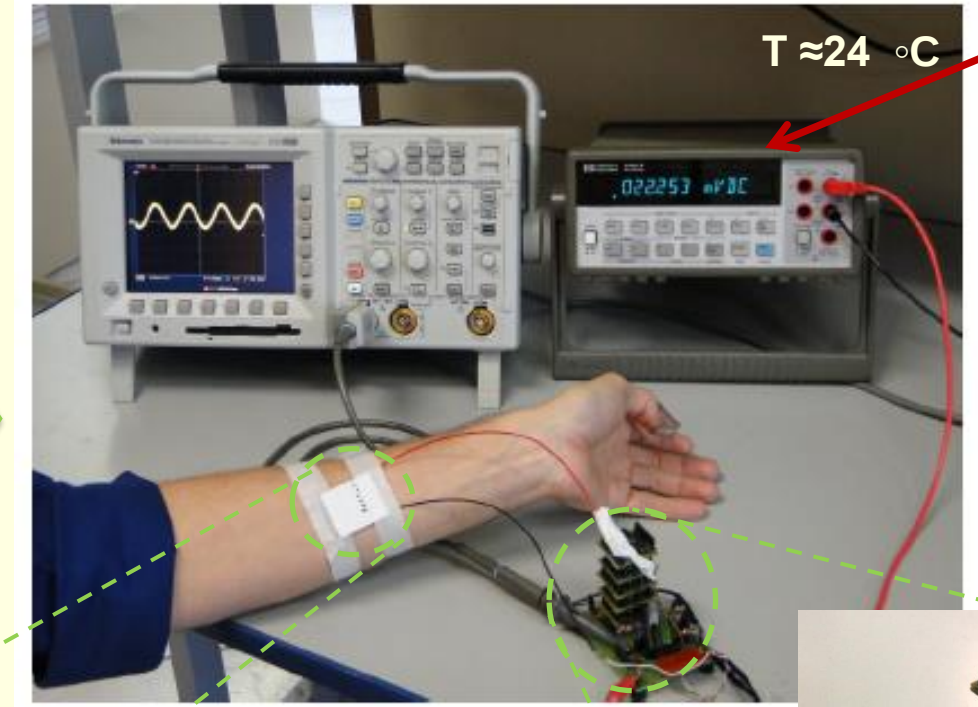
$$g_{ms} > \left(1+\frac{C_2}{C_1}\right) g_{md}$$

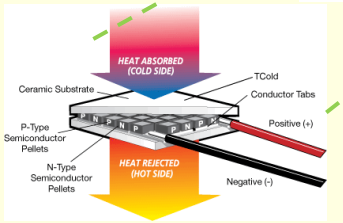
$$V_{DD\lim} = \frac{kT}{q} \ln\left(1+\frac{C_2}{C_1}\right)$$

Colpitts oscillator: first prototype

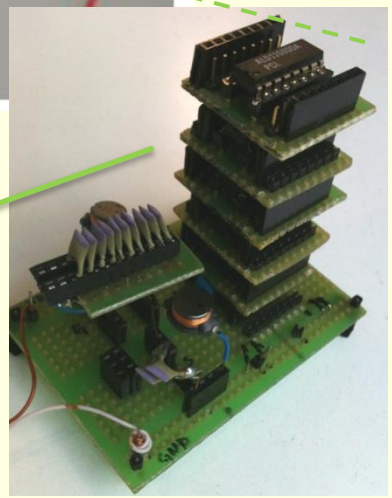
Powered by a thermoelectric generator







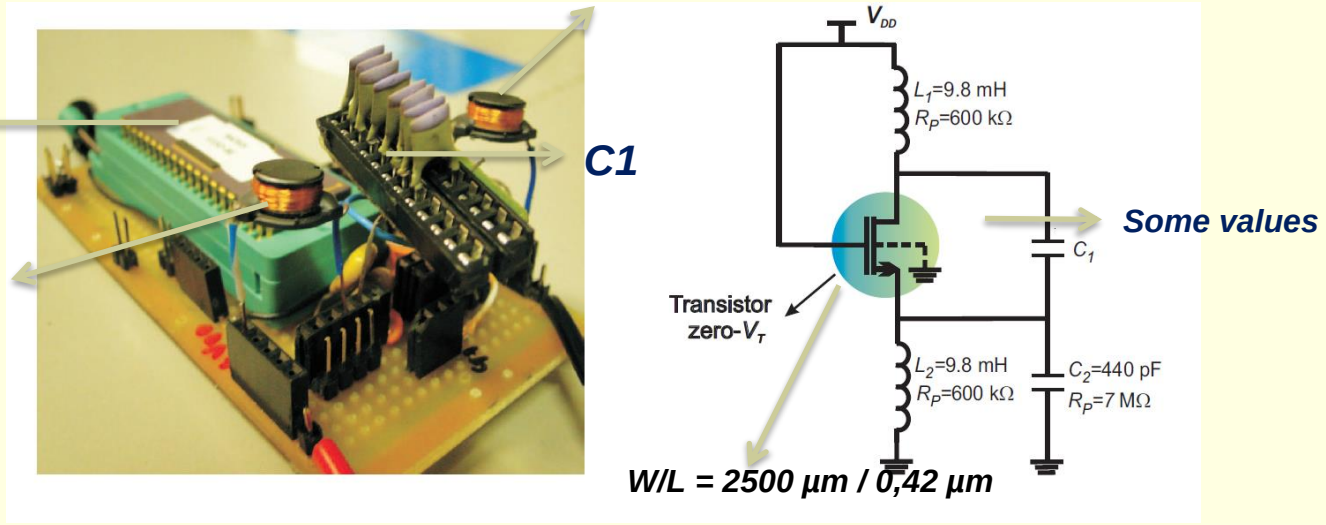
thermoelectric generator

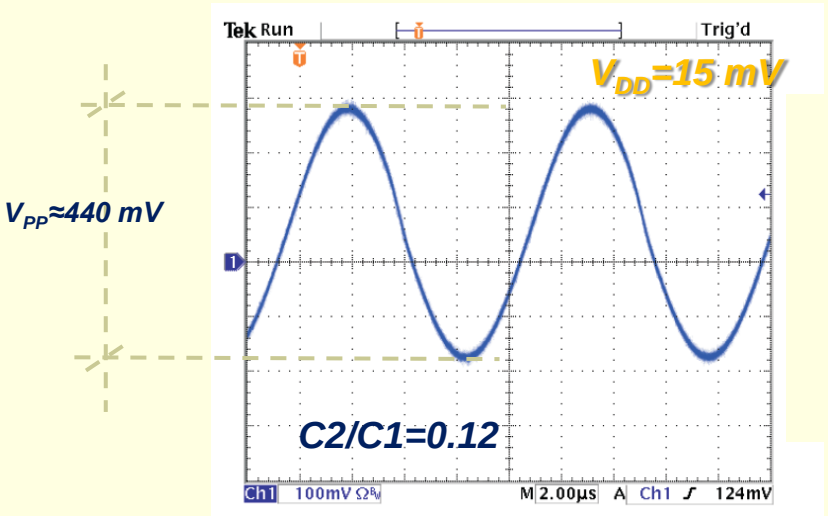


24 // NMOS
Zero-VT (ALD 1108)
VT=59 mV, IS=11.2 uA

Colpitts oscillator: second prototype

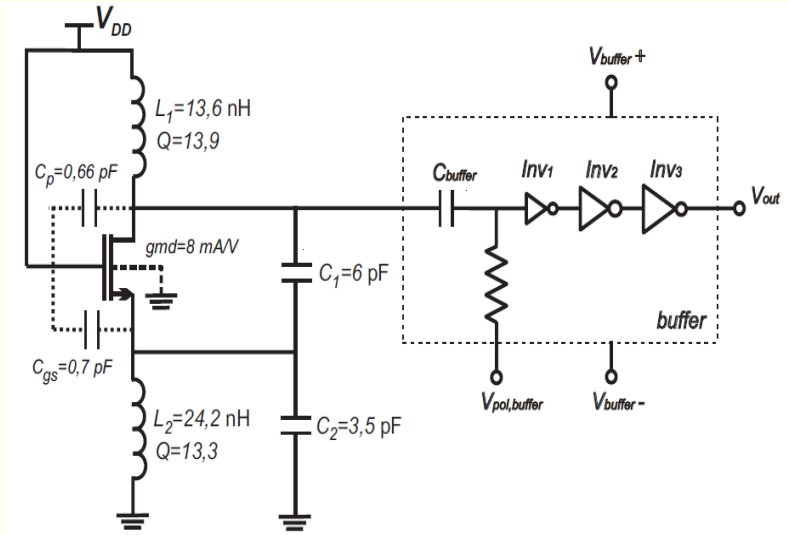
Vdd < 20 mV

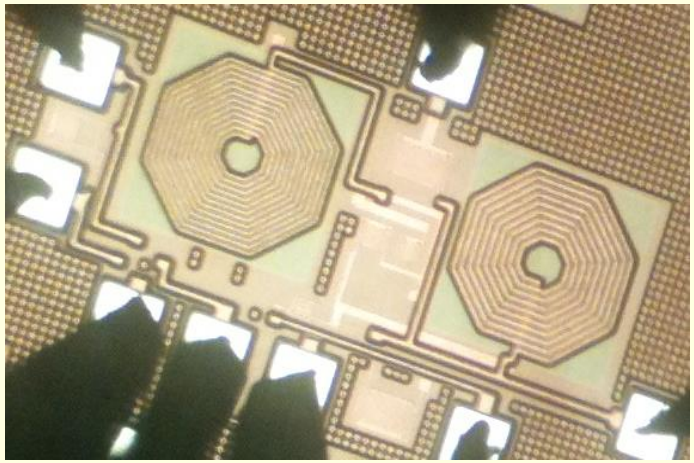




f_{osc}≈110 kHz
V_{DD}=15 mV

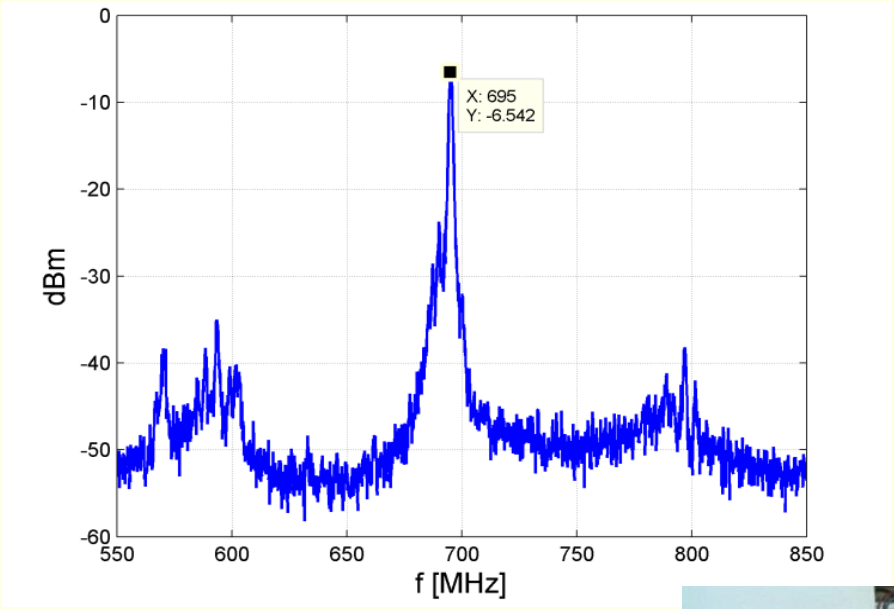
ESCO designed for operation at 800 MHz





- Micrograph of the ESCO built in 130 nm technology

Spectral diagram of the ESCO (V_{DD} = 86 mV)



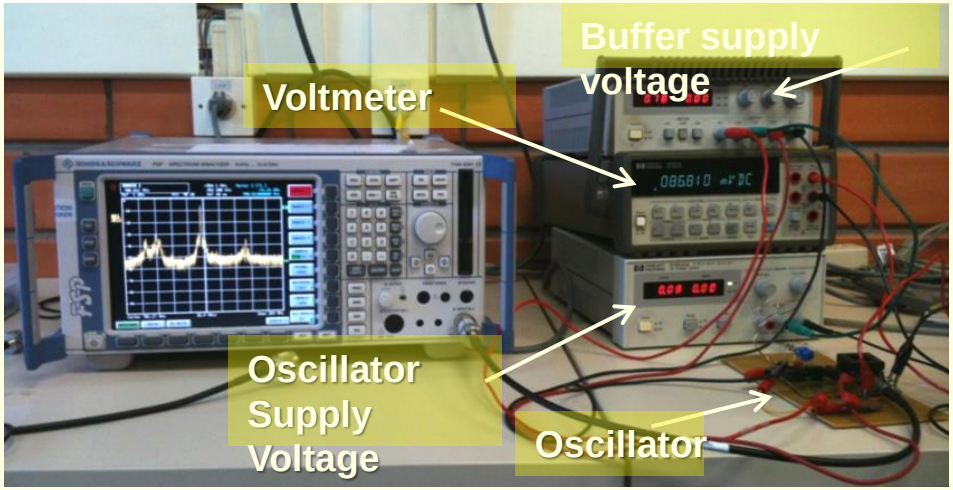


TABLE I
EXPERIMENTAL RESULTS FOR THE OSCILLATION FREQUENCY AND MINIMUM SUPPLY VOLTAGE OF THE OSCILLATOR TOPOLOGIES

Topology	Theoretical V_{dd} (min) *	IC prototype 130nm CMOS		Discrete prototype	
		V_{dd} (min)	f_{osc}	V_{dd} (min)	f_{osc}
ILRO	$\phi_t \ln(1+n)$	53 mV	550 MHz	50 mV	11 MHz
ESRO	$\phi_t \ln\left(1+n\frac{L_1}{L_1+L_2}\right)$	32 mV	400 MHz	3.5 mV	1.1 MHz
ESCO	$\phi_t \ln\left(1+\frac{C_2/C_1}{1+L_1/L_2}\right)$	86 mV	700 MHz	15 mV	108 kHz

* For lossless passive devices and operation of MOSFETs in weak inversion

Values of components:
ILRO – IC prototype – L = 100 nH, Q = 8.
ILRO – discrete prototype – L = 4.6 uH, Q = 50.
ESRO – IC prototype – L_1 = 20 nH, Q_1 = 9; L_1 = 80 nH, Q_2 = 8.
ESRO – discrete prototype – L_1 = 4.6 uH, Q_1 = 55, L_2 = 1.2 mH, Q_2 = 60.
ESCO – IC prototype – L_1 = 13.6 nH, Q_1 = 13.9, L_2 = 24.2 nH, Q_2 = 13.3, C_1 = 6 pF, C_2 = 3.5 pF.
ESCO – discrete prototype – $L_1 = L_2$ = 9.8 mH, $Q_1 = Q_2$ = 80, C_1 = 1.54 nF, C_2 = 0.44 nF.

References

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- M. B. Machado *et al.* , “On the minimum supply voltage for MOSFET oscillators”, *IEEE Transactions on Circuits and Systems I: Regular Papers*, Feb 2014.
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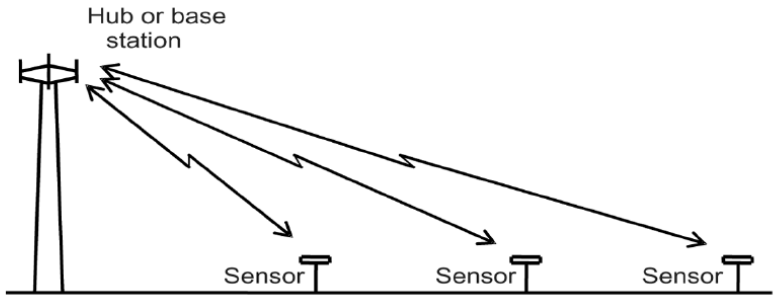
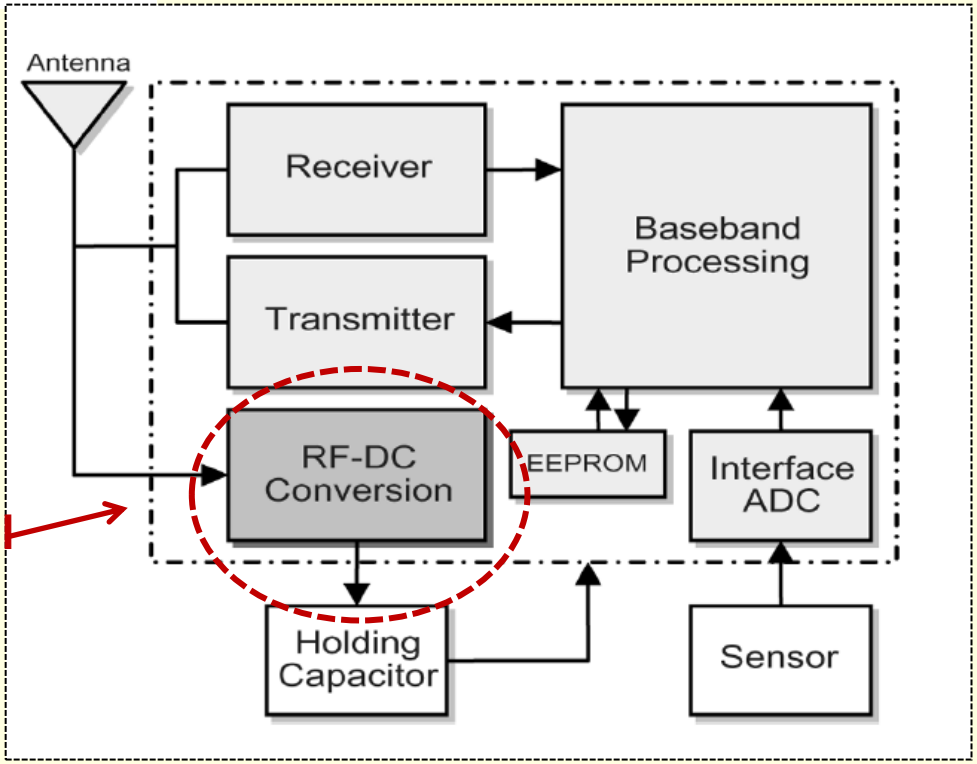
Outline

- 1. Introduction
- 2. Subthreshold MOSFET model
- 3. Ultra-low-voltage (ULV) CMOS digital circuits
- 4. ULV LC tank oscillators
- 5. ULV rectifiers and voltage multipliers

Motivation

Wirelessly powered sensors

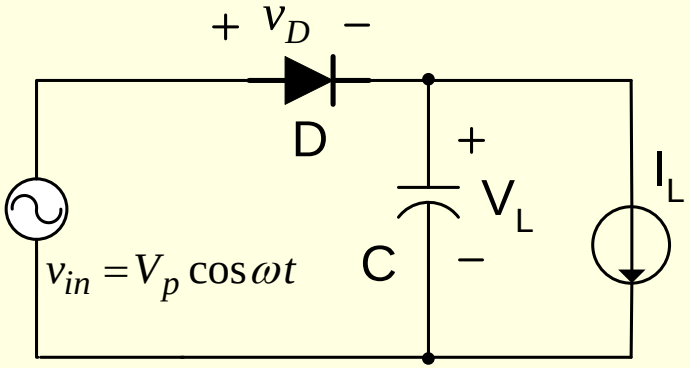


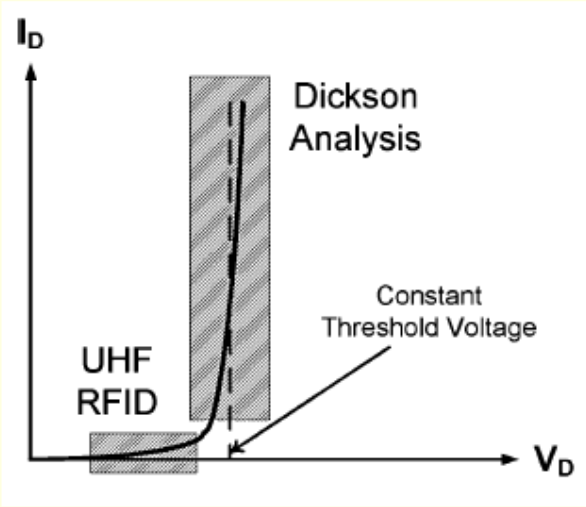


Low power/voltage level

Low-voltage diode circuits

Dickson analysis of voltage multipliers: constant threshold voltage diode model, not appropriate for low voltage operation





$V_L = V_P - V_{ON}$

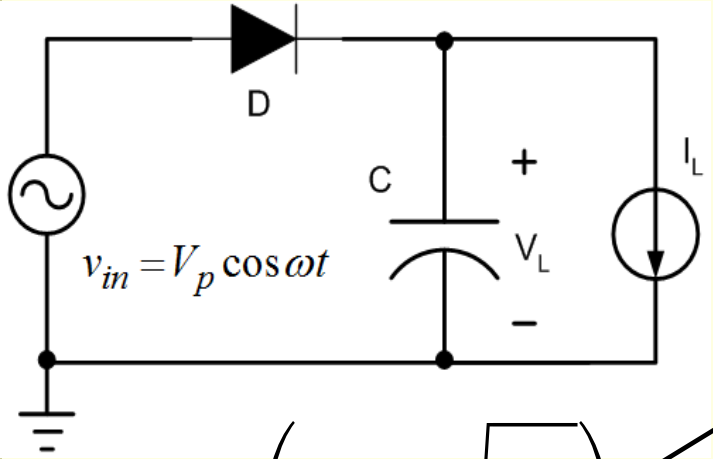
How to substitute the constant 'diode voltage drop' model?

Use the i-v characteristic of the diode and the load current

$$I_D = I_S[e^{\frac{V_D}{n\phi_t}} - 1] \qquad \phi_t = \frac{kT}{q}$$

$$n \sim 1 \text{ to } 1.5$$

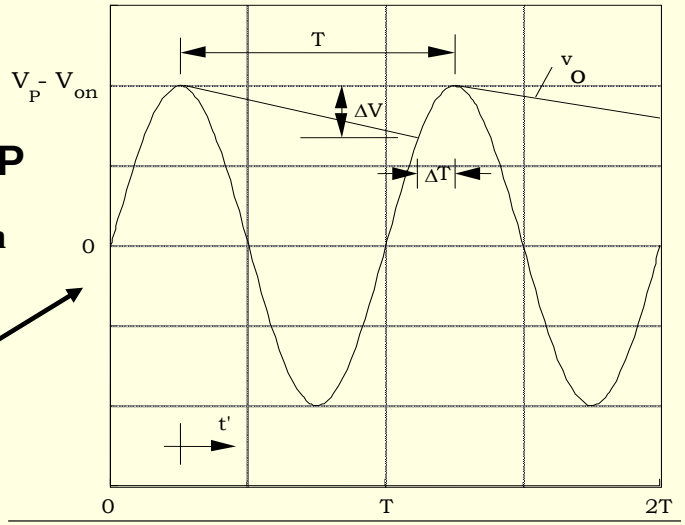
Classical rectifier analysis



High V_P

$V_P >> V_{on}$

correct



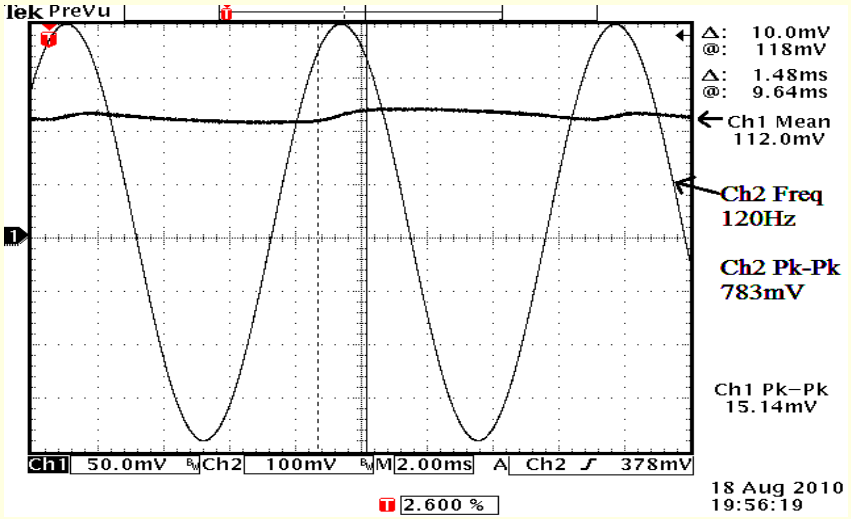
$$I_P \cong I_L \left(1 + 2\pi \sqrt{\frac{2V_P}{\Delta V}}\right)$$

$$\Delta V \cong \frac{I_L}{fC}$$

wrong

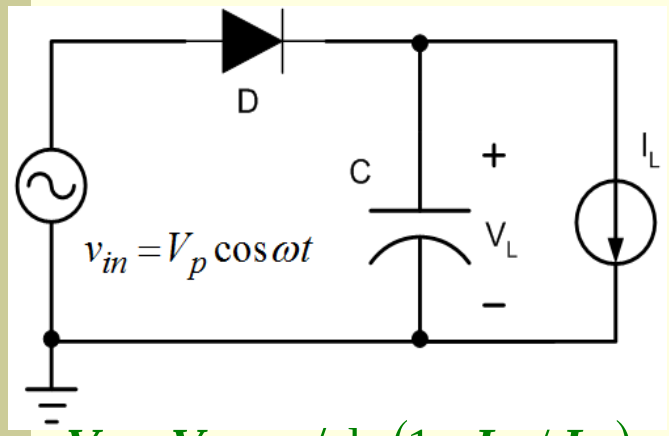
Low V_P

$$\Delta V \to 0, I_P \to \infty \text{ !!}$$



The diode does not have a constant voltage drop, diode current is LIMITED!

Physics-based rectifier model

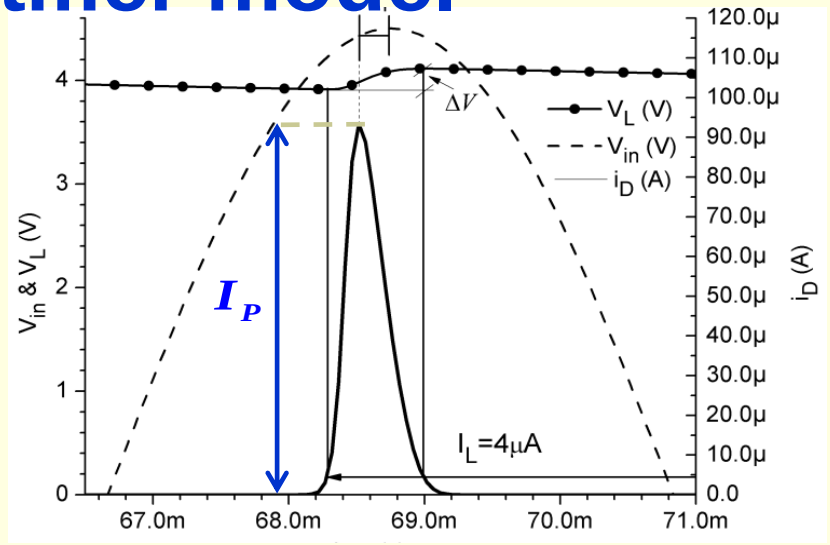


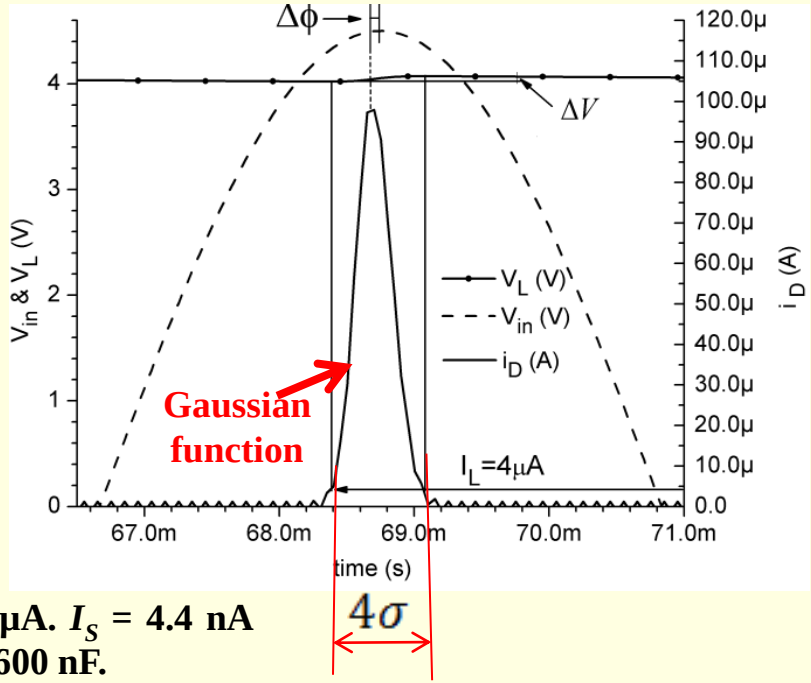
$$V_L \cong V_P - n\phi_t \ln\left(1 + I_P / I_S\right) \qquad V_P > n\phi_t$$

$$\left.\begin{aligned} I_P &\cong I_L \sqrt{\frac{2\pi V_P}{n\phi_t}} \\ \theta_C &= 4\sigma = 4\sqrt{\frac{n\phi_t}{V_P}} \end{aligned}\right\} \quad I_P \theta_C \cong 4 I_L \sqrt{2\pi}$$

$$\Delta V \cong \frac{I_L T}{C}\left(1 - \frac{\theta_C}{2\pi}\right) \cong \frac{I_L T}{C}$$

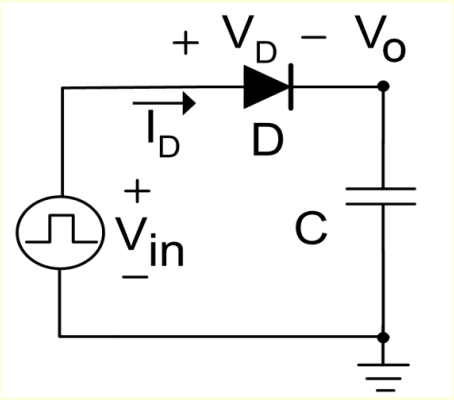
I_P: peak current
θ_C: conduction angle



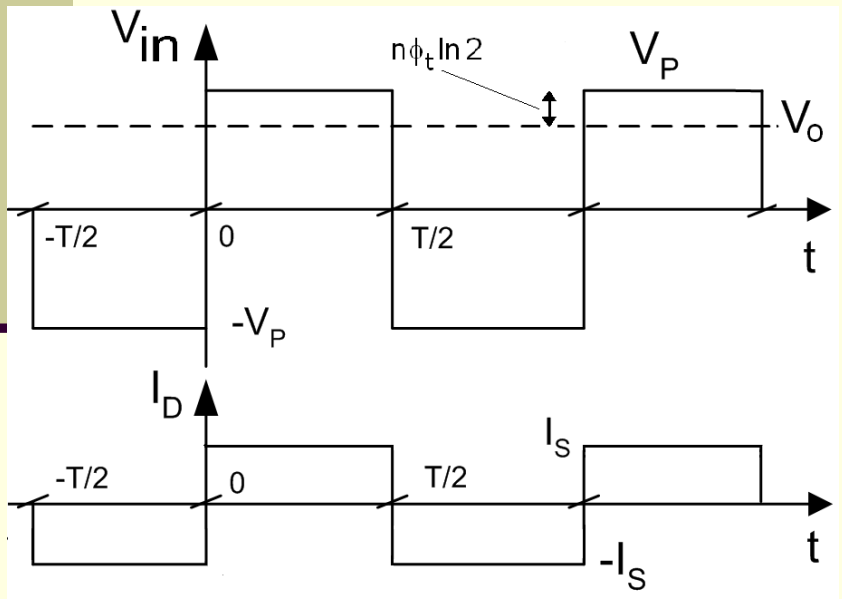


V_P = 4.5 V, f=120 Hz and I_L=4μA. I_S = 4.4 nA and $n\phi_t$= 50 mV. C=150 nF and 600 nF.

ULV rectifier with pure capacitive load - 1



$V_P >> n\phi_t$



Steady-state analysis

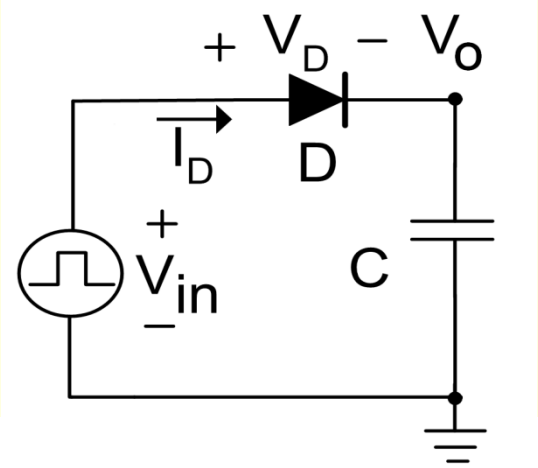
$$\frac{1}{T}\int_{-T/2}^{T/2} I_D dt = 0 \qquad I_D = I_S\left[e^{\frac{V_D}{n\phi_t}} - 1\right]$$

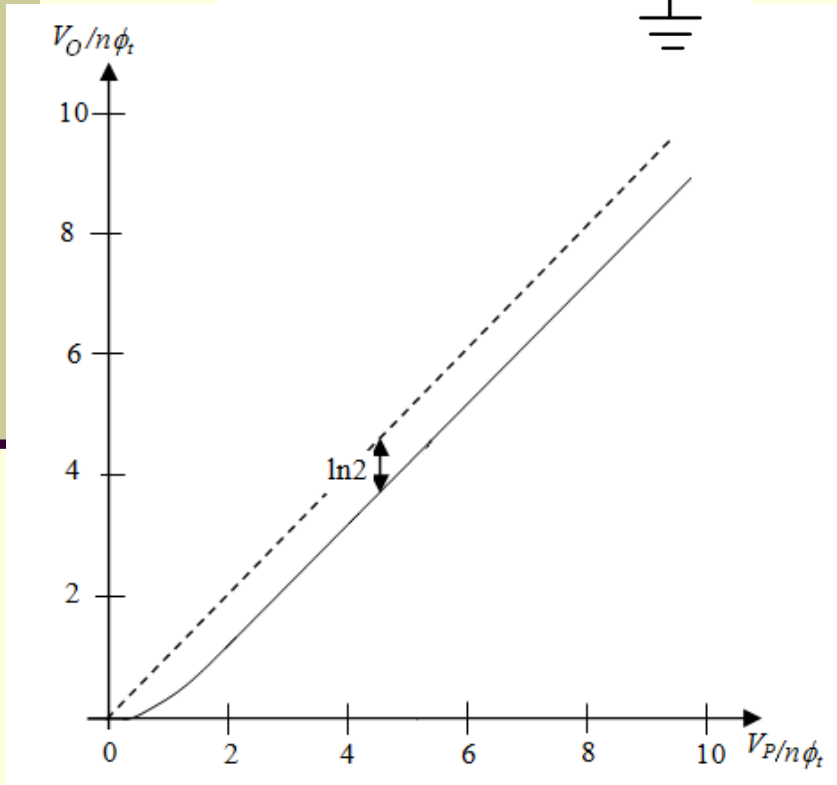
$$\frac{I_S}{T}\left[\int_{-T/2}^{0}\left(e^{\left(\frac{-V_P - V_o}{n\phi_t}\right)} - 1\right)dt + \int_{0}^{T/2}\left(e^{\left(\frac{V_P - V_o}{n\phi_t}\right)} - 1\right)dt\right] = 0$$

Assumption: very low ripple (high C)
→ V_o ≅ constant

$$\frac{V_o}{n\phi_t} = \ln\left[\frac{e^{V_P/n\phi_t} + e^{-V_P/n\phi_t}}{2}\right] = \ln\left[\cosh\left(V_P/n\phi_t\right)\right]$$

ULV rectifier with pure capacitive load - 2





$$\frac{V_o}{n\phi_t} = \ln\left[\cosh\left(V_P/n\phi_t\right)\right]$$

Power Detector

$$V_P << n\phi_t \quad \rightarrow \quad \frac{V_o}{n\phi_t} \cong \frac{1}{2}\left(\frac{V_P}{n\phi_t}\right)^2$$

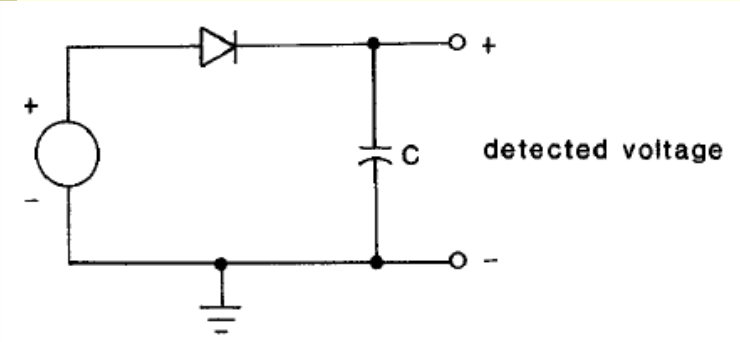
Peak Detector

Diode "ON" voltage drop

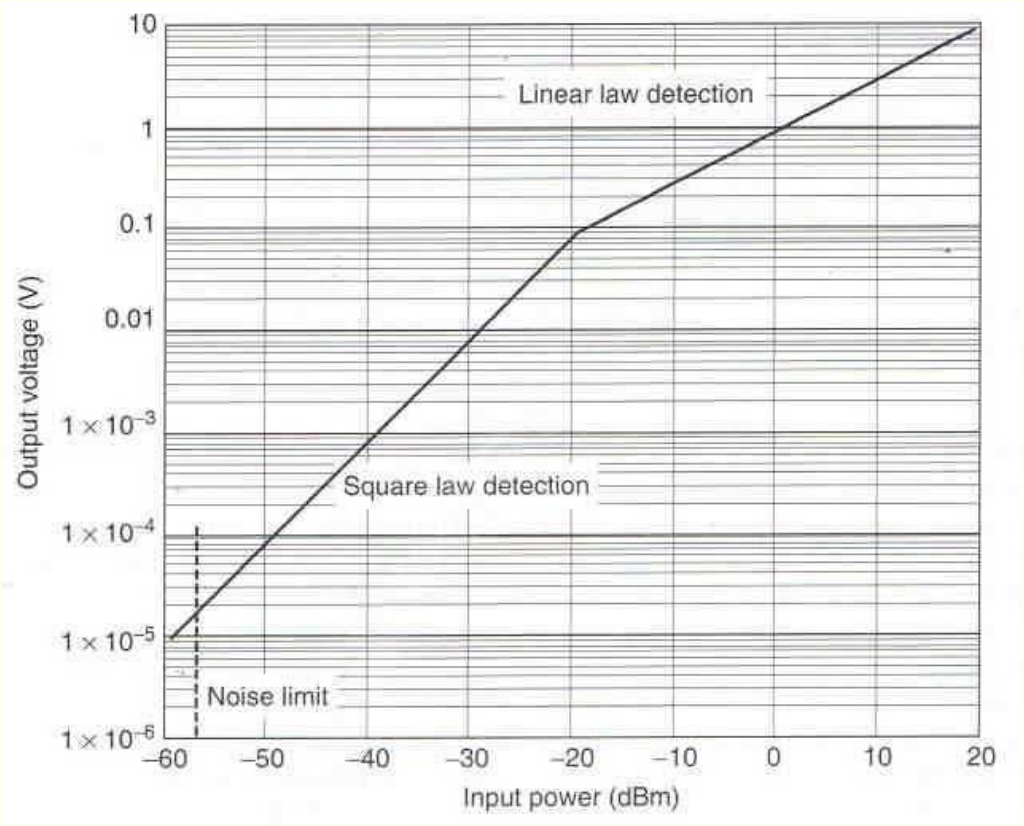
$$V_P >> n\phi_t \quad \rightarrow \quad V_L \cong V_P - n\phi_t \ln 2$$

Input

Application: microwave power detection



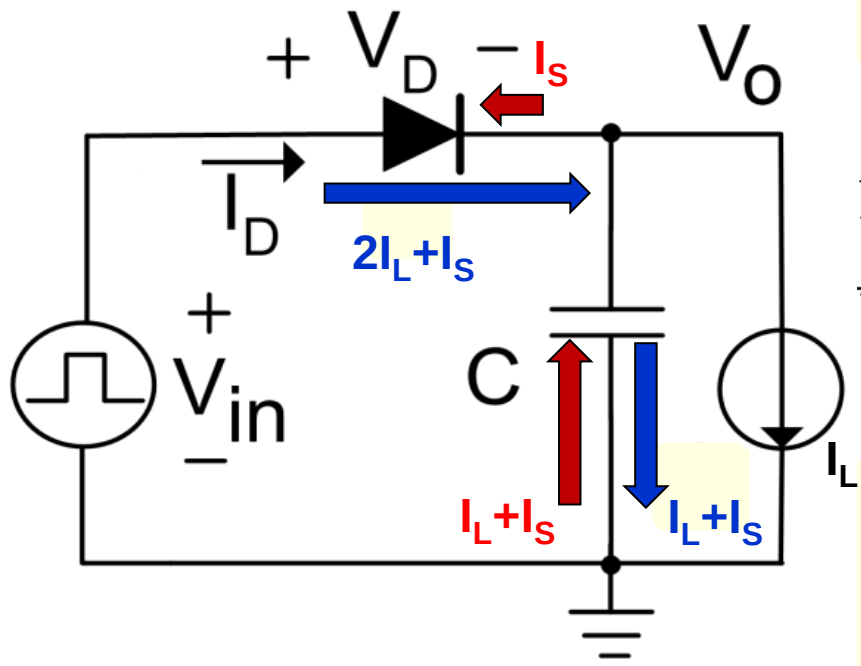
- Basic detector circuit



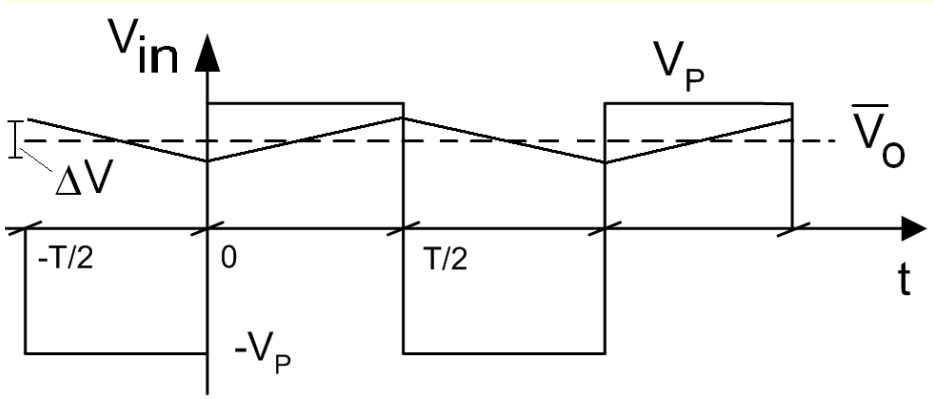
R. G. Meyer, “ Low-power monolithic RF peak detector analysis, ” IEEE J. Solid-State Circuits, vol. 30, no. 1, pp. 65–67, Jan. 1995.

Wetenkamp, IEEE MTT-S Int. Microwave Symp. Dig., 1983

ULV rectifier with DC load - 1



Output voltage ripple

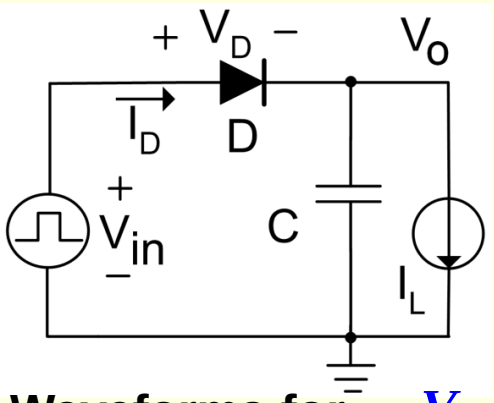


The discharge rate of the capacitor

$$I_C = \frac{dQ_C}{dt} = C\frac{dV_C}{dt} \cong I_L + I_S$$

$$\int_{-T/2}^{0} dV_C = \Delta V \cong \frac{I_L + I_S}{C}\frac{T}{2} = \frac{I_L + I_S}{2fC}$$

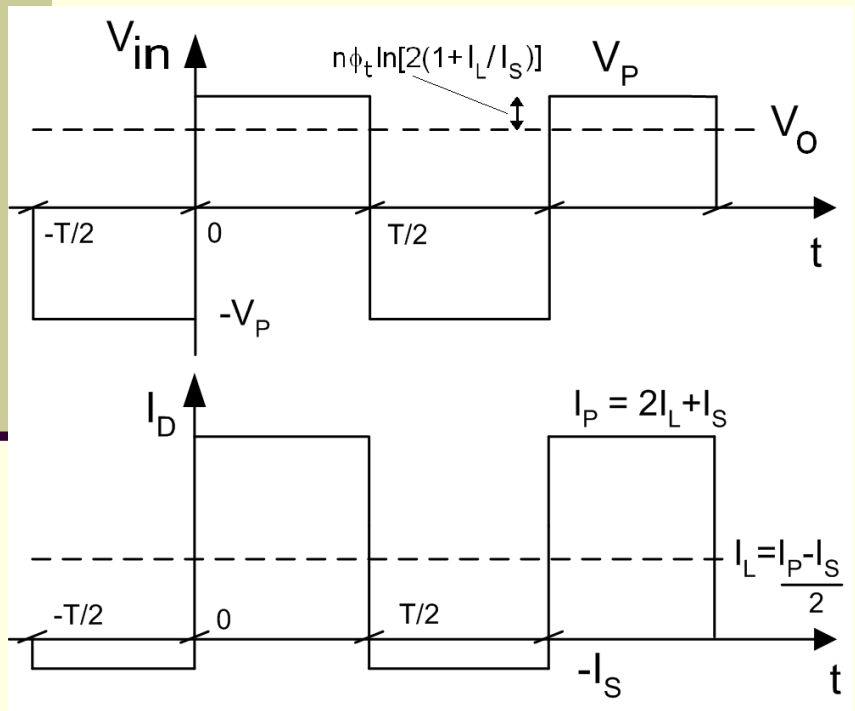
ULV rectifier with DC load - 2



Steady-state analysis

$$\frac{I_S}{T}\left[\int_{-T/2}^{0}\left(e^{\left(\frac{-V_P-V_o}{n\phi_t}\right)}-1\right)dt+\int_{0}^{T/2}\left(e^{\left(\frac{V_P-V_o}{n\phi_t}\right)}-1\right)dt\right]=I_L$$

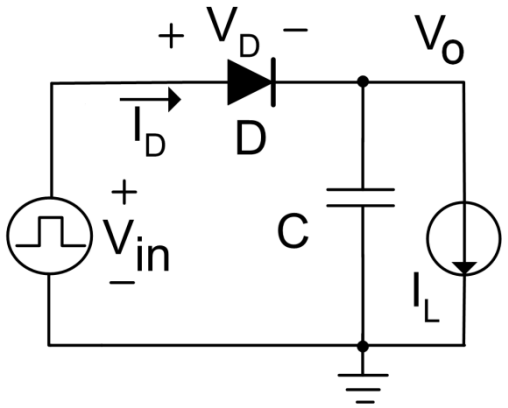
Waveforms for $V_P >> n\phi_t$



Assumption: very low ripple → V_o ≅ constant

$$\frac{V_o}{n\phi_t}=\ln\left[\frac{\cosh\left(V_P/n\phi_t\right)}{1+I_L/I_S}\right]$$

ULV rectifier with DC load - 3

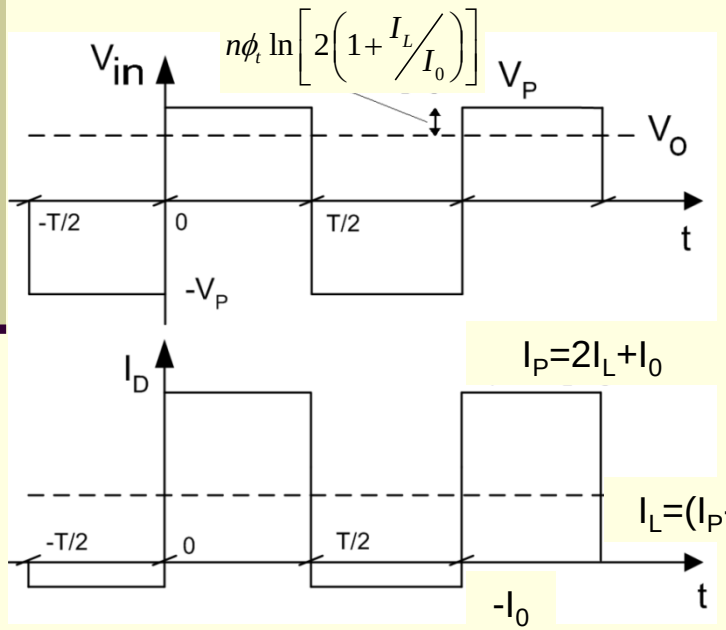


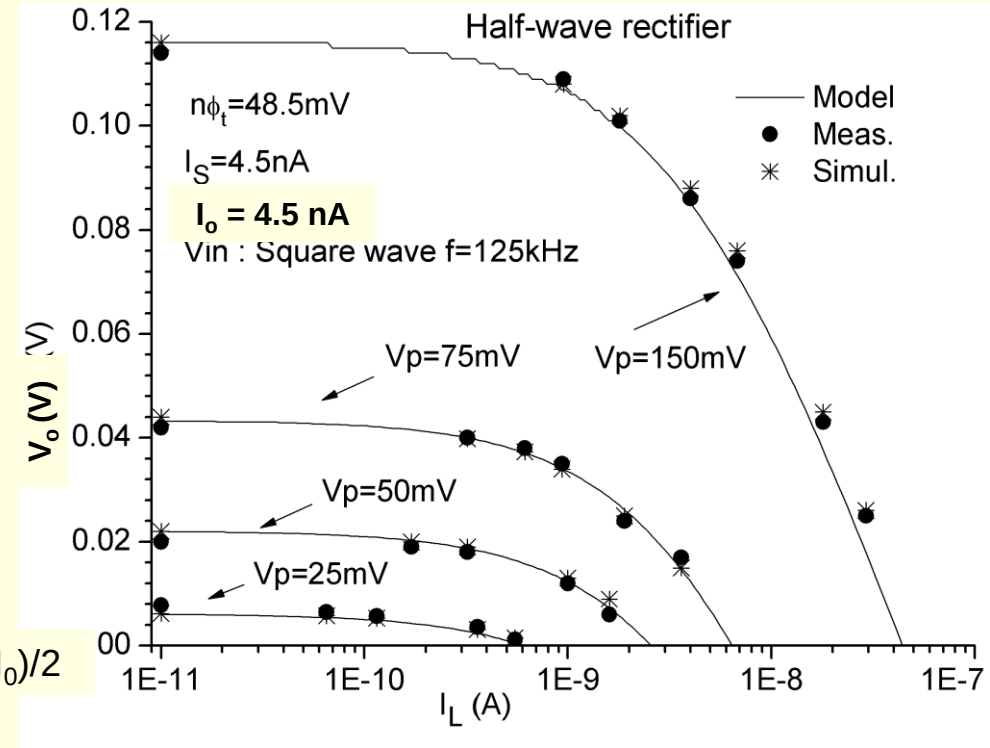
Input

Diode "ON" voltage drop

$$V_P > n\phi_t \rightarrow V_o \cong V_P - n\phi_t \ln\left(\frac{I_P + I_0}{I_0}\right)$$

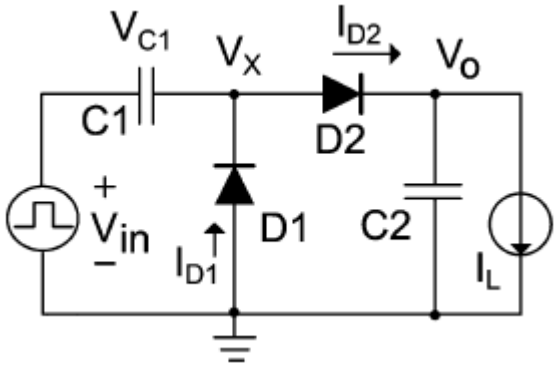
Waveforms for $V_P >> n\phi_t$

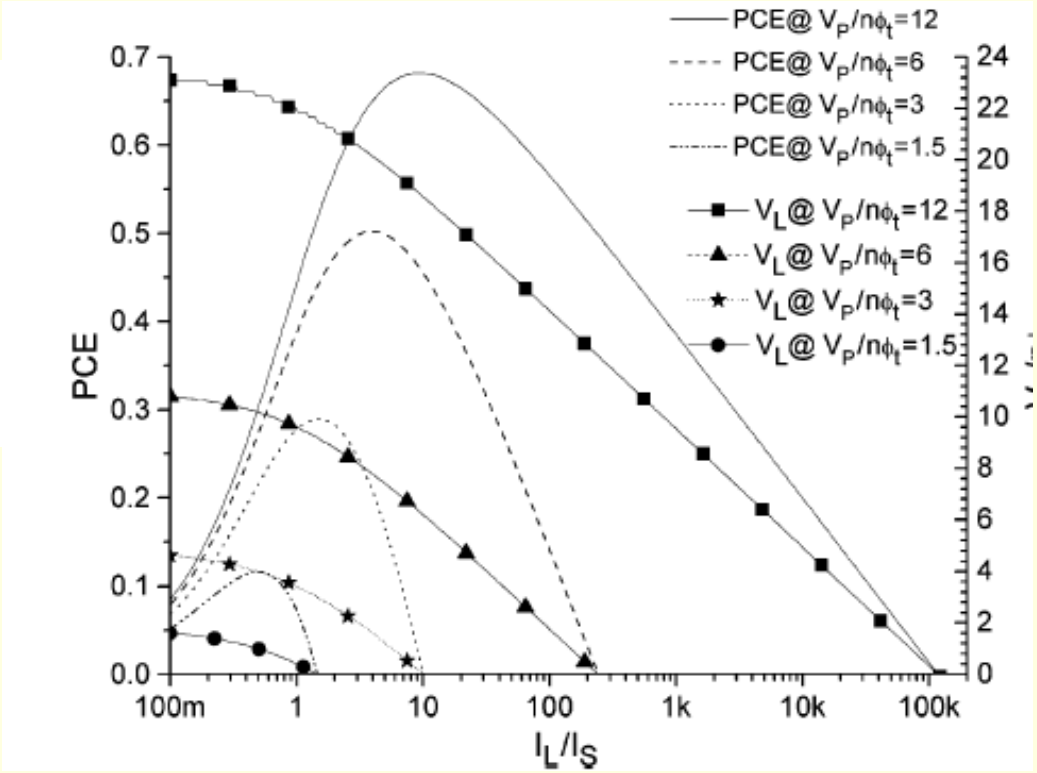




The voltage doubler

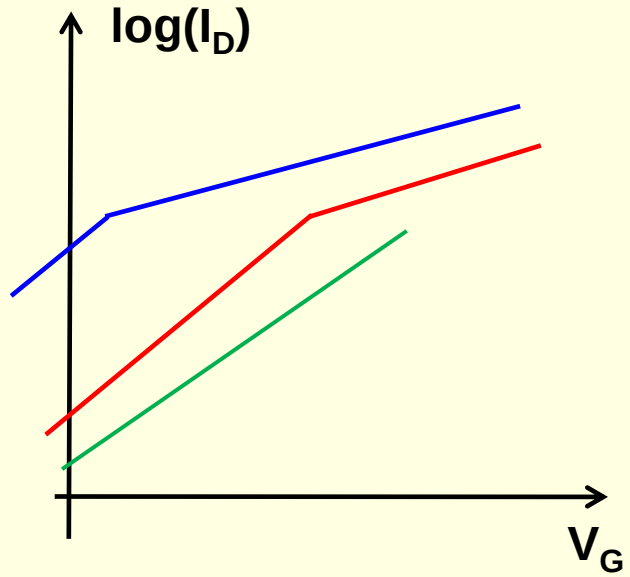
$$\mathrm{PCE} = \frac{P_{\mathrm{out}}}{P_{\mathrm{out}} + P_{\mathrm{loss}}} \cong \frac{1 - \frac{n\phi_t}{V_P} \ln\left[2(1 + I_L/I_S)\right]}{(1 + I_S/I_L)}.$$





Power conversion efficiency and load voltage of the voltage doubler versus normalized load current

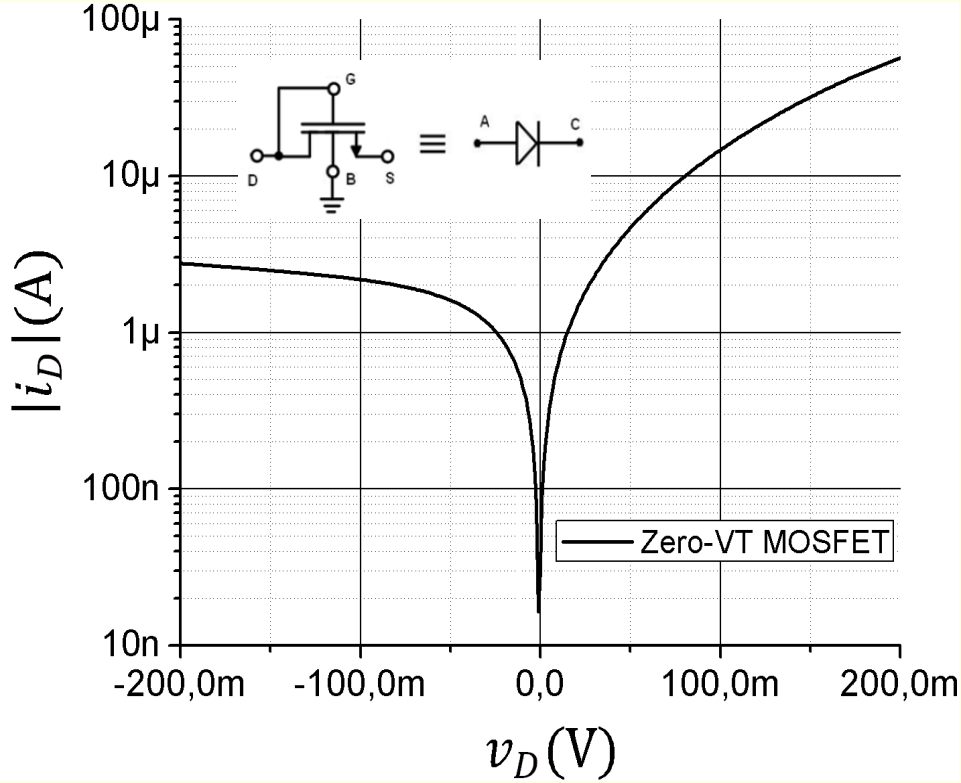
What about diodes?



Low (zero)-VT

Standard-VT

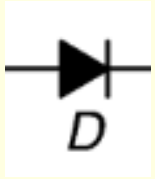
pn junction

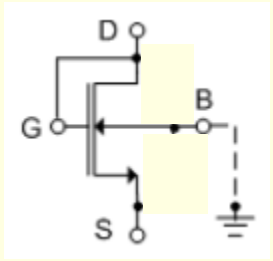


Diode-connected zero-VTMOSFET

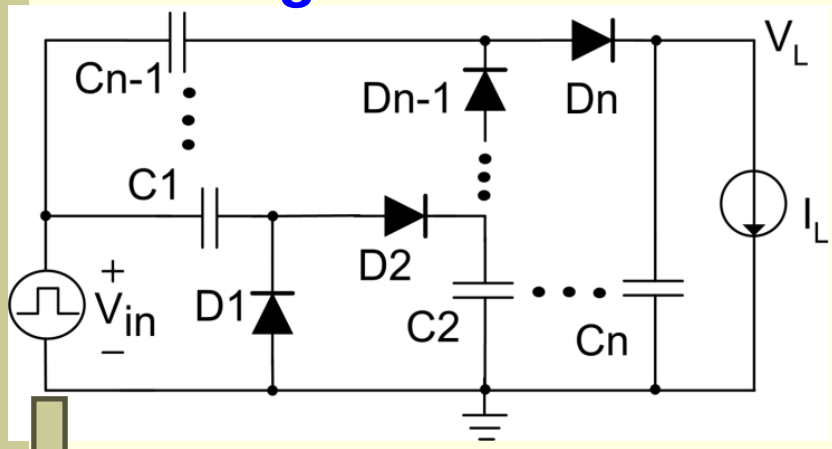
- high drive capability

AC/DC converter in 130 nm CMOS technology

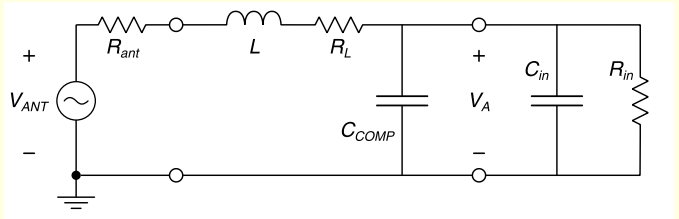


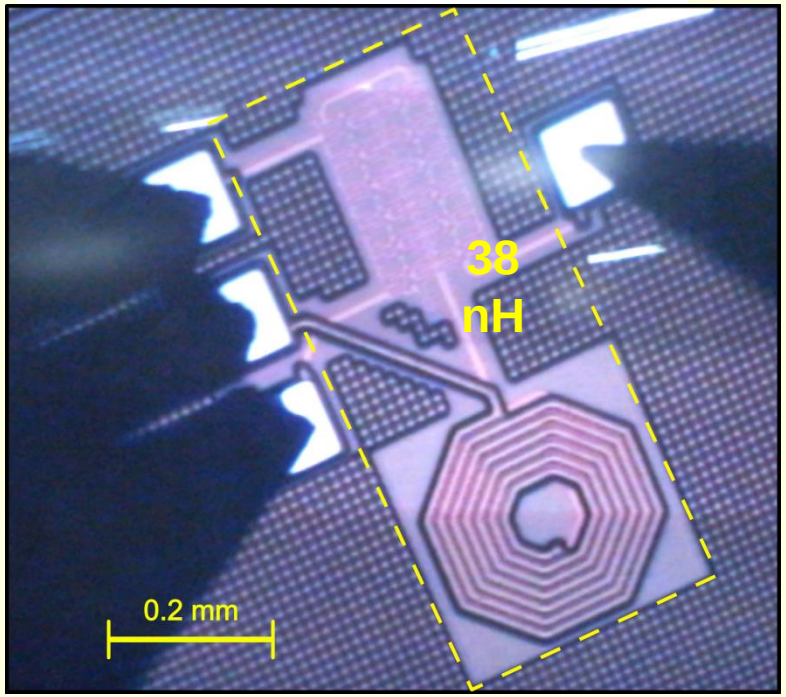


24-stage rectifier



Matching network





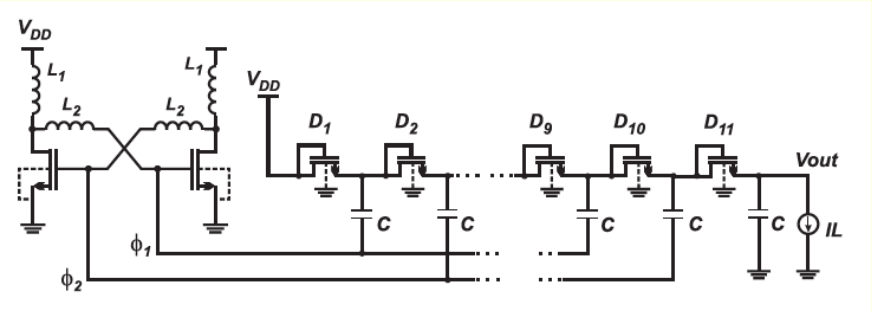
$P_{AV} \cong 10\ \mu W$ ⇨ $V_{in,peak} \cong 63\ mV$

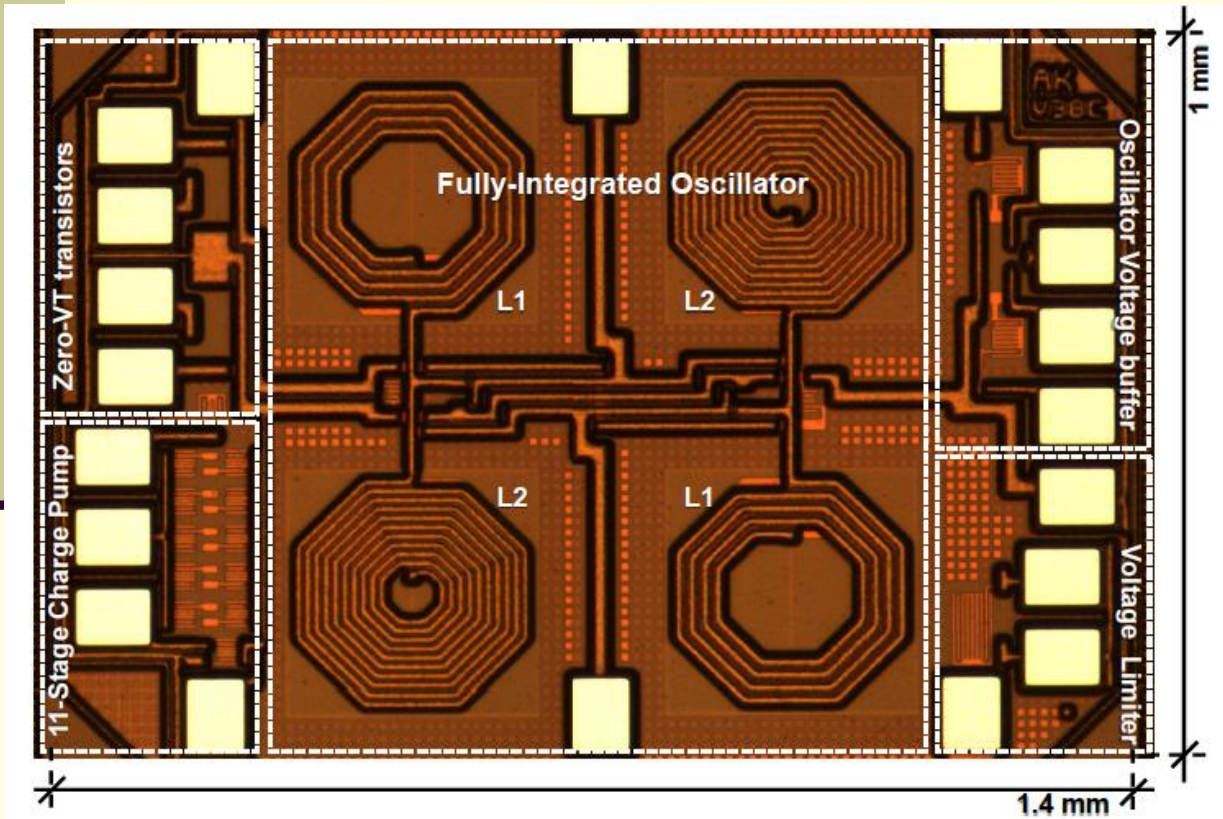
$V_L \cong 1\ V$ $I_L \cong 1\ \mu A$

$P_L = V_L I_L \cong 1\ \mu W$

$$\eta = \frac{P_L}{P_{AV}} \cong 10\%$$

Step-up converter





IBM 0.13 µm technology

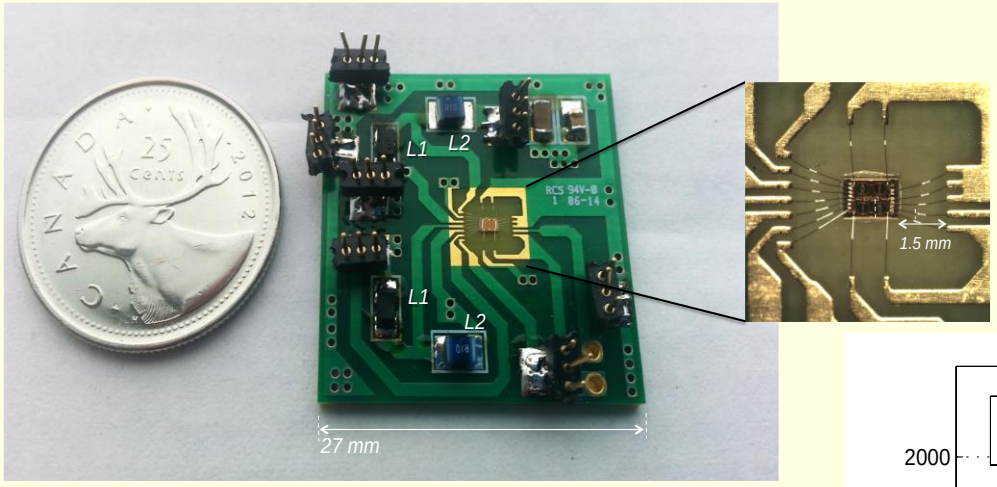
11-stage Dickson charge pump

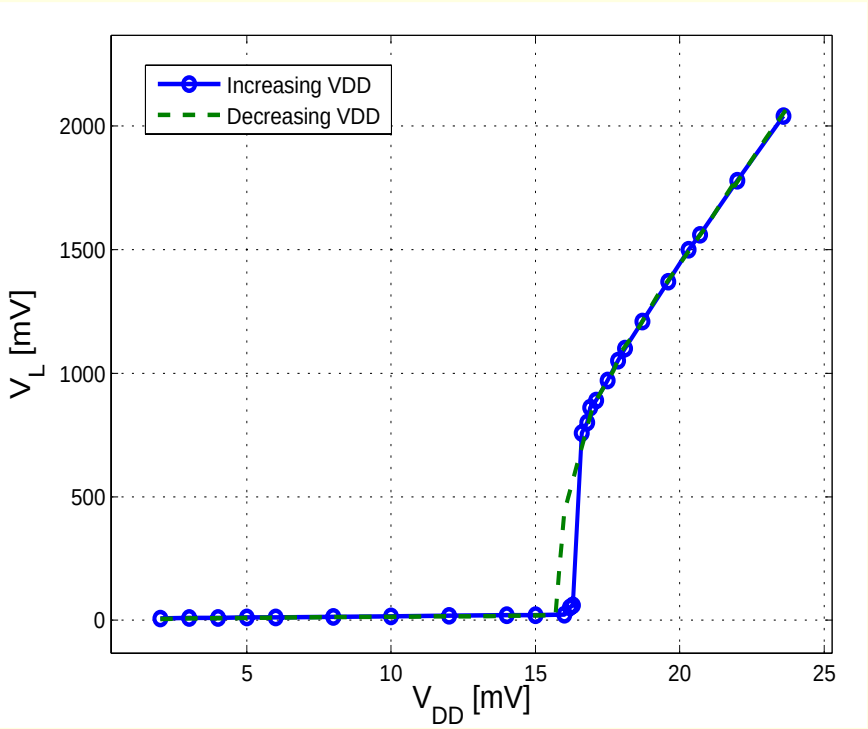
Zero-VT transistor as a diode
W/L=4.2µm/0.42µm
V_T=76.5 mV
Isat = 500 nA

2-stage ESRO

Zero-VT transistor
W/L=500µm/0.42µm
V_T=63 mV
Integrated inductors
L_1=18.8 nH, L_2 = 66 nH
Q ≈ 8

Wire-bonded prototype designed with off-chip inductors





Output voltage of the DC/DC converter for increasing and decreasing input voltages

Design parameters and experimental results for the ULV step-up converters

		Fully integrated design	Design with off-chip inductors
Design parameters	Oscillator	W/L = 500um/0.42um g_{md} = 7.08 mA/V L_1 = 18.8 nH, Q_{L1} = 8.7 L_2 = 66 nH, Q_{L2} = 8.1	W/L = 2000um/0.42um g_{md} = 19 mA/V L_1 = 220 nH, Q_{L1} = 58 L_2 = 594 nH, Q_{L2} = 67
	Charge Pump	W/L = 4.2 um/0.42um I_S = 550 nA; n = 1.4 C = 2 pF	W/L = 4.2 um/0.42um I_S = 550 nA; n = 1.4 C = 2 pF
Experimental results	f_{osc}	*550 MHz*	*50 MHz*
	Active area	*1 mm²*	*20 mm²*
	Start-up at I_L=10nA; V_l=1V	$V_{DD,min}$ = 77.6 mV	$V_{DD,min}$ = 17.4 mV
	At I_L=1uA; V_L=1V	V_{DD} = 86 mV	V_{DD} = 23 mV
	At V_{DD}=50mV; V_L=1V	-	I_L = 9.4 uA PCE = 9.4%
	At V_{DD}=0.1V; V_L=1V	I_L = 3.3 uA PCE = 1 %	I_L = 30 uA PCE = 6.2 %

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- M. B. Machado *et al.* "Analysis and design of the Dickson charge pump for sub-50 mV energy harvesting," Microelectronics Journal, August 2019.
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Summary

Minimum V_{DD} for voltage gain =-1

Inverter	Stacked Inverter	Standard ST
$2\varphi_t \ln 2 =$ 36 mV at 300 K	$2\varphi_t \ln 1.77 =$ 29.8 mV at 300 K	$2\varphi_t \ln\left(\frac{8+\sqrt{73}}{9}\right) =$ 31.5 mV at 300 K

Minimum V_{DD} for hysteresis

Three-Inverter ST	Standard ST
$2\varphi_t \ln 2$=36 mV at 300 K	$2\varphi_t \ln\left(2+\sqrt{5}\right)=$ 75 mV at 300 K

z

NMOS Oscillators

Minimum V_{DD} for oscillation

Cross-coupled	Enhanced-Swing Cross-Coupled	Enhanced-Swing Colpitts
$\varphi_t \ln(1+n)$	$\varphi_t \ln[1+nL_1/(L_1+L_2)]$	$\varphi_t \ln[1+C_2/C_1/(1+L_1/L_2)]$
	L_1 - load capacitance L_2- coupling capacitance	L_1, L_2 - drain and souce capacitances