Charge-based transistor models facilitate the IC design process and the designer education

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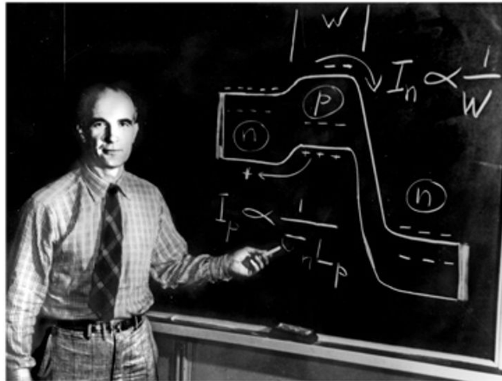
https://lci.ufsc.br/

https://github.com/ACMmodel/MOSFET_model

Outline

- Introduction: BJTs vs MOSFETs
- ACM2.0 model
- Parameter extraction & model validation
- Circuit examples

BJTs vs. MOSFETs: history in a nutshell

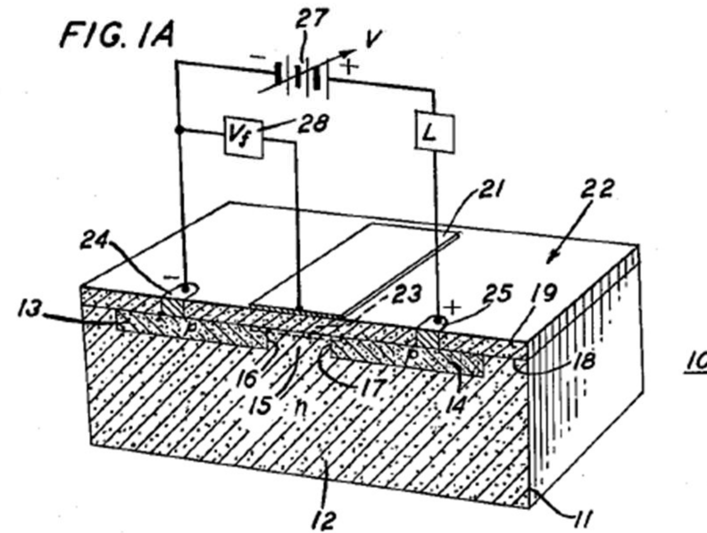


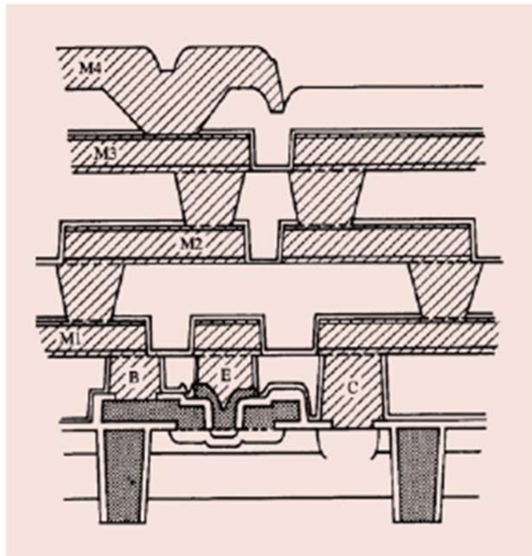
1948: conception of the bipolar transistor

Aug. 27, 1963 DAWON KAHNG 3,102,230

ELECTRIC FIELD CONTROLLED SEMICONDUCTOR DEVICE

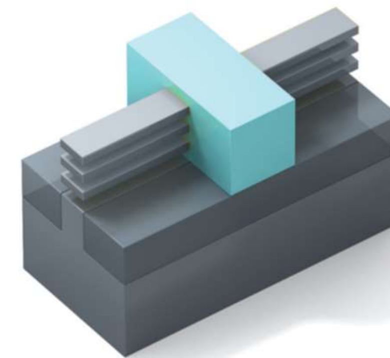
Filed May 31, 1960





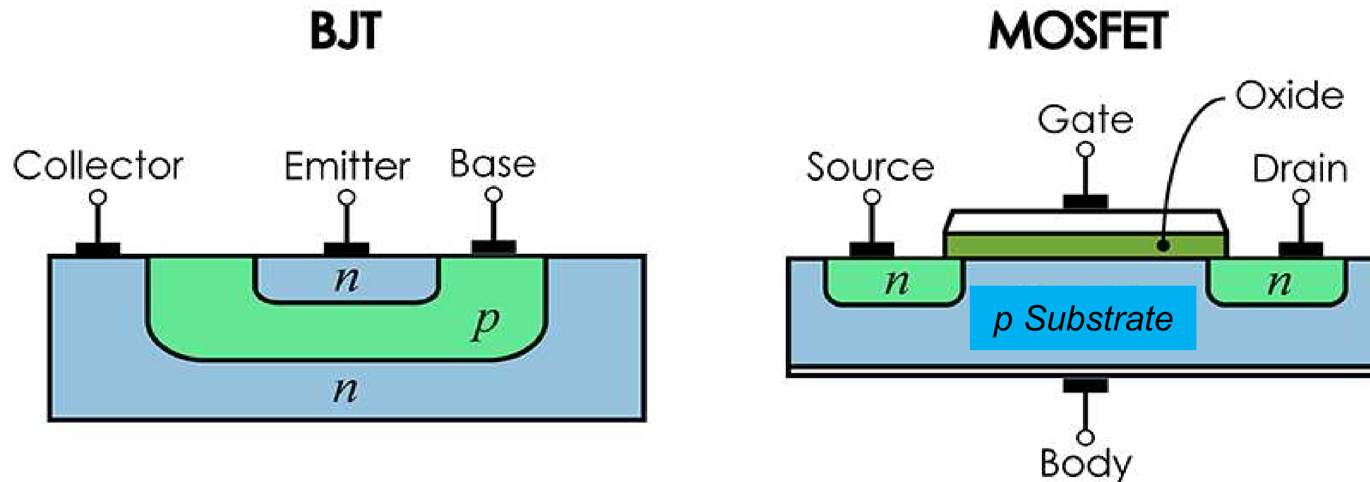
1990: IBM announce ES/9000 last family of mainframes in bipolar technology

T. Ning, EDM June 2023



Cutting-edge RibbonFET

BJTs vs. MOSFETs: structural differences



BJT transconductance

$$g_m = \frac{\partial I_C}{\partial V_B}$$

Gate, source and drain transconductances

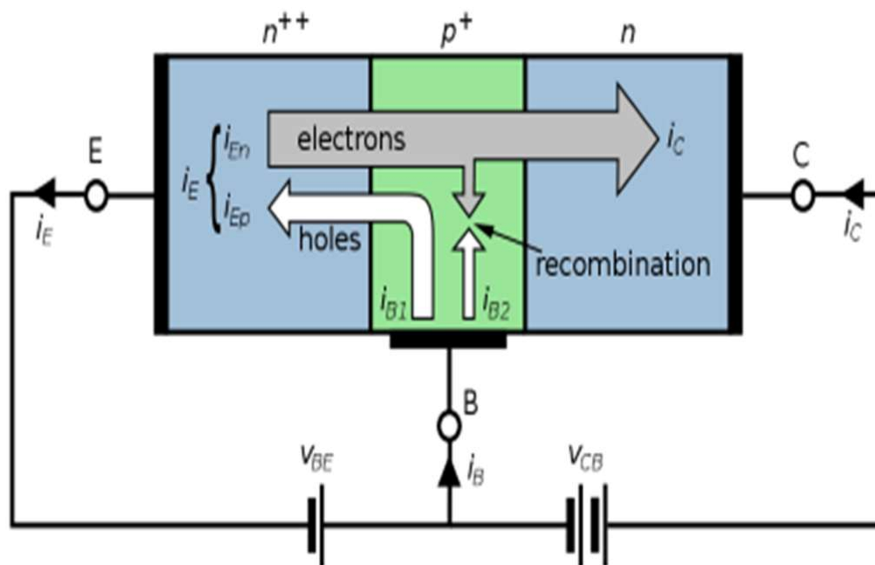
$$g_m = \frac{\partial I_D}{\partial V_G} \quad g_{ms} = -\frac{\partial I_D}{\partial V_S} \quad g_{md} = \frac{\partial I_D}{\partial V_D}$$

The body effect reduces the gate transconductance with respect to the source transconductance.
n is the slope factor.

$$g_m = \frac{g_{ms} - g_{md}}{n}$$

n ranges from ~ 1.1 to 1.5 in bulk technologies

BJT: essentially a unidimensional device

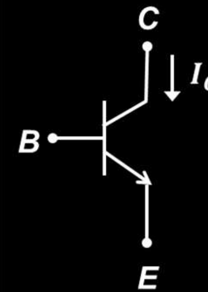


I_0 saturation current

q_b normalized base charge

φ_t thermal voltage 26 mV @ 300K

Gummel-Poon model:



$$I_C = I_0 \frac{e^{\frac{V_{BE}}{\varphi_t}} - e^{\frac{V_{BC}}{\varphi_t}}}{q_b}$$

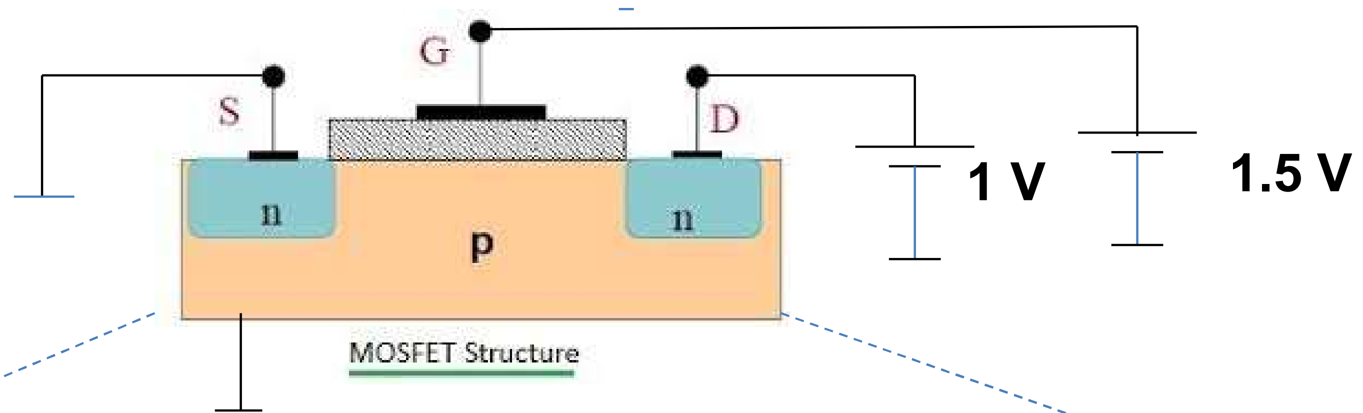
$$q_b = \sqrt{q_2 + \frac{q_1^2}{4}} + \frac{q_1}{2}$$

$$q_1 = 1 + \frac{V_{BC}}{V_{EF}} + \frac{V_{BE}}{V_{ER}}$$

$$q_2 = \frac{I_0}{I_{KF}}\left(e^{\frac{V_{BE}}{\varphi_t}} - 1\right) + \frac{I_0}{I_{KR}}\left(e^{\frac{V_{BC}}{\varphi_t}} - 1\right)$$

MOSFET: essentially a bidimensional device

X. Yang &
D. K. Schroeder
TED July 2012



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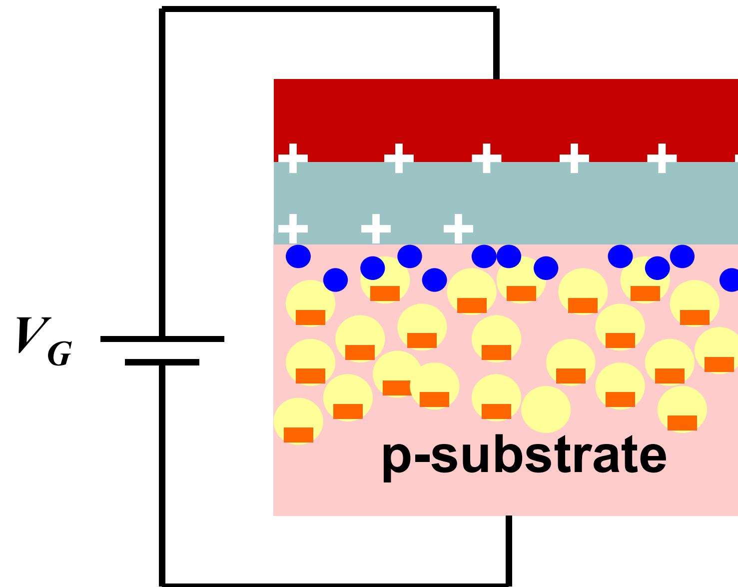
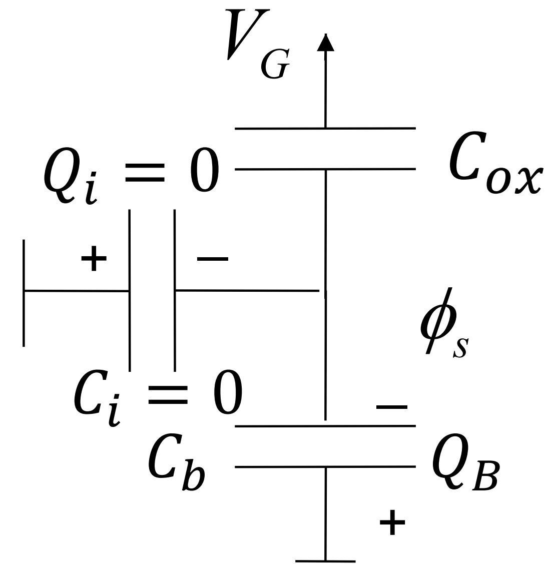
The capacitive model of the MOSFET





$$\frac{\Delta\phi_s}{\Delta V_G} = \frac{C_{ox}}{C_{ox} + C_b} = \frac{1}{n}$$

ϕ_s **surface potential**

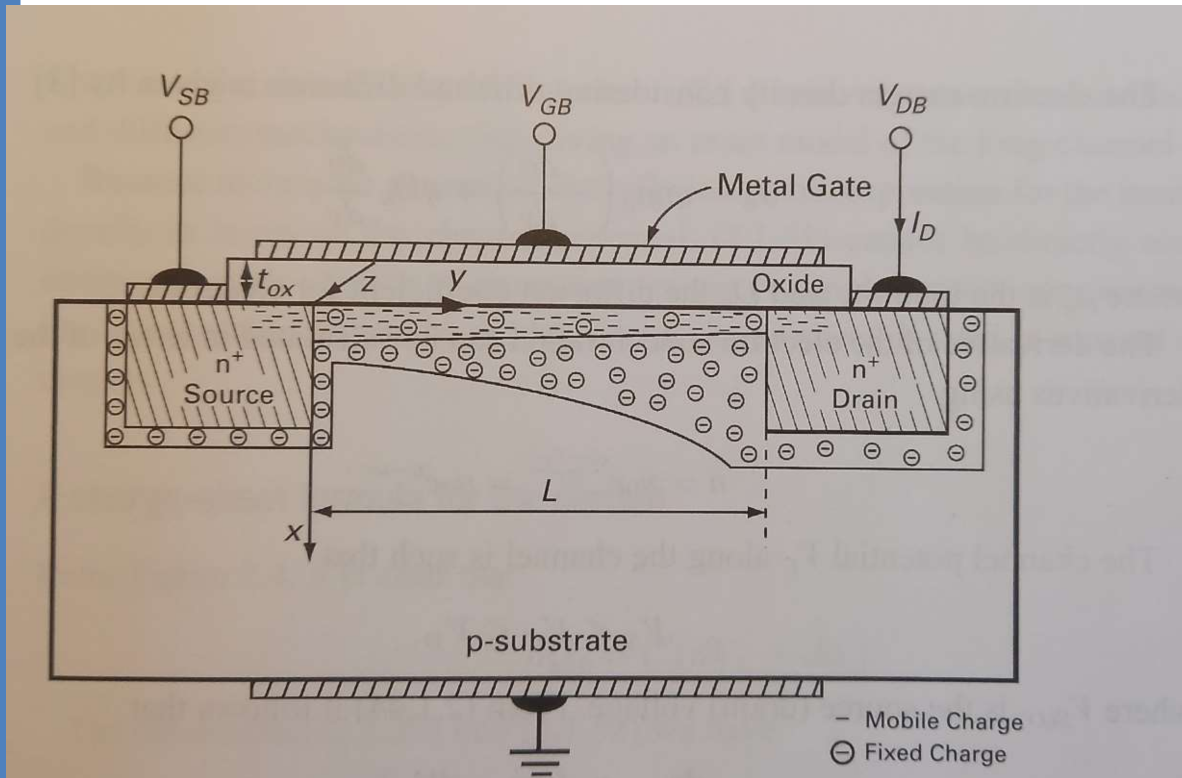
C_{ox} **oxide capacitance per unit area**

C_b **depletion capacitance per unit area**

Q_I **carrier charge density**

$$\phi_s = 2\phi_F + \frac{V_G - V_{T0}}{n} = 2\phi_F + V_P$$

Drain current model: main simplifications



- $dQ_I = nC_{ox}d\phi_s$

$$I_D = \mu W \left(-Q_I \frac{d\phi_s}{dy} + \phi_t \frac{dQ_I}{dy} \right)$$

drift **Diffusion**

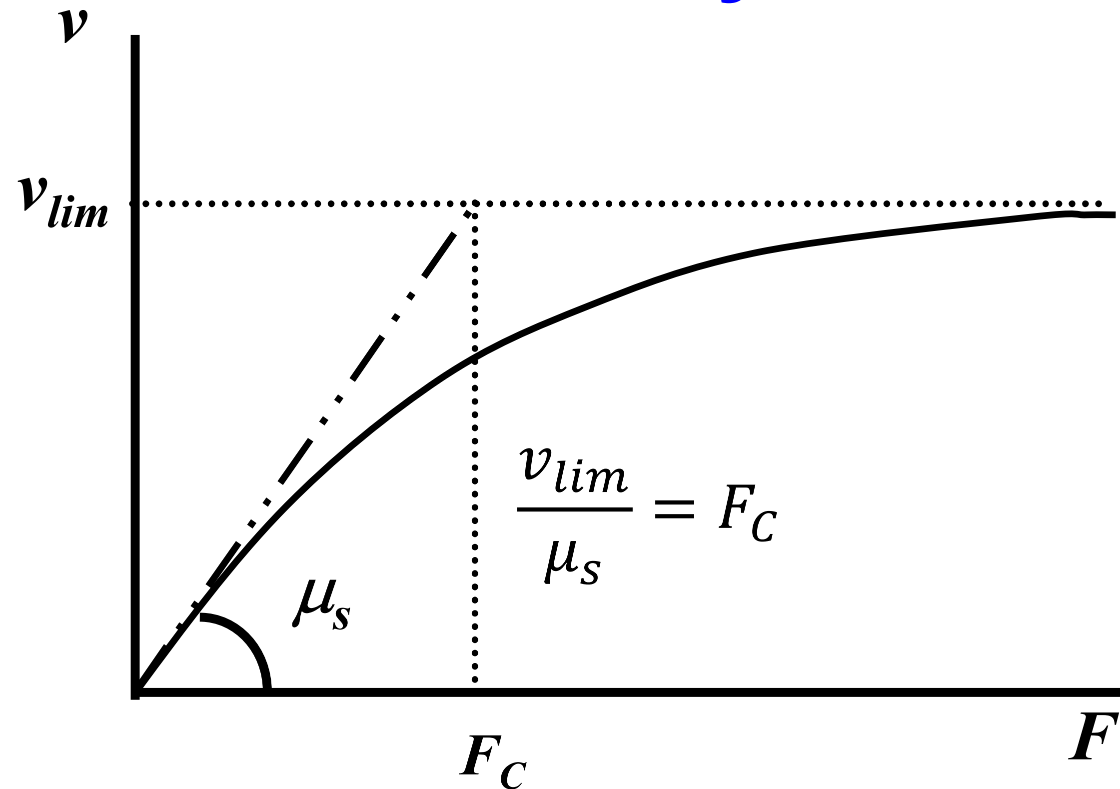
Q_I carrier charge density

W transistor width

μ carrier mobility

ϕ_t thermal voltage
26 mV @ 300K

Velocity saturation



ϕ_S: surface potential

F: longitudinal electrical field

$$\frac{d\phi_S}{dy} = -F$$

$$\mu = \frac{\mu_S}{1 + \frac{\mu_S}{v_{lim}} \frac{d\phi_S}{dy}}$$

Allows analytical integration for I_D

Velocity saturation effects

Normalized current vs. normalized charge densities at source and drain

$$i_D = \frac{(q_S + q_D + 2)}{1 + \zeta(q_S - q_D)}(q_S - q_D)$$

$$i_D = I_D / I_S$$

$$I_S = \frac{W}{L}\mu_s n C_{ox} \frac{\phi_t^2}{2}$$

normalization (specific) current

$$q_{S(D)} = Q_{S(D)}/(-nC_{ox}\phi_t)$$

$-nC_{ox}\phi_t$ thermal charge

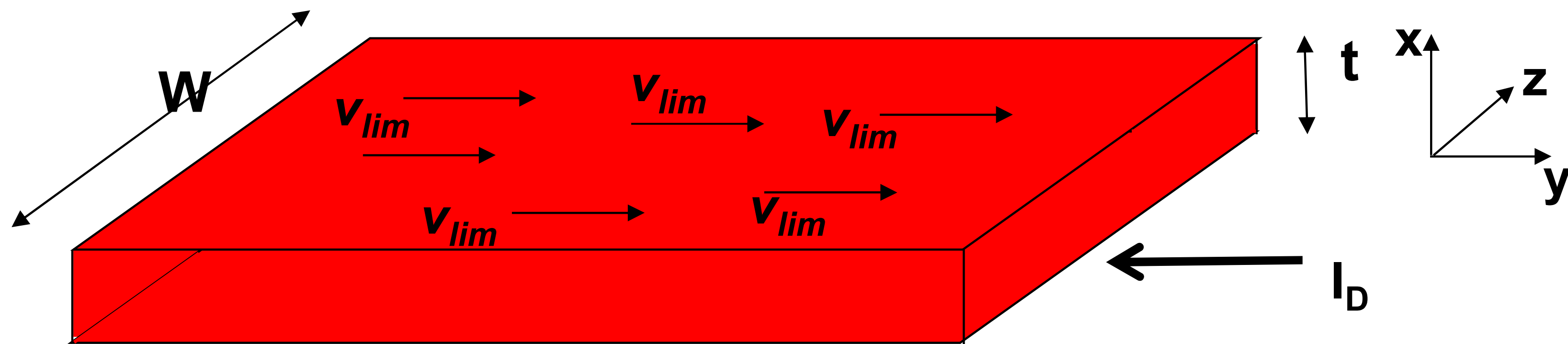
***SI* : $q_{S(D)}$ >> 1   *WI* : $q_{S(D)}$ << 1**

Short-channel parameter ζ :

$$\zeta = \frac{(\mu_s \phi_t / L)}{v_{lim}}$$

ratio of diffusion-related velocity to saturation velocity

Physics-based saturation



Saturation current due to saturation velocity of the carriers

$$I_{Dsat} = -WQ_{Dsat}\, v_{lim}$$

Q_{Dsat} is the saturation inversion charge per unit area

or, using normalized variables

$$i_{Dsat} = \frac{2}{\zeta} q_{dsat}$$

"Carrier velocity approaches v_{sat}, but never reaches v_{sat}"
Y.Taur TED March 2019

Physics-based saturation: design model

$$i_{Dsat} = \frac{2}{\zeta} q_{dsat} \qquad i_{Dsat} = \frac{(q_S + q_{Dsat} + 2)}{1 + \zeta(q_S - q_{Dsat})}(q_S - q_{Dsat})$$

$$q_{Dsat} = q_s + 1 + \frac{1}{\zeta} - \sqrt{\left(1 + \frac{1}{\zeta}\right)^2 + \frac{2q_S}{\zeta}}$$

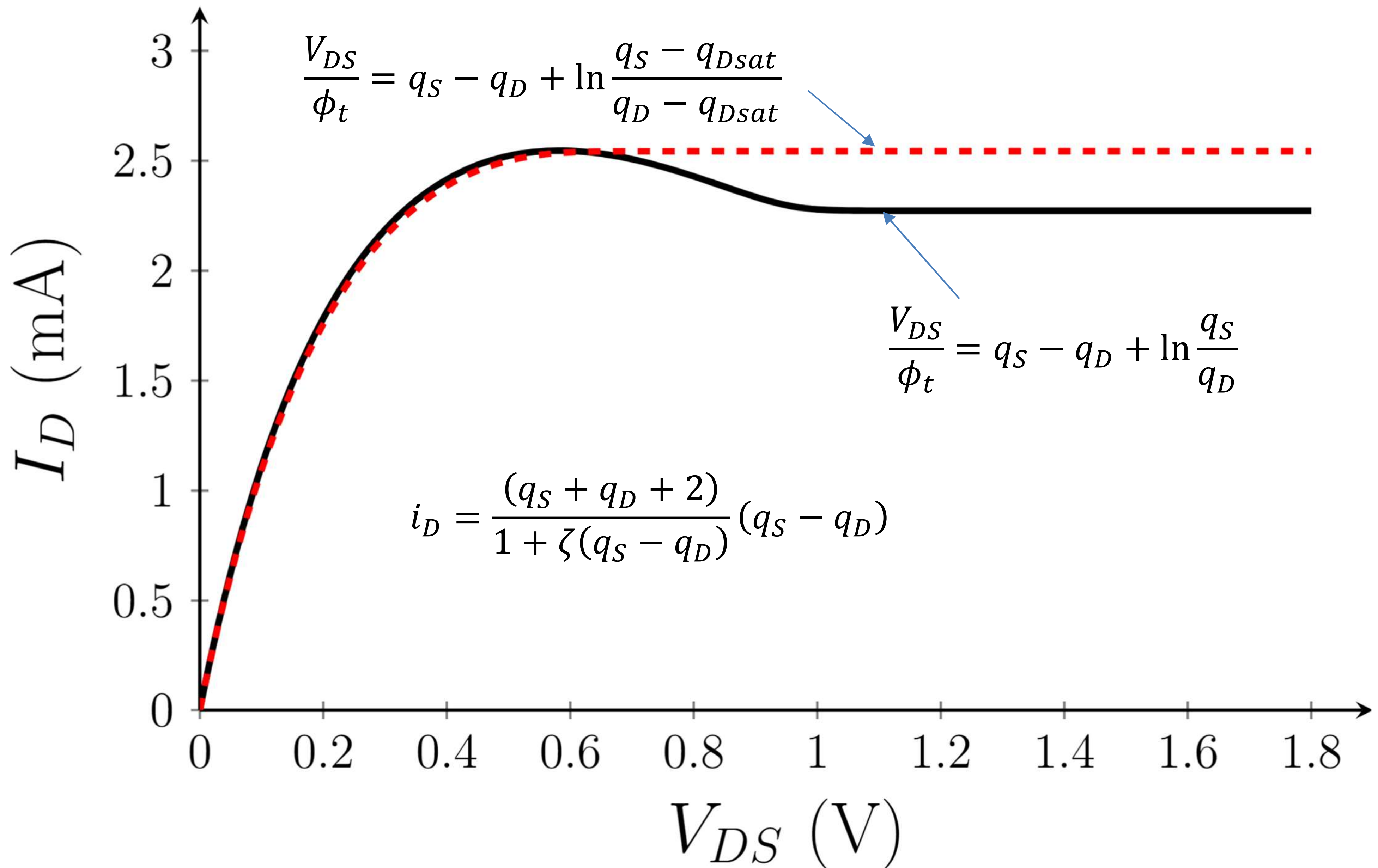
or equivalently

$$q_s = \sqrt{1 + \frac{2}{\zeta} q_{dsat}} - 1 + q_{dsat}$$

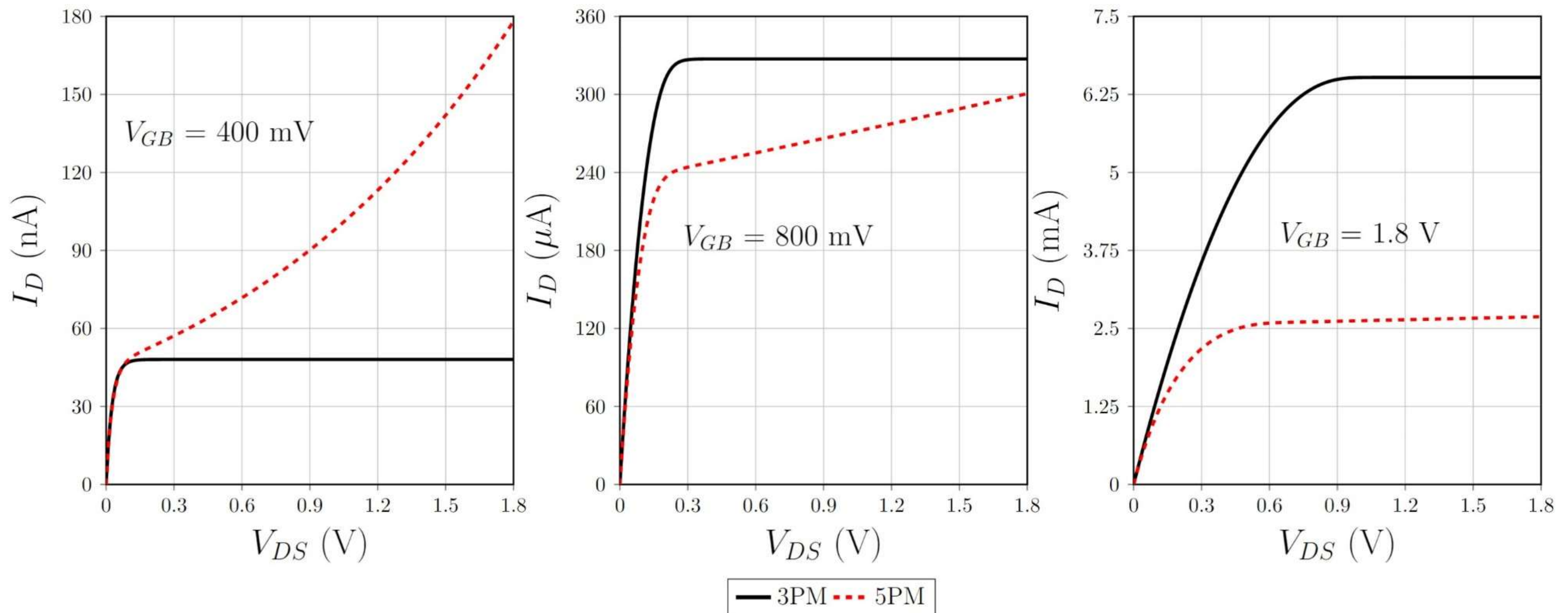
***U**nified **C**harge **C**ontrol **M**odel including the effect of velocity saturation*

$$\frac{V_P - V_{SB}}{\phi_t} = q_S - 1 + \ln q_S \qquad \frac{V_{DS}}{\phi_t} = q_S - q_D + \ln \frac{q_S - q_{Dsat}}{q_D - q_{Dsat}}$$

Effect of the maximum of $i_D(q_D)$ on the output characteristic $i_D(v_D)$



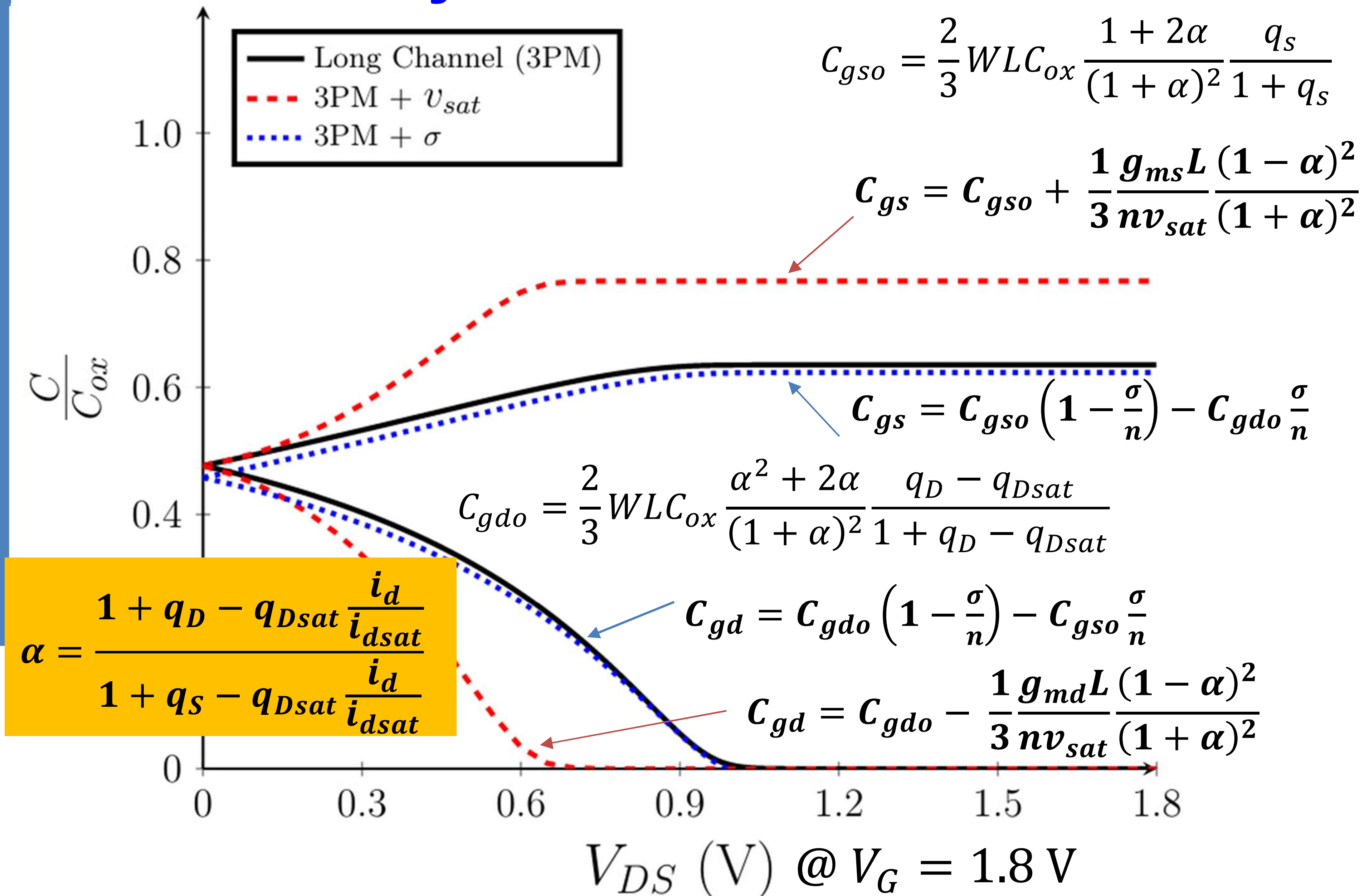
Output characteristics including DIBL and v_{sat}



$DIBL\ model$: $V_T = V_{T0} - \sigma(V_{SB} + V_{DB})$

Transistor	W/L $(\mu m/\mu m)$	V_{T0} (mV)	I_S (μA)	n	σ	ζ
NMOS2V	$\mathbf{5/0.18}$	528	5.52	1.37	0.025	0.056

Intrinsic capacitances including velocity saturation and DIBL



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V_T I_S and n extraction: the g_m/I_D method

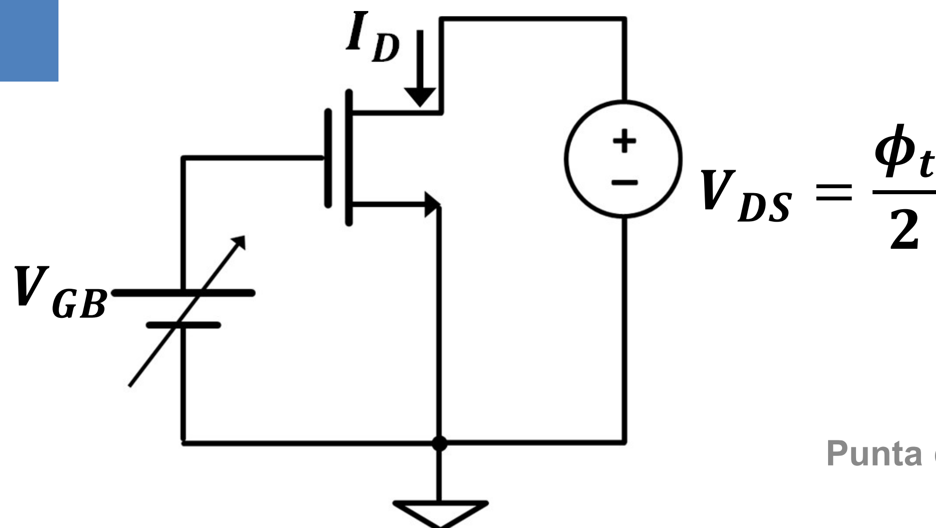
$$g_{ms} = \mu\frac{W}{L}nC_{ox}\phi_t q_S = \frac{2I_S}{\phi_t}q_S$$

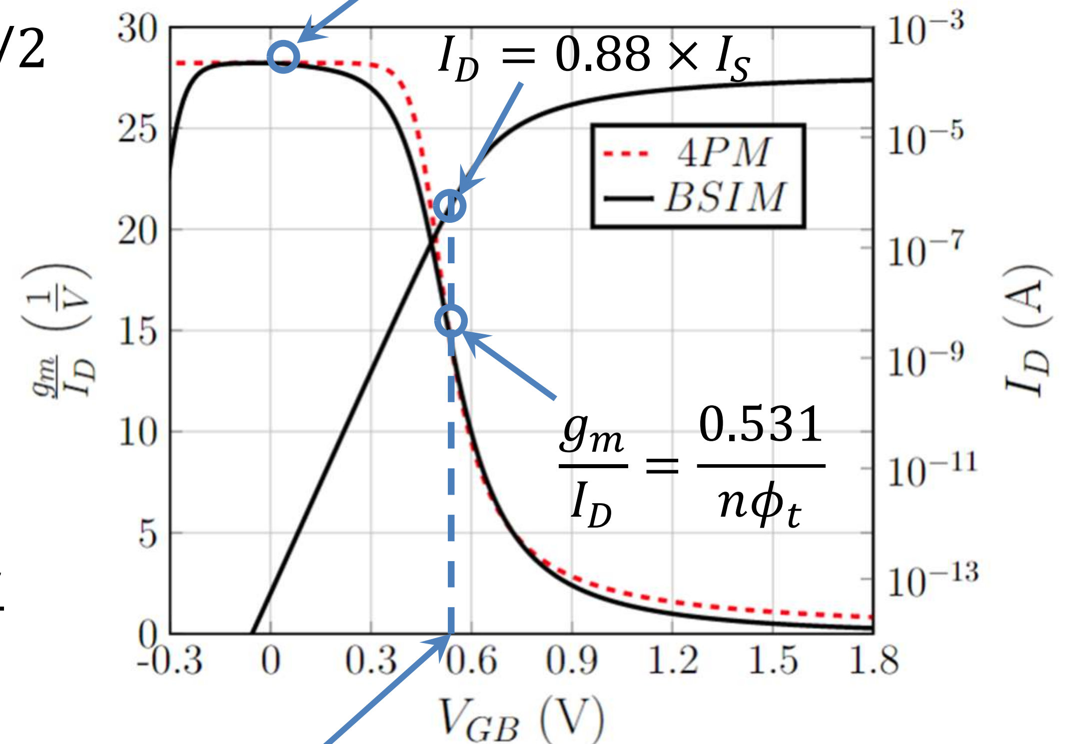
$$\left.\frac{g_m}{I_D}\right|_{V_{DS}\to 0} = \frac{1}{n\phi_t(1+q_S)}$$

Thus, at threshold ($q_S = 1$) g_m/I_D is at ½ of its maximum value,

$$\left(\frac{g_m}{I_D}\right)_{max} \cong \frac{1}{n\phi_t}$$

$$I_D(q_S = 1, V_{DS} = \phi_t/2) \cong g_{ms}\phi_t/2 = \frac{2I_S}{\phi_t}\phi_t/2 = I_S$$

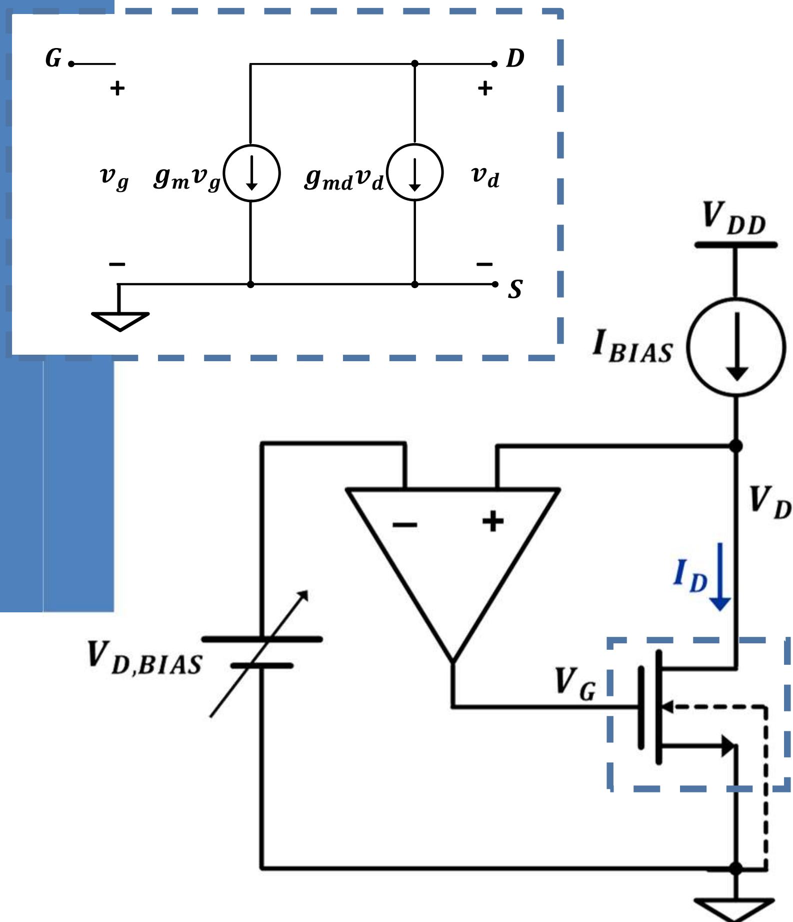


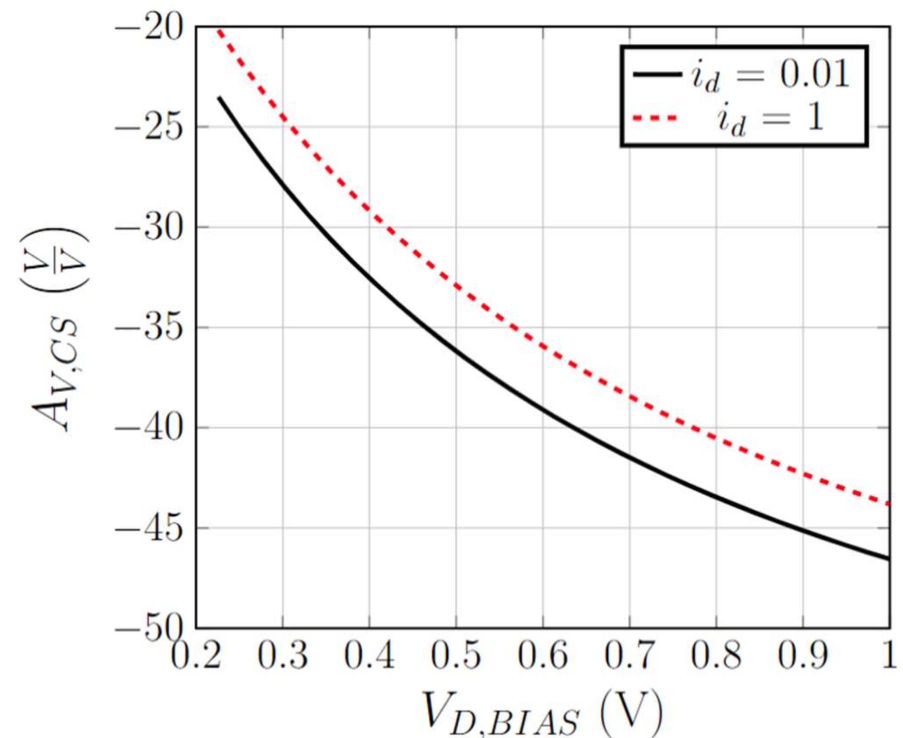


Extraction of σ in WI (MI) and saturation

Common-Source Intrinsic-Gain method

$$A_{V,CS} = \frac{v_d}{v_g} = -\frac{g_m}{g_{md}} = -\frac{1}{\sigma}$$

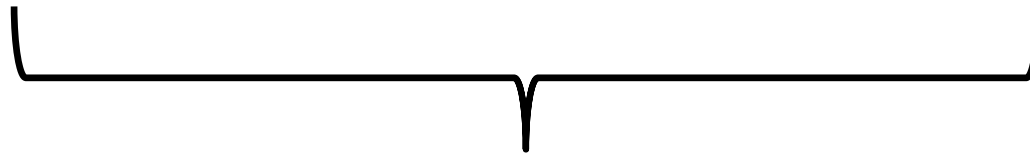




ζ extraction at $V_G = V_D = V_{DDmax}$

$$i_{dsat} = \frac{2}{\zeta} q_{dsat}$$

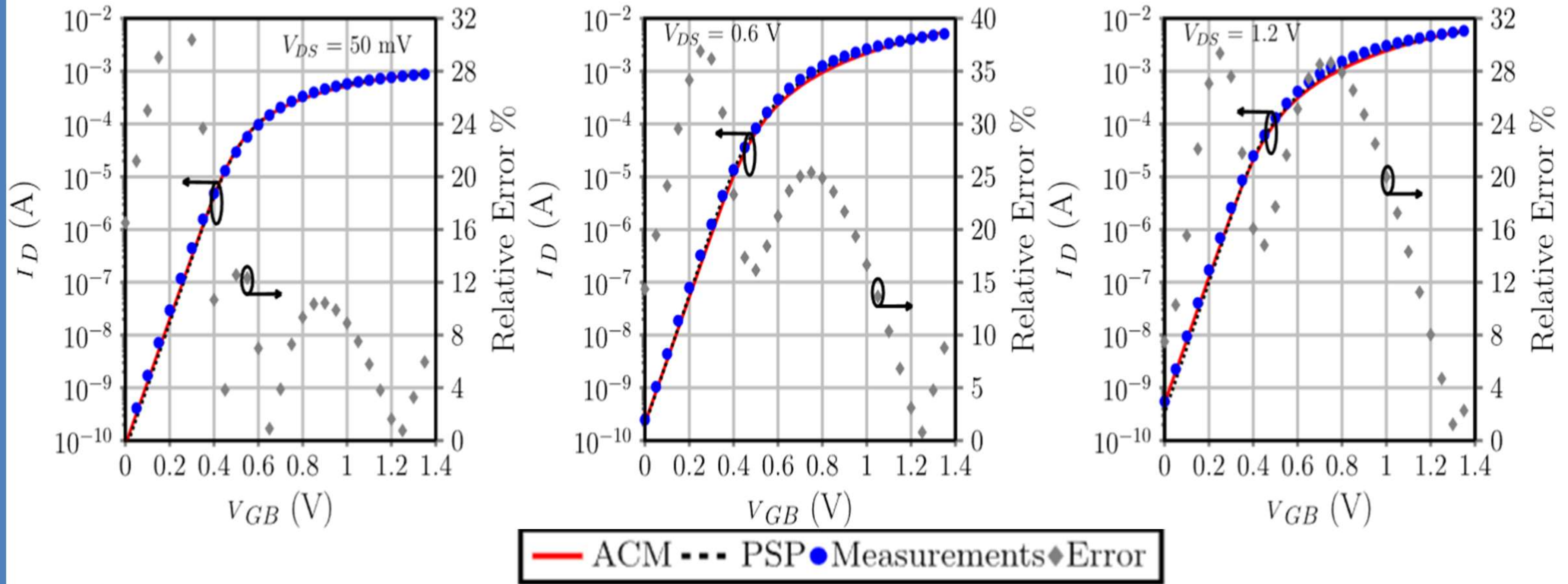
$$q_s = \sqrt{1 + \frac{2}{\zeta} q_{dsat}} - 1 + q_{dsat}$$



$$\zeta = \frac{2\left(q_s + 1 - \sqrt{1 + i_{dsat}}\right)}{i_{dsat}}$$

- q_s calculated using parameters (V_{T0} , n, σ) and UCCM.
  - *measure* $I_{Dsat}(V_G\ , V_D, V_S\ , V_B\ )$-> $i_{dsat} = I_{Dsat}/I_S$.
- Example: NMOS transistor, $V_G = V_D = V_{DDmax}$ and $V_S = V_B = 0$V.

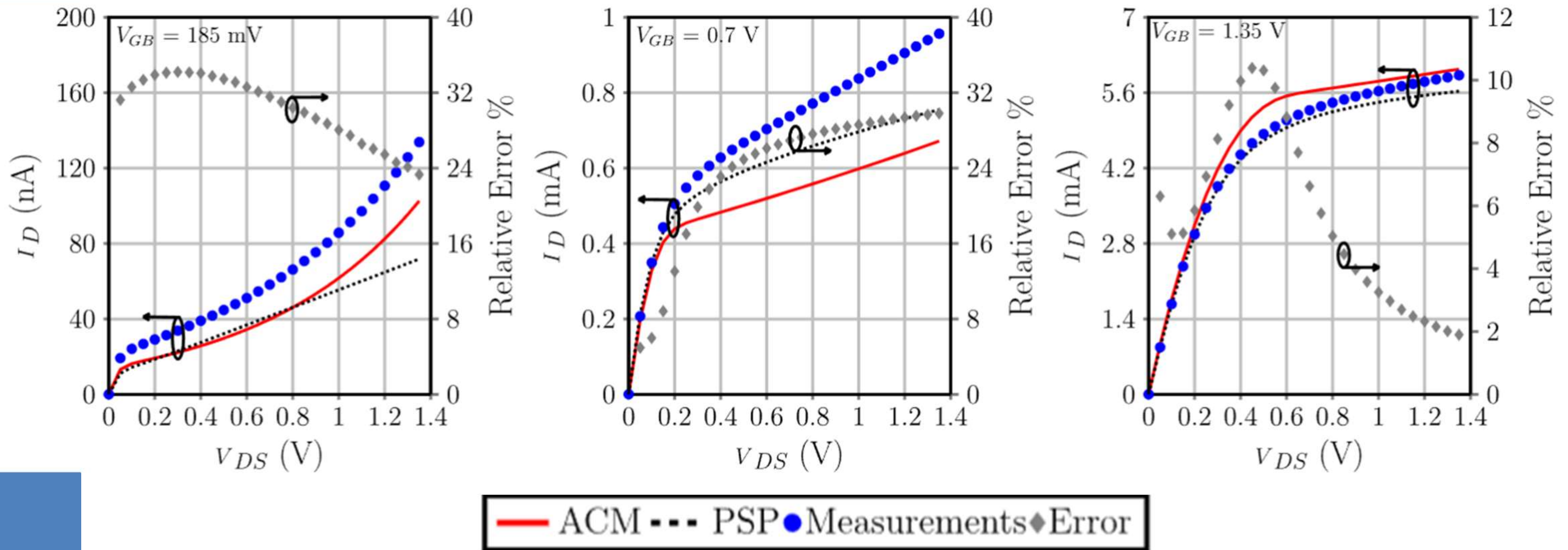
I_D vs V_{GB} - ACM-5PM vs PSP – 130 nm SiGe IHP[1]



Characteristics of an LVT NMOS bulk transistor with W /L = 10μm/ 120 nm.

[1] Institut for High-Performance Microelectronics (IHP) open-source PDK

I_D vs V_{DS} - ACM-5PM vs PSP – 130 nm SiGe IHP



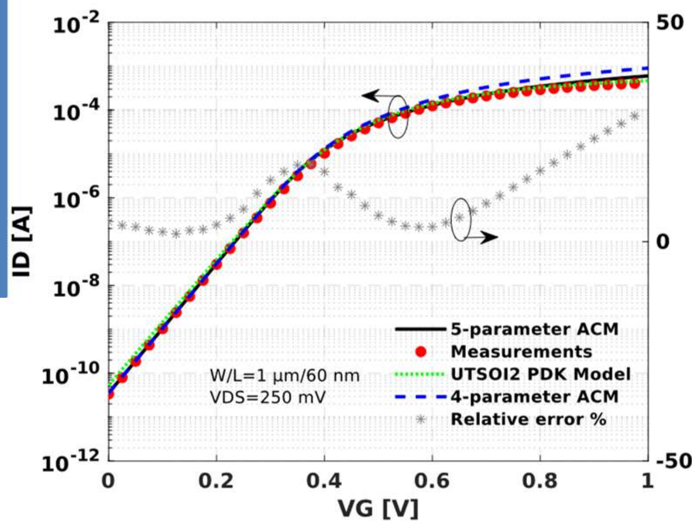
Characteristics for a LVT NMOS bulk transistor with W /L = 10μm/ 120 nm.

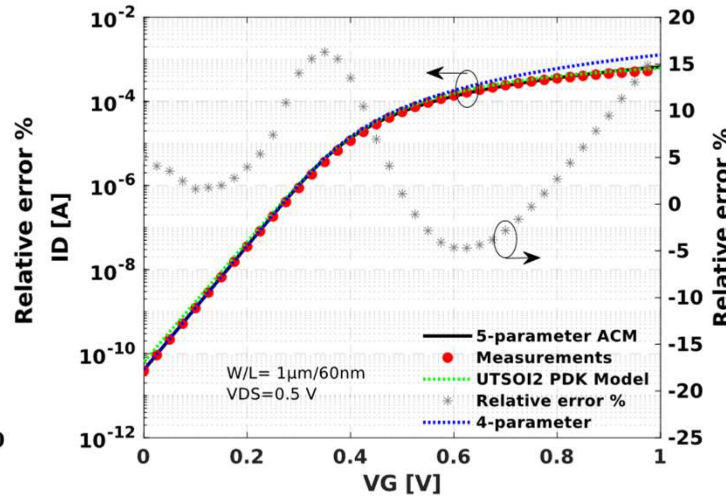
28 nm FD-SOI[2] technology DC characteristics

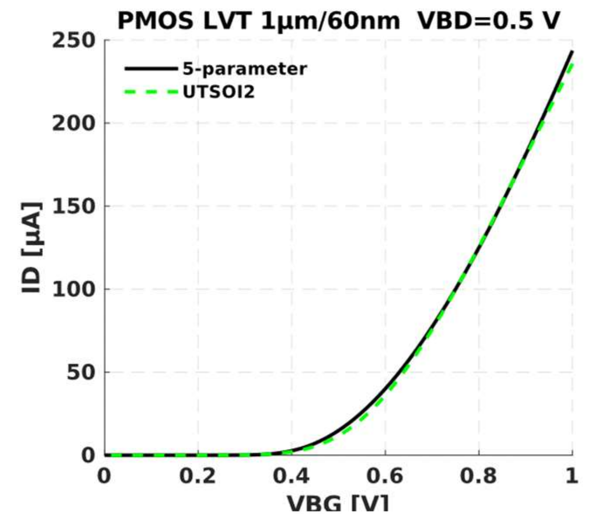
Parameter extraction for L=60 nm

Transistor	W/L	V_{T0} (mV)	I_S (μA)	n	σ	ζ
LVTNMOS	1µm/60 nm	390.5	3.25	1.138	0.018	0.039
LVTPMOS	1µm/60 nm	403.6	0.755	1.014	0.029	0.024

Model Verification: NMOS & PMOS TRANSISTORS







[2] ST Microelectronics

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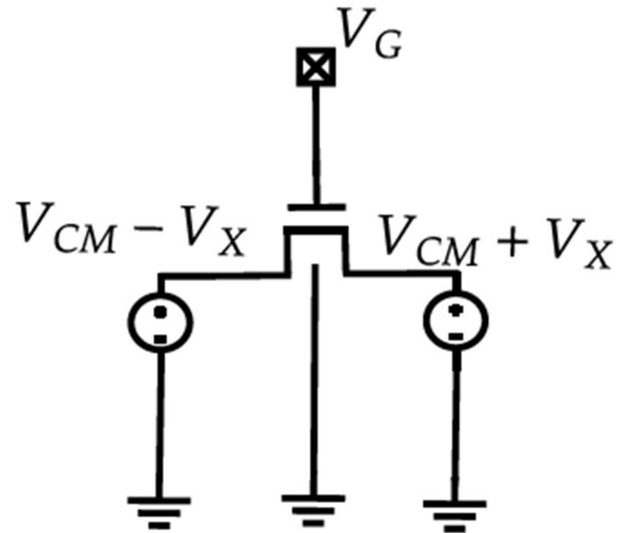
PSP Gummel symmetry test [3]



(a) I_x (mA)
(b) 1st deriv.
(c) 2nd deriv.
(d) 3rd deriv.
(e) 4th deriv.
(f) 5th deriv.

Meas
Existing PSP
PSP with C^∞ U_{ss} func, Vdsat smoothed
PSP with SCS (new)

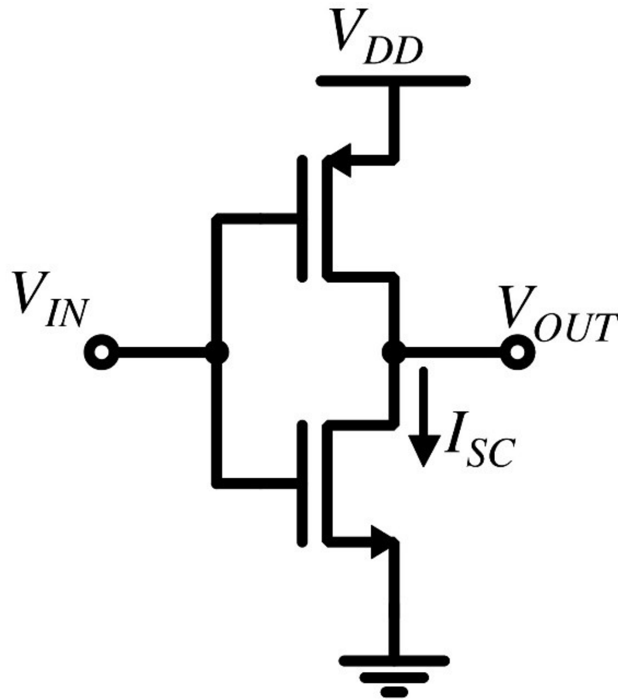
Issue of existing PSP
Still has bump with U_{ss}

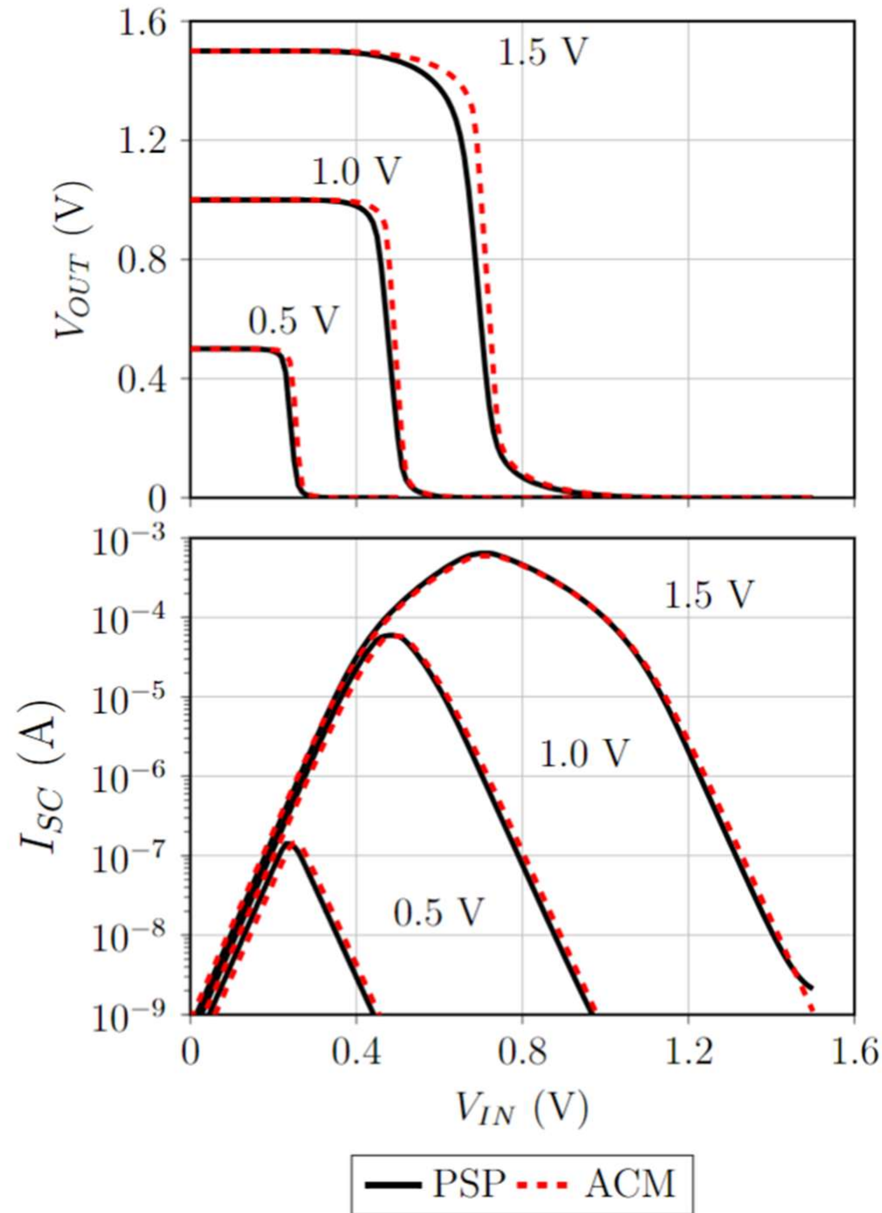
V_x (V)

[3] K. Xia TED Aug. 2020

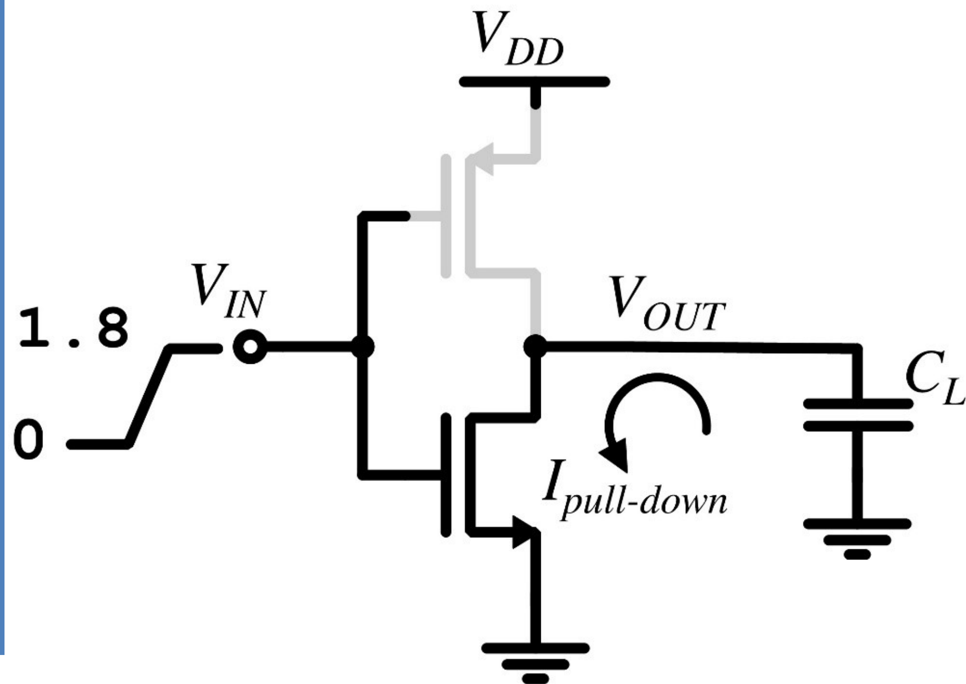
ACM2.0 Gummel symmetry test

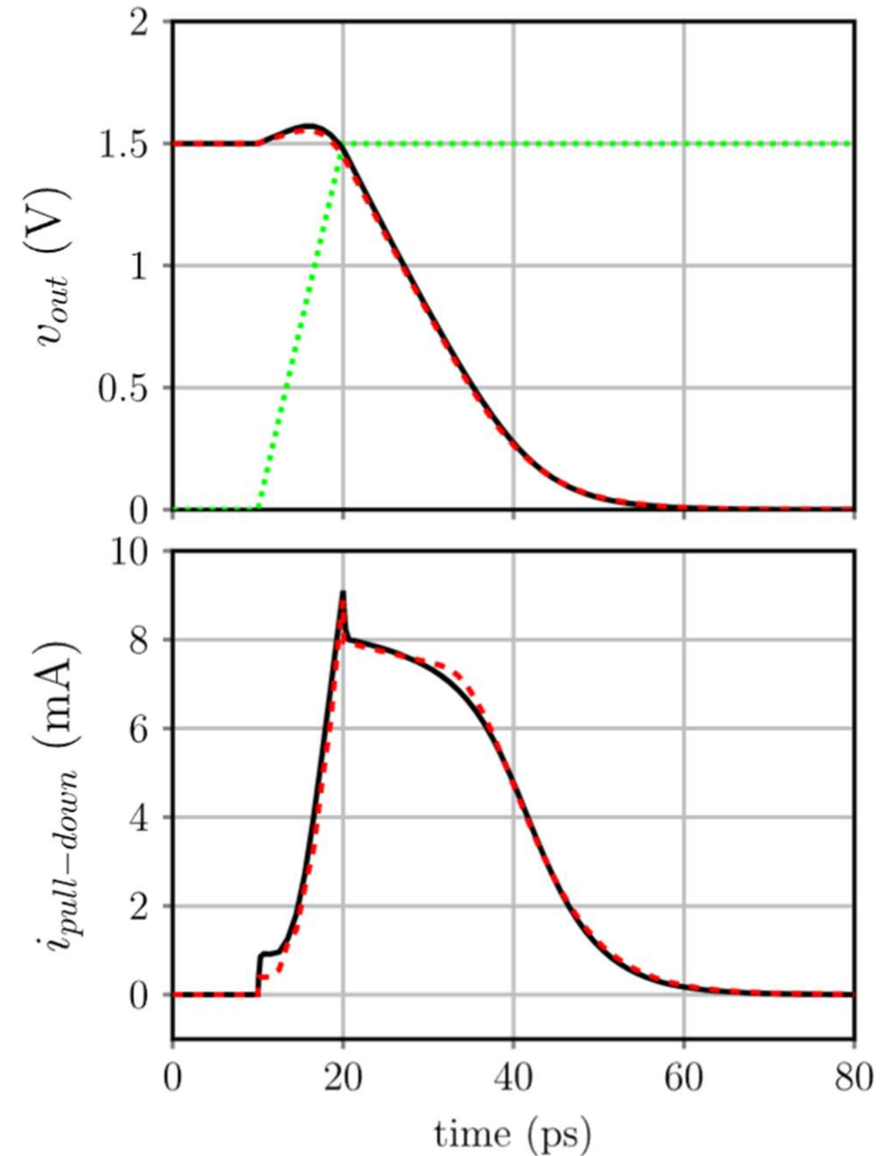
CMOS Inverter in 130 nm bulk VTC and short-circuit current



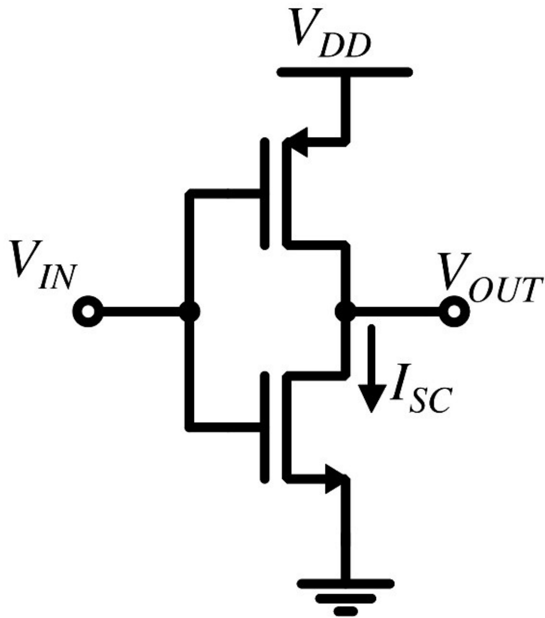


CMOS Inverter in 130 nm bulk
Output Voltage and pull-down current

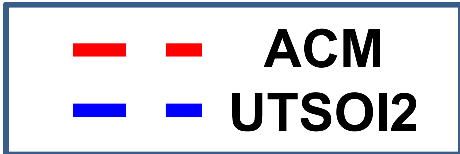


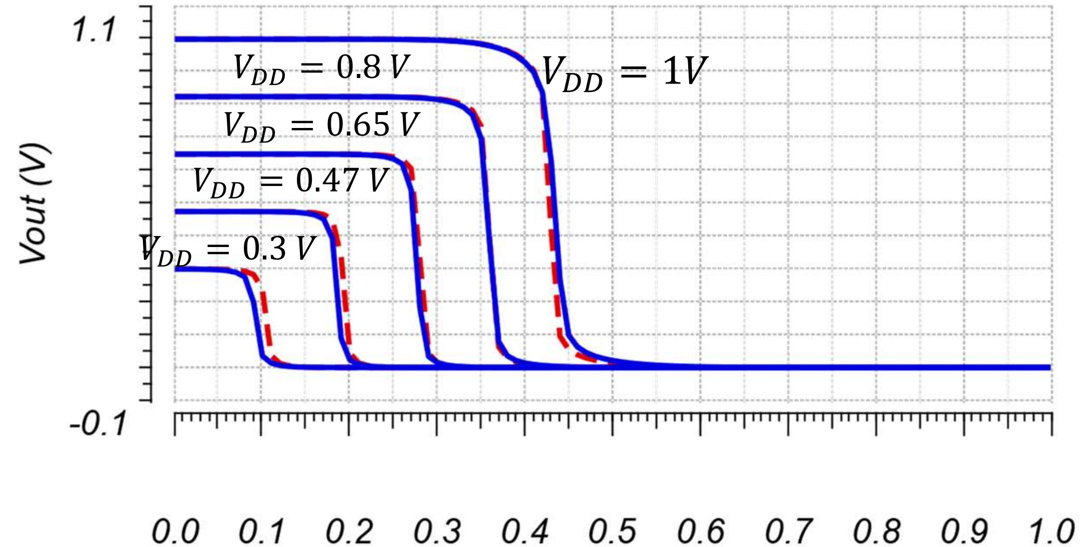


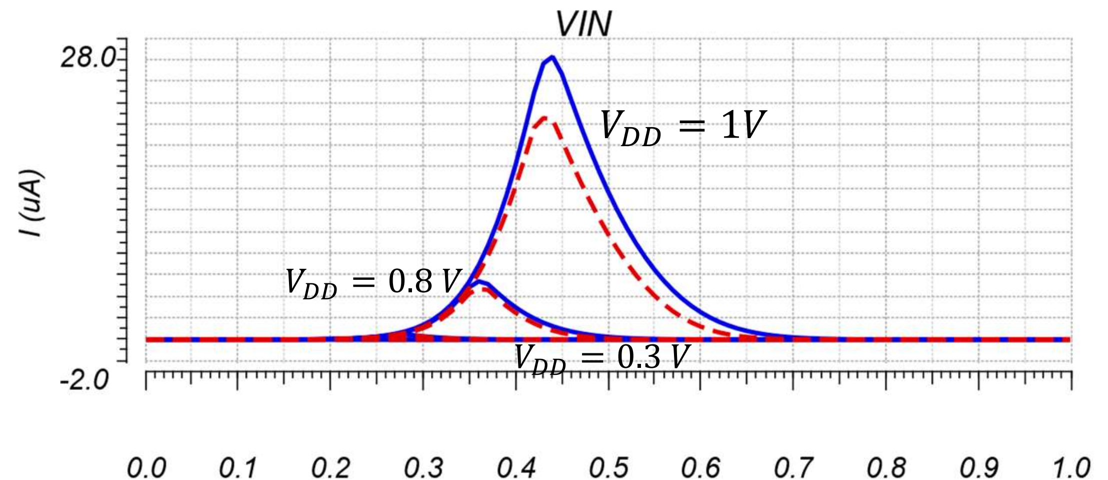
CMOS Inverter
VTC and short-circuit current in 28 nm FD-SOI



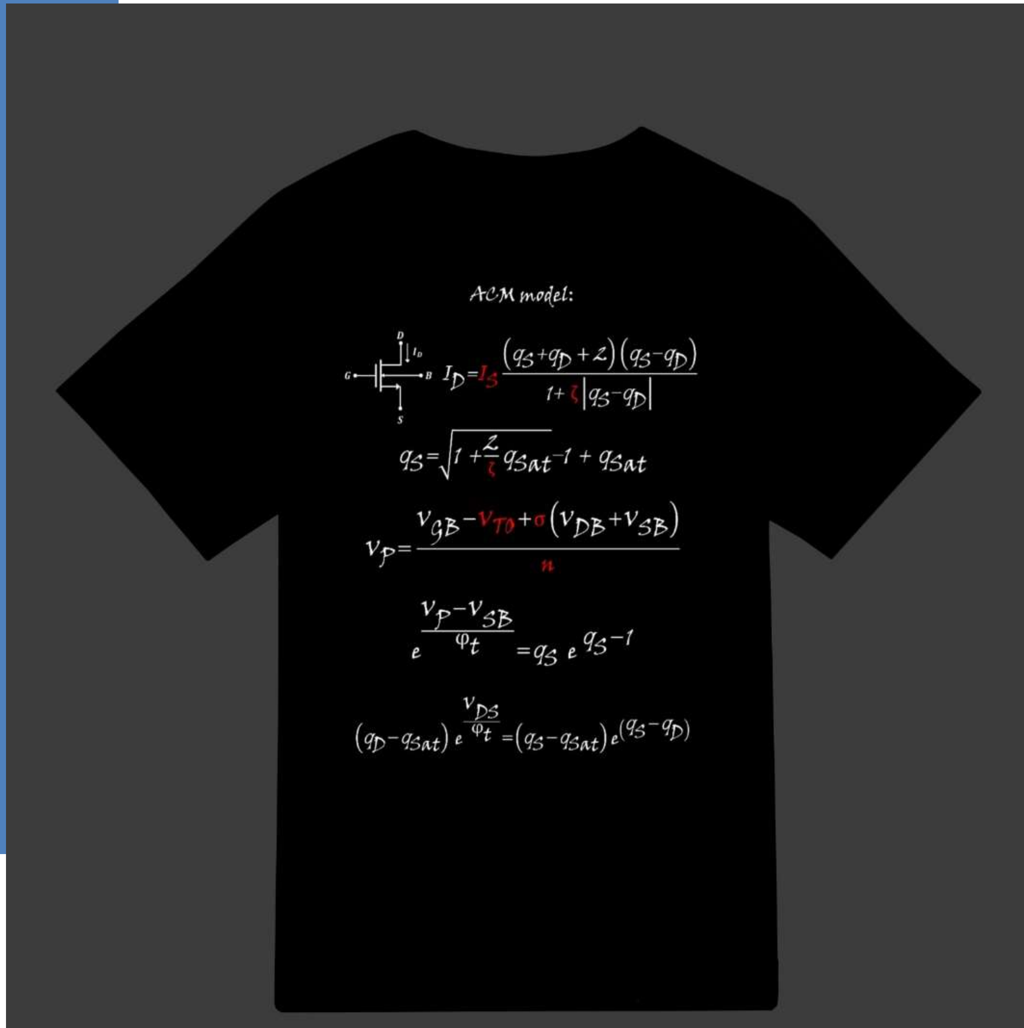
$W_n = W_p = 1\ \mu m$
$L_n = L_p = 60\ nm$







ACM2.0: Simple 5-DC-parameter MOSFET model



$$V_P = \frac{V_{GB} - \boldsymbol{V_{T0}} + \boldsymbol{\sigma}(V_{DB} + V_{SB})}{\boldsymbol{n}}$$

$$\frac{V_P - V_{SB}}{\phi_t} = q_s - 1 + \ln(q_s)$$

$$q_{dsat} = q_s + 1 + \frac{1}{\boldsymbol{\zeta}} - \sqrt{\left(1 + \frac{1}{\boldsymbol{\zeta}}\right)^2 + \frac{2q_s}{\boldsymbol{\zeta}}}$$

$$\frac{V_{DS}}{\phi_t} = q_s - q_d + \ln\left(\frac{q_s - q_{dsat}}{q_d - q_{dsat}}\right)$$

$$I_D = \boldsymbol{I_S} \frac{(q_S + q_D + 2)}{1 + \boldsymbol{\zeta}(q_S - q_D)}(q_S - q_D)$$

Acknowledgments

- LCI-UFSC, Florianopolis, Brazil
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- STIC-AmSud multinational program
- CAPES and CNPq agencies, Brazil
- LASCAS 2024 for the invitation

Live Demonstration: A 5-DC-parameter MOSFET model for circuit design and simulation using open-source EDA tools
Gabriel Maranhão, Deni Germano Alves Neto, Marcio Cherem Schneider, Carlos Galup-Montoro

A design-oriented single-piece short-channel MOSFET model
Deni Germano Alves Neto, Gabriel Maranhão, Marcio Cherem Schneider, Carlos Galup-Montoro