CMOS ANALOG DESIGN USING ALL-REGION MOSFET MODELING: PART I

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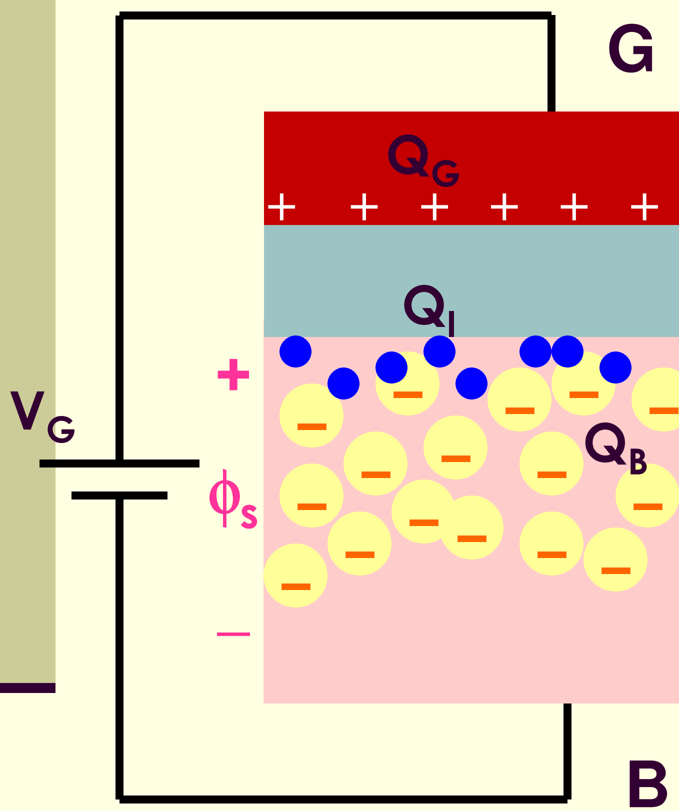
CONTENTS

- Two-terminal MOS structure
- Unified charge control model (UCCM)
- Drain current
- Pinch-off and threshold voltage
- Small-signal parameters
- Noise and mismatch compact models

TWO-TERMINAL MOS STRUCTURE



V_G gate-to-bulk voltage

C'_{ox} oxide capacitance per unit area

ϕ_s surface potential

Q'_I inversion charge per unit area

Q'_B bulk charge per unit area

V_{FB} flat-band potential

$$Q'_G = C'_{ox}\left(V_G - V_{FB} - \phi_s\right) = -(Q'_I + Q'_B)$$

MOSFET SMALL-SIGNAL EQUIVALENT CIRCUIT

$$C'_{gb} = \frac{dQ'_G}{dV_G}$$

$$C'_{gb} = \frac{1}{\dfrac{1}{C'_c} + \dfrac{1}{C'_{ox}}}$$

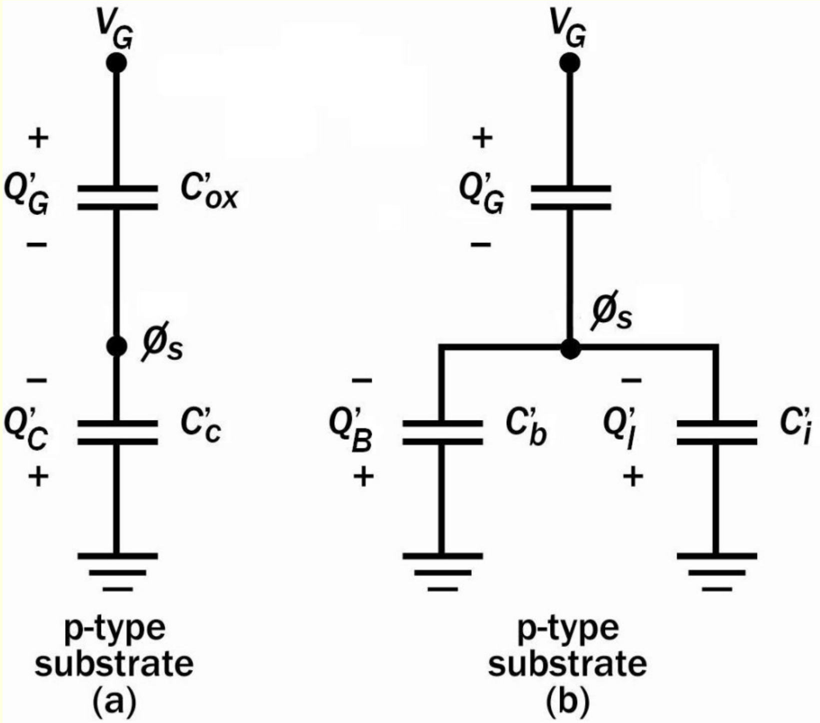
$$C'_c = C'_b + C'_i$$

$$C'_i = -\frac{dQ'_I}{d\phi_s} \cong -\frac{Q'_I}{\phi_t}$$

$$\phi_t = \frac{kT}{q}$$ thermal voltage (26 mV @ 300K)

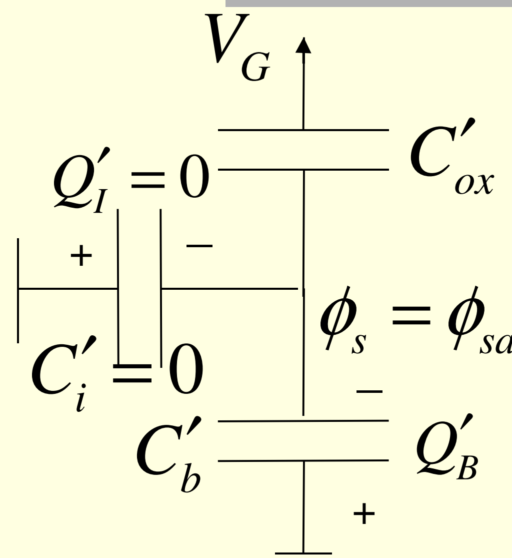
$$C'_b \cong \frac{\gamma C'_{ox}}{2\sqrt{\phi_s - \phi_t}}$$

γ body-effect coefficient



THE LINEARIZATION SURFACE POTENTIAL ϕ_{sa}

Determination of $\phi_{sa} = \phi_s \big|_{Q'_I = 0}$

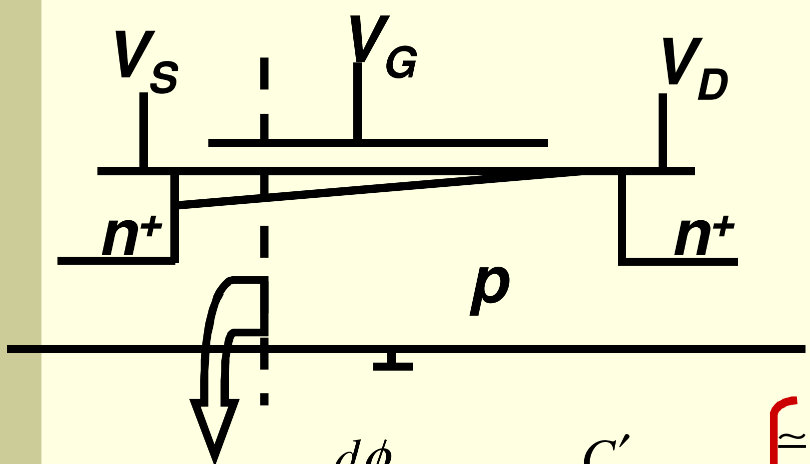


Potential balance

$$V_G - V_{FB} = \phi_{sa} + sgn(\phi_{sa})\gamma\sqrt{\phi_{sa} + \phi_t\left(e^{-\phi_{sa}/\phi_t} - 1\right)}$$

$$\frac{dV_G}{d\phi_{sa}} = n = 1 + \frac{C'_b}{C'_{ox}} = 1 + \frac{\gamma\left(1 - e^{-\phi_{sa}/\phi_t}\right)}{2\,\mathrm{sgn}\left(\phi_{sa}\right)\sqrt{\phi_{sa} + \phi_t\left(e^{-\phi_{sa}/\phi_t} - 1\right)}}$$

UNIFIED CHARGE CONTROL MODEL (UCCM)-1



$$C'_{ox} + C'_b = nC'_{ox}$$

$$n = n(V_G)$$

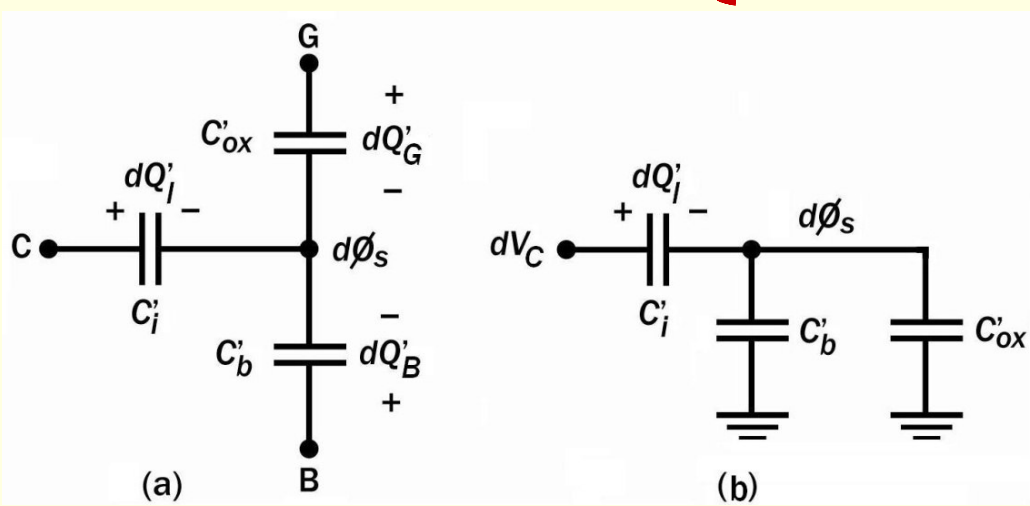
$$dQ'_I = nC'_{ox} d\phi_s$$

$$\frac{d\phi_s}{dV_C} = \frac{C'_i}{C'_i + C'_{ox} + C'_b} \begin{cases} \cong -\dfrac{Q'_I}{nC'_{ox}\phi_t} < 1 & \text{WI} \\ \cong 1 & \text{SI} \end{cases}$$

$$C'_i = -\frac{Q'_I}{\phi_t}$$

$$\boxed{dV_C = dQ'_I \left(\frac{1}{nC'_{ox}} - \frac{\phi_t}{Q'_I} \right)}$$

$$V_S \le V_C \le V_D$$



(a) (b)

UNIFIED CHARGE CONTROL MODEL (UCCM)-2

Integrating $dV_C = dQ'_I\left(\frac{1}{nC'_{ox}} - \frac{\phi_t}{Q'_I}\right)$ between V_C and V_P yields UCCM

$$\boxed{V_P - V_C = \frac{Q'_{IP} - Q'_I}{nC'_{ox}} + \phi_t \ln\left(\frac{Q'_I}{Q'_{IP}}\right)}$$

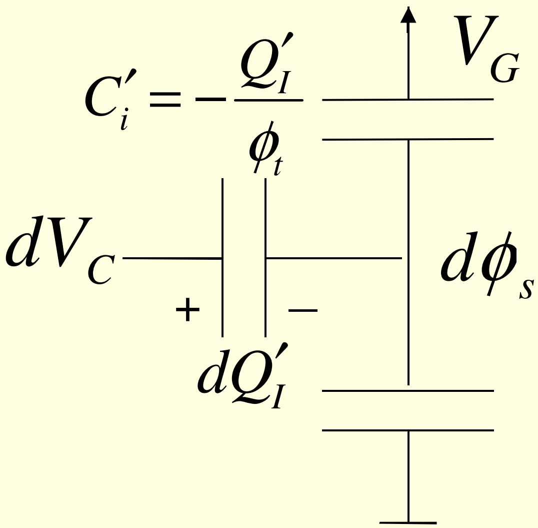
$Q'_{IP} = -nC'_{ox}\phi_t$ Thermal charge

$q'_I = \frac{Q'_I}{-nC'_{ox}\phi_t}$ Normalized inversion charge density

Normalized UCCM $\boxed{V_P - V_C = \phi_t(q'_I - 1 + \ln q'_I)}$

DRAIN CURRENT: PAO-SAH MODEL

$$C_i' = -\frac{Q_I'}{\phi_t}$$



$$dQ_I' = C_i'\left(dV_C - d\phi_s\right)$$

$$dV_C = d\phi_s - \phi_t \frac{dQ_I'}{Q_I'}$$

$$\overbrace{}^{I_{drift}} \qquad \overbrace{}^{I_{diff}}$$

$$\boxed{I_D = -\mu W Q_I' \left(\frac{d\phi_s}{dy} - \frac{\phi_t}{Q_I'}\frac{dQ_I'}{dy} \right) = -\mu W Q_I' \frac{dV_C}{dy}}$$

$$I_D = -\frac{W}{L}\int_{V_S}^{V_D} \mu Q_I' dV_C$$

$$\boxed{g_{md} = \left.\frac{\partial I_D}{\partial V_D}\right|_{V_G, V_S} = -\frac{W}{L}\mu Q_I'(V_D, V_G)}$$

DRAIN CURRENT: CHARGE-SHEET MODEL

drift diffusion

$$I_D = -\mu W Q_I' \frac{d\phi_s}{dy} + \mu W \phi_t \frac{dQ_I'}{dy}$$

$$dQ_I' = nC_{ox}' d\phi_s$$

drift diffusion

$$I_D = \frac{\mu W}{L}\left[\frac{Q_{IS}'^{\,2} - Q_{ID}'^{\,2}}{2nC_{ox}'} - \phi_t\left(Q_{IS}' - Q_{ID}'\right)\right]$$

$$S = \frac{W}{L}$$

Normalization (specific) current

$$\boxed{I_S = \mu C_{ox}' n \frac{\phi_t^2}{2} S}$$

Sheet normalization (specific) current

$$\boxed{I_{SH} = \mu C_{ox}' n \frac{\phi_t^2}{2}}$$

$$\boxed{I_D = I_F - I_R = I_S\left[i_f - i_r\right] = S I_{SH}\left[i_f - i_r\right]}$$

FORWARD AND REVERSE CURRENTS

Long-channel MOSFET $I_D = I_F - I_R = I(V_G, V_S) - I(V_G, V_D)$

I_F: forward current I_R: reverse current

(Forward) Saturation

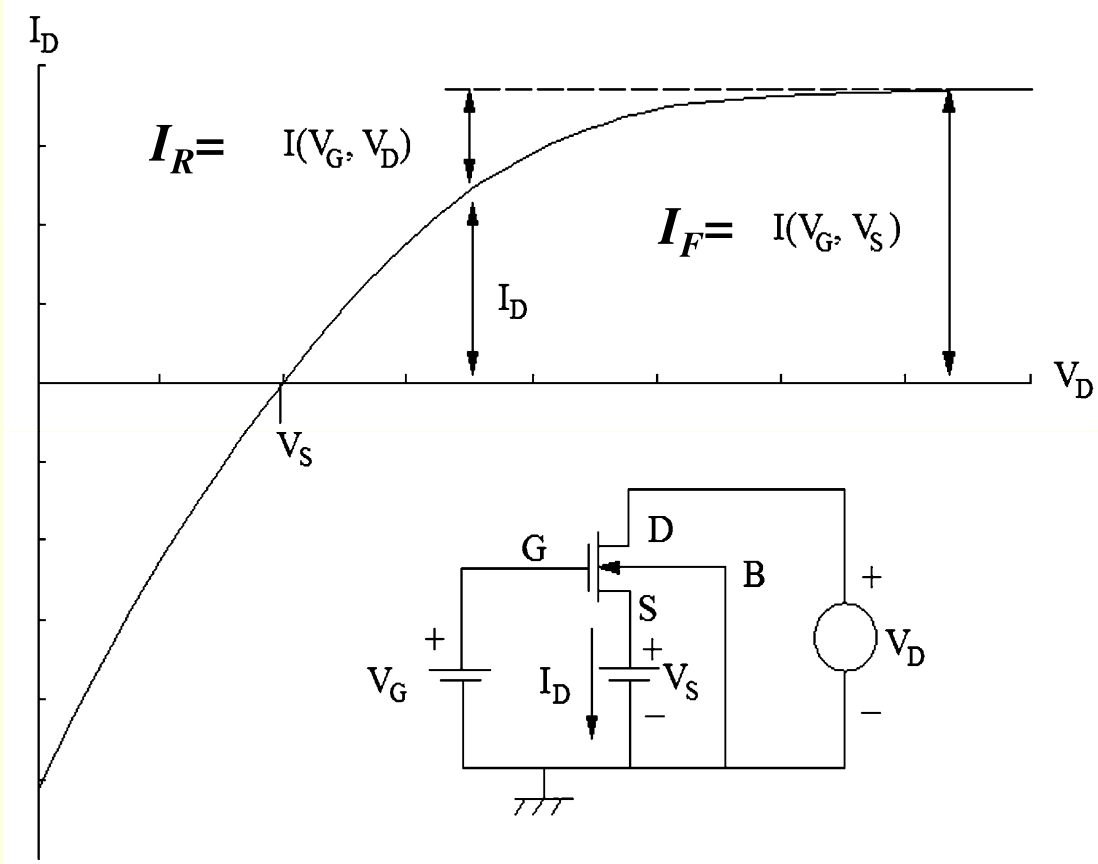
$$I_D = I_F - I_R \cong I_F$$

Triode

$$I_D = I_F - I_R$$

Triode for $V_{DS} \to 0$

$$I_F \cong I_R; \;\; I_D = I_F - I_R << I_F$$



MASTER DESIGN EQUATION

$$I_F = I_{drift} + I_{diff} = \frac{\mu W}{L}\left[\frac{Q_{IS}'^{\,2}}{2nC_{ox}'} - \phi_t Q_{IS}'\right]$$

$$g_{ms} = -\frac{W}{L}\mu Q_{IS}'$$ Pao-Sah model

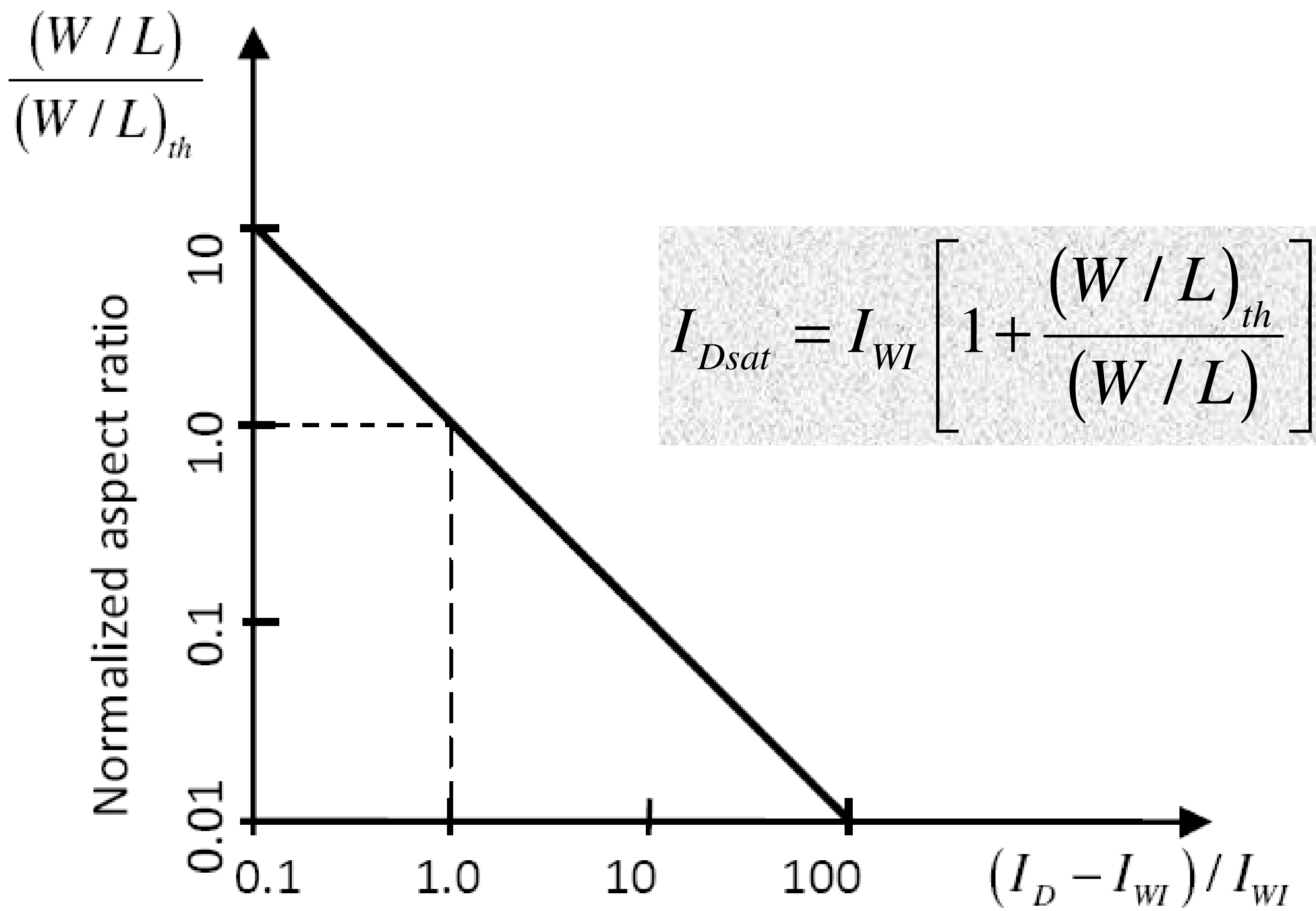
$$I_F = g_{ms}\phi_t\left[1 + \frac{g_{ms}}{2\mu C_{ox}' n\phi_t (W/L)}\right]$$

or

$$I_{Dsat} = I_{WI}\left[1 + \frac{(W/L)_{th}}{(W/L)}\right]$$

$$g_{ms} = (W/L)_{th}\,\mu\left(2nC_{ox}'\phi_t\right)$$

ASPECT RATIO VS. CURRENT EXCESS



$$I_{Dsat} = I_{WI}\left[1 + \frac{(W/L)_{th}}{(W/L)}\right]$$

WEAK, MODERATE, STRONG INVERSION

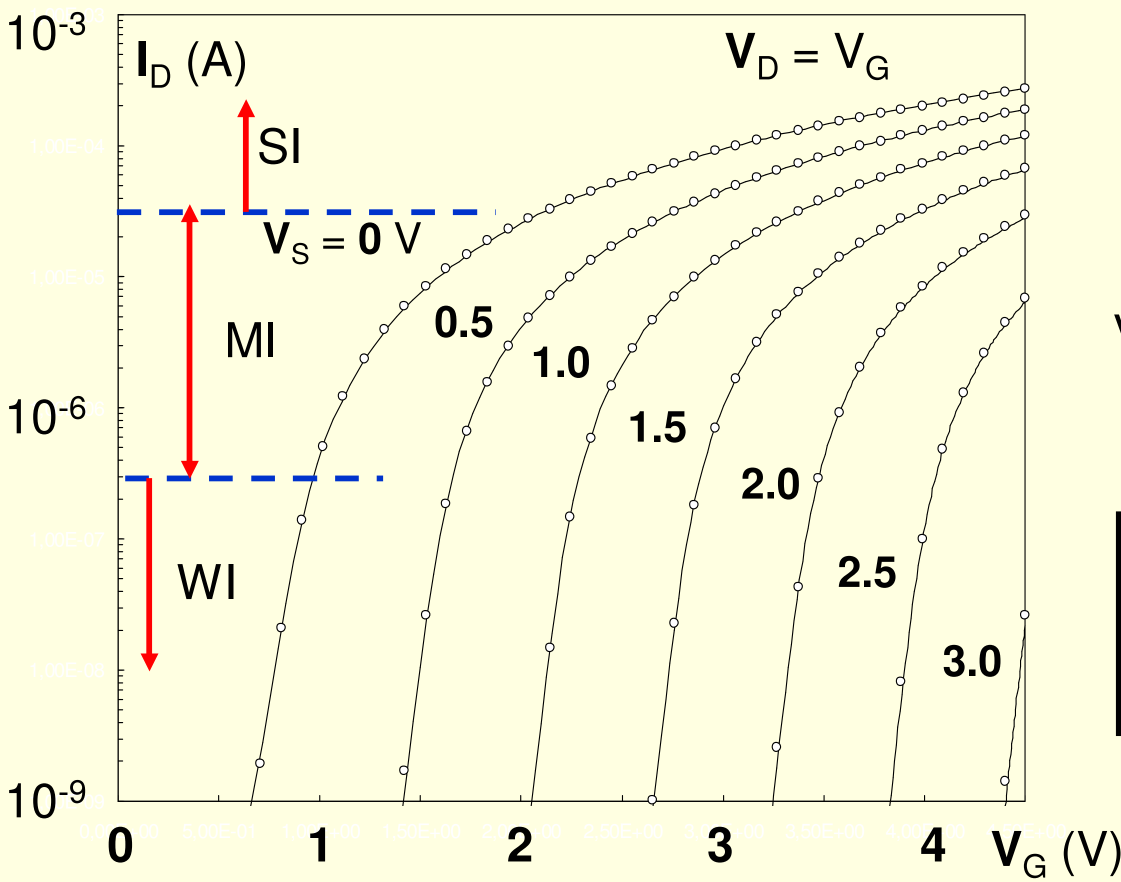
$$I_D = I_F - I_R = I_S\left[i_f - i_r\right]$$

$$\boxed{i_{f(r)} = {q'_{IS(D)}}^2 + 2q'_{IS(D)} \Rightarrow q'_{IS(D)} = \sqrt{1+i_{f(r)}} - 1}$$

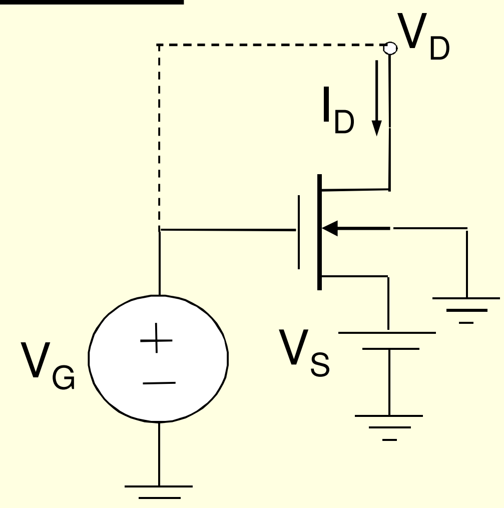
WI	MI	SI
$i_f < 1$	$1 < i_f < 100$	$100 < i_f$
$q'_I < 0.4$	$0.4 < q'_I < 9$	$9 < q'_I$

UNIFIED I-V RELATIONSHIP (UICM)

$$V_P - V_S = \phi_t \left[\sqrt{1+i_f} - 2 + \ln\left(\sqrt{1+i_f} - 1 \right) \right]$$



Common-source characteristics



$$I_D = I_S \left[i_f - i_r \right] \cong I_S i_f$$

$$\text{since} \quad i_f >> i_r$$

THE PINCH-OFF CHARGE DENSITY

The channel charge density corresponding to the effective channel capacitance times the thermal voltage, or thermal charge, defines pinch-off

$$Q'_{IP} = -(C'_{ox} + C'_b)\phi_t = -nC'_{ox}\phi_t$$

The name pinch-off is retained herein for historical reasons and means the channel potential corresponding to a small (but well-defined) amount of carriers in the channel.

THE PINCH-OFF VOLTAGE V_P

The channel-to-substrate voltage (V_C) for which the channel charge density equals the pinch-off charge density is called the pinch-off voltage V_P.

in weak inversion ⇨

$$-Q_I' = C_b' \phi_t e^{(\phi_{sa} - 2\phi_F - V_C)/\phi_t} = C_{ox}'(n-1)\phi_t e^{(\phi_{sa} - 2\phi_F - V_C)/\phi_t}$$

UCCM is asymptotically correct in weak inversion if

$$V_P = \phi_{sa} - 2\phi_F - \phi_t \left[1 + \ln\left(\frac{n}{n-1}\right)\right]$$

$$\boxed{V_P \cong \phi_{sa} - 2\phi_F}$$

THE THRESHOLD VOLTAGE V_{T0}

Equilibrium threshold voltage V_{T0}, for V_C=0, gate voltage for which $Q'_I = Q'_{IP} = -nC'_{ox}\phi_t$

(gate voltage for which V_P=0)

Recalling that

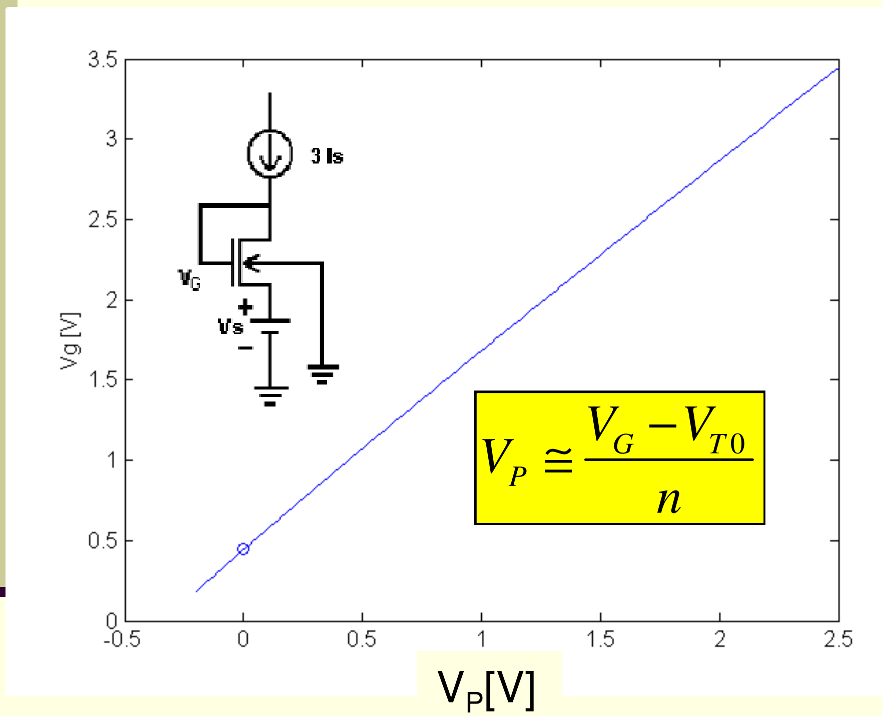
$$\begin{cases} V_P \cong \phi_{sa} - 2\phi_F \\ V_G - V_{FB} = \phi_{sa} + \gamma C'_{ox}\sqrt{\phi_{sa} - \phi_t} \end{cases}$$

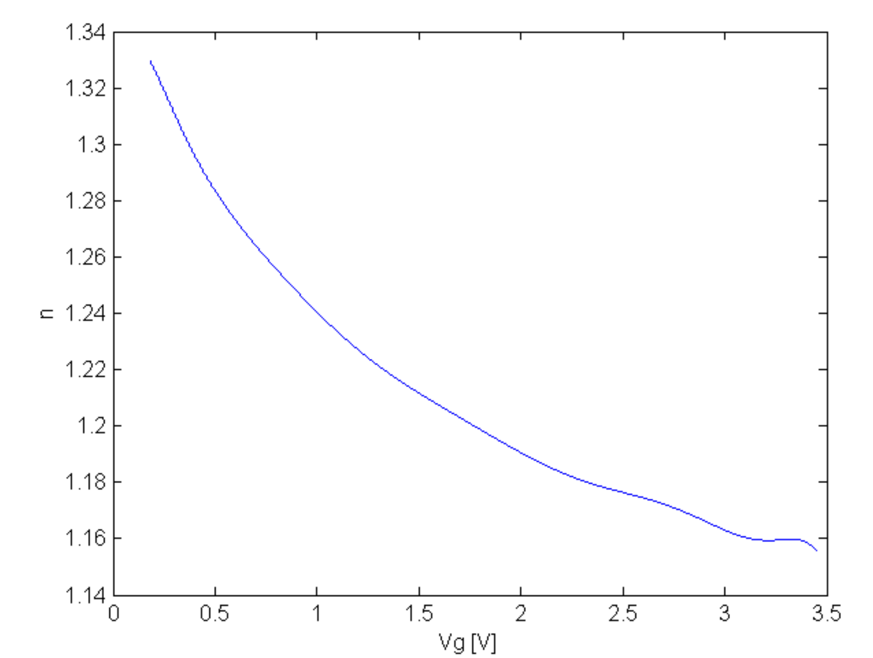
it follows that

$$\boxed{V_{T0} \cong V_{FB} + 2\phi_F + \gamma\sqrt{2\phi_F}}$$

PINCH-OFF VOLTAGE AND SLOPE FACTOR

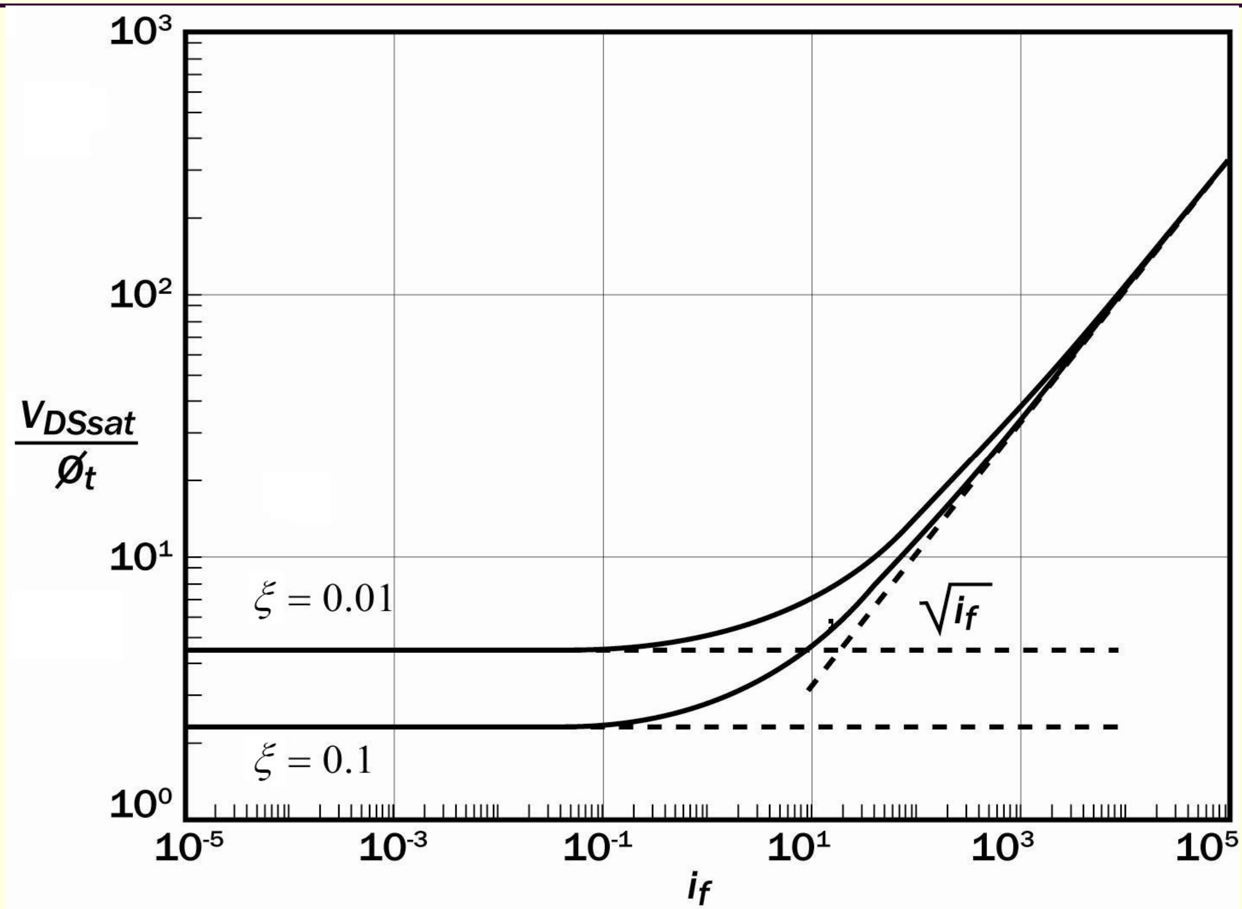
i_f=*3* at pinch-off ⇒ $$\boxed{V_P - V_S = 0 = \left[\sqrt{1+3} - 2 + \ln\left(\sqrt{1+3} - 1\right)\right]}$$





Pinch-off voltage and slope factor as functions of V_G [0.18 μm CMOS technology].

SATURATION VOLTAGE



Saturation voltage versus inversion level

Saturation voltage (V_{DSsat}): V_{DS} at which the ratio $q'_{ID}/q'_{IS} = \xi$

$$V_{DSsat} = \phi_t \left[\ln\left(\frac{1}{\xi}\right) + (1-\xi)\left(\sqrt{1+i_f} - 1\right) \right]$$

$(1-\xi)$ **is the saturation level**

TRANSCONDUCTANCES

$$\Delta I_D = g_{mg}\Delta V_G - g_{ms}\Delta V_S + g_{md}\Delta V_D + g_{mb}\Delta V_B$$

$$g_{mg} - g_{ms} + g_{md} + g_{mb} = 0$$

Calculation of g_{ms}

$$I_D = I_F - I_R = I_S\left[i_f - i_r\right]$$

$$i_{f(r)} = {q'_{IS(D)}}^2 + 2q'_{IS(D)}$$

$$V_P - V_C = \phi_t(q'_I - 1 + \ln q'_I)$$

$$\boxed{g_{ms} = -I_S\frac{di_f}{dV_S} = -\mu\frac{W}{L}Q'_{IS} = \frac{2I_S}{\phi_t}\left(\sqrt{1+i_f} - 1\right)}$$

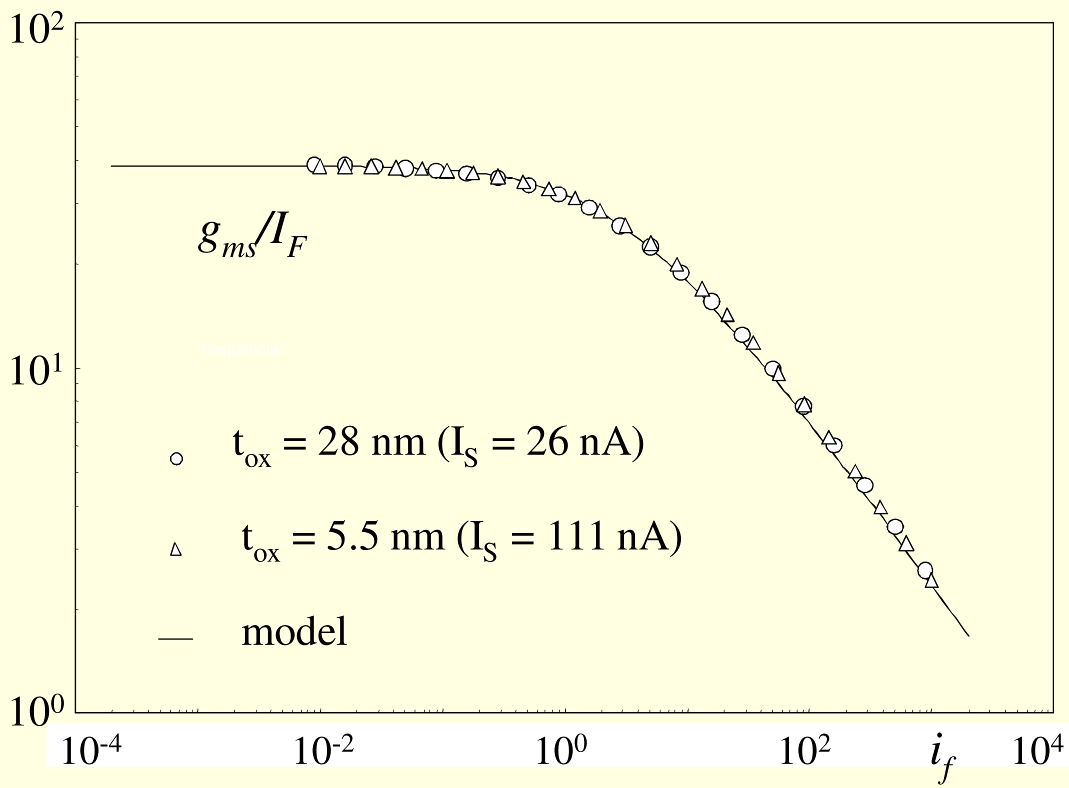
TRANSCONDUCTANCE-TO-CURRENT RATIO

Transconductance -to-current ratio

$$\frac{g_{ms(d)}\phi_t}{I_{F(R)}} = \frac{2}{\sqrt{1+i_{f(r)}}+1}$$

$\cong 1 \longrightarrow$ WI ($i_f < 1$)

$\cong \dfrac{2}{\sqrt{i_{f(r)}}} \longrightarrow$ SI ($i_f >> 1$)

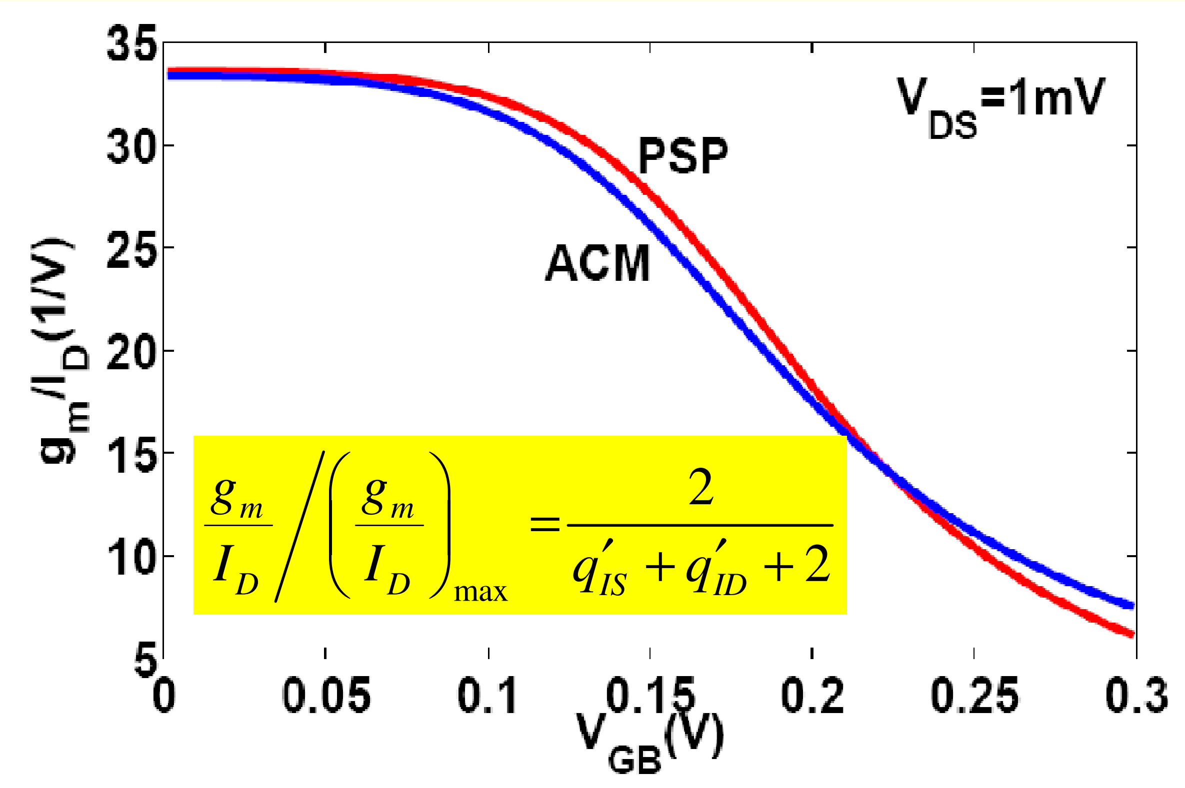


$$g_{mg} = \frac{g_{ms} - g_{md}}{n}$$

in saturation:

$$g_{mg} = \frac{g_{ms}}{n}$$

PARAMETER EXTRACTION



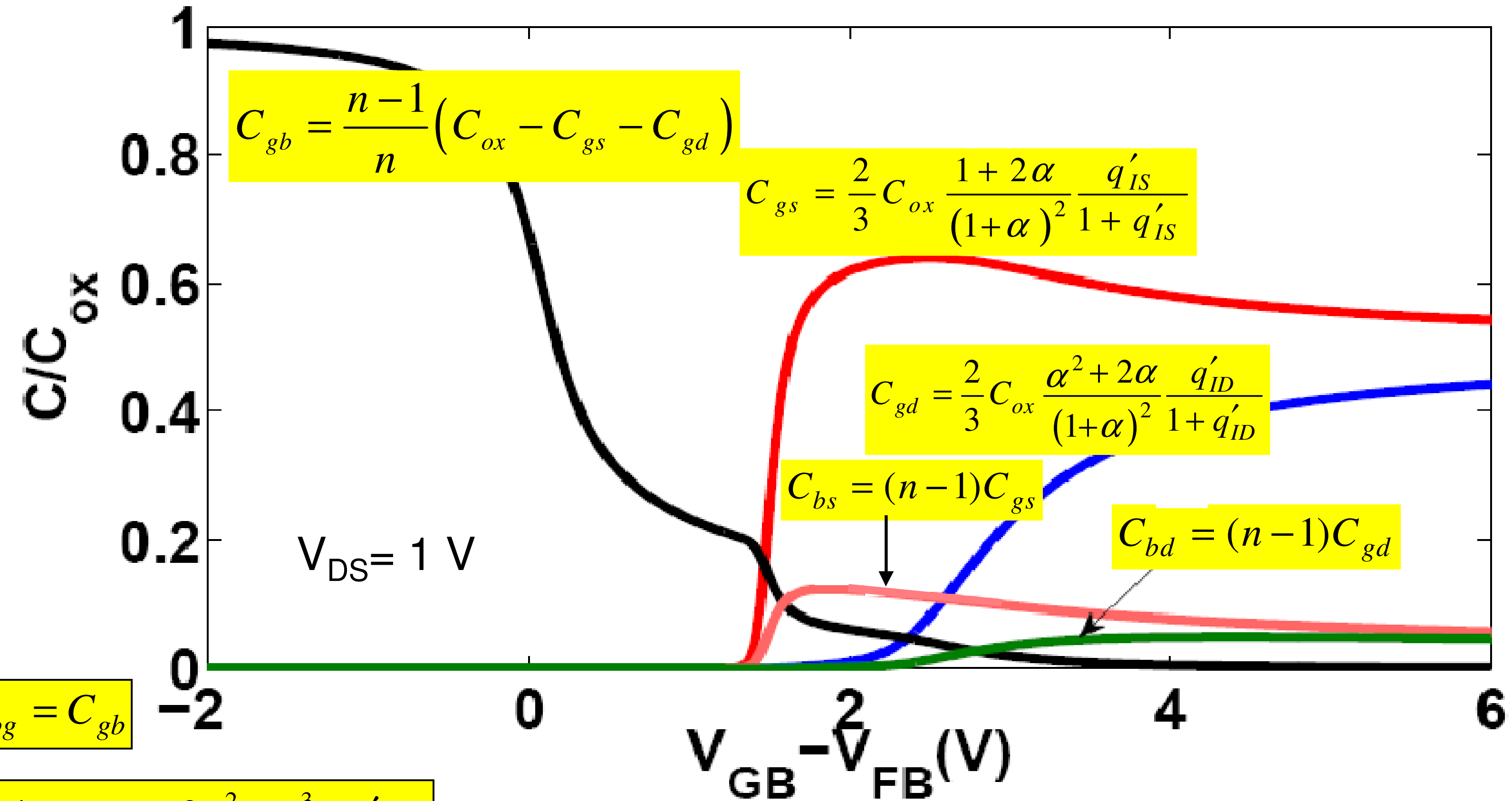
$$\frac{g_m}{I_D}\Bigg/\left(\frac{g_m}{I_D}\right)_{\max} = \frac{2}{q'_{IS} + q'_{ID} + 2}$$

$$\left(g_m / I_D\right)_{\max} = 1/\left(n\phi_t\right)$$

$$q'_{IS(D)} = \frac{Q'_{IS(D)}}{Q'_{IP}} = \frac{Q'_{IS(D)}}{-nC'_{ox}\phi_t}$$

INTRINSIC CAPACITANCES

A set of 9 independent MOSFET capacitances



$$C_{gb} = \frac{n-1}{n}\left(C_{ox} - C_{gs} - C_{gd}\right)$$

$$C_{gs} = \frac{2}{3} C_{ox} \frac{1+2\alpha}{(1+\alpha)^2} \frac{q'_{IS}}{1+q'_{IS}}$$

$$C_{gd} = \frac{2}{3} C_{ox} \frac{\alpha^2+2\alpha}{(1+\alpha)^2} \frac{q'_{ID}}{1+q'_{ID}}$$

$$C_{bs} = (n-1) C_{gs}$$

$$C_{bd} = (n-1) C_{gd}$$

$$C_{bg} = C_{gb}$$

$$C_{sd} = -\frac{4}{15} n C_{ox} \frac{\alpha + 3\alpha^2 + \alpha^3}{(1+\alpha)^3} \frac{q'_{ID}}{1+q'_{ID}}$$

$$C_{ds} = -\frac{4}{15} n C_{ox} \frac{1 + 3\alpha + \alpha^2}{(1+\alpha)^3} \frac{q'_{IS}}{1+q'_{IS}}$$

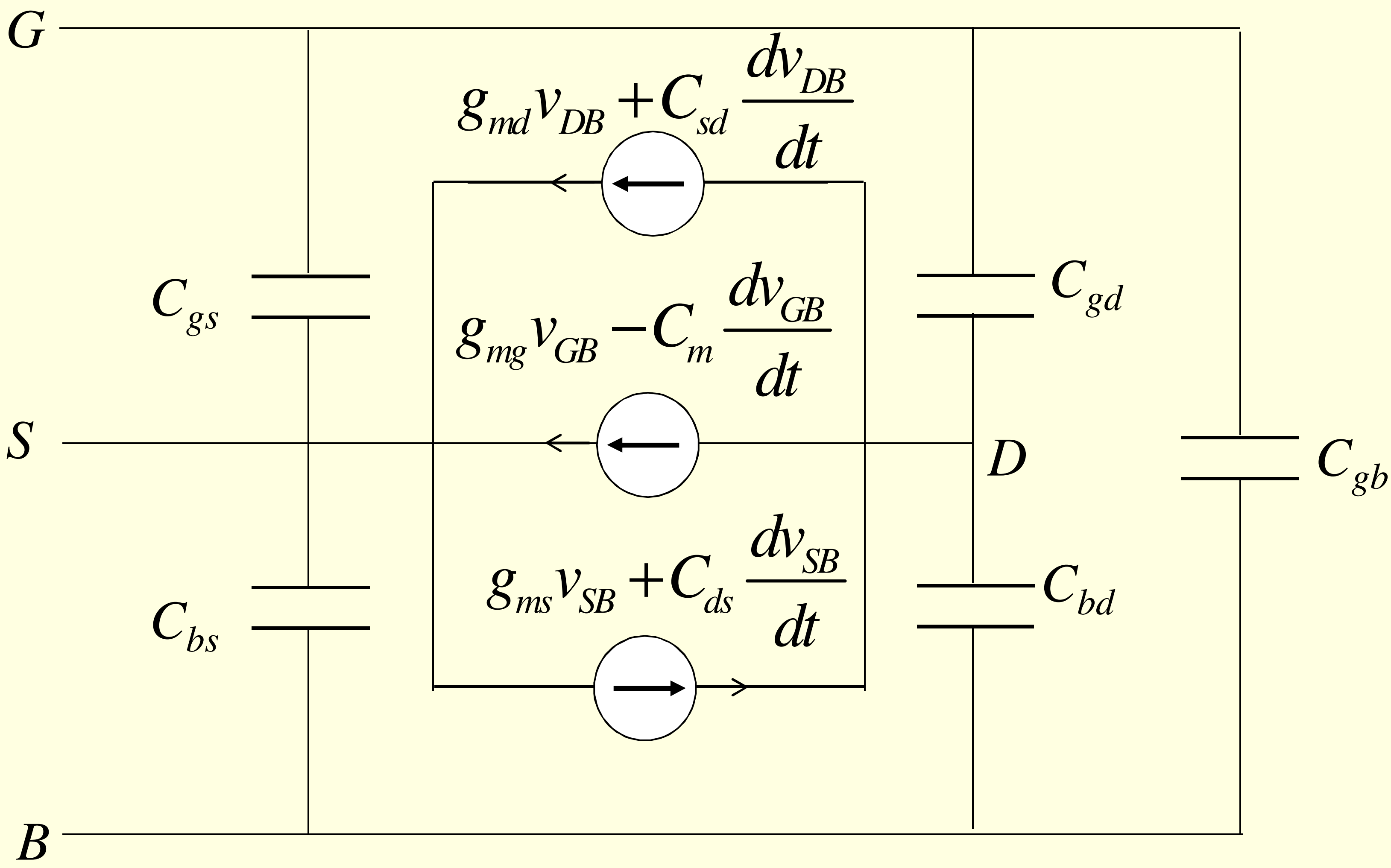
$$C_{dg} - C_{gd} = C_m = (C_{sd} - C_{ds})/n$$

$$C_{ox} = WLC'_{ox}$$

$$\alpha = \frac{1+q'_{ID}}{1+q'_{IS}}$$

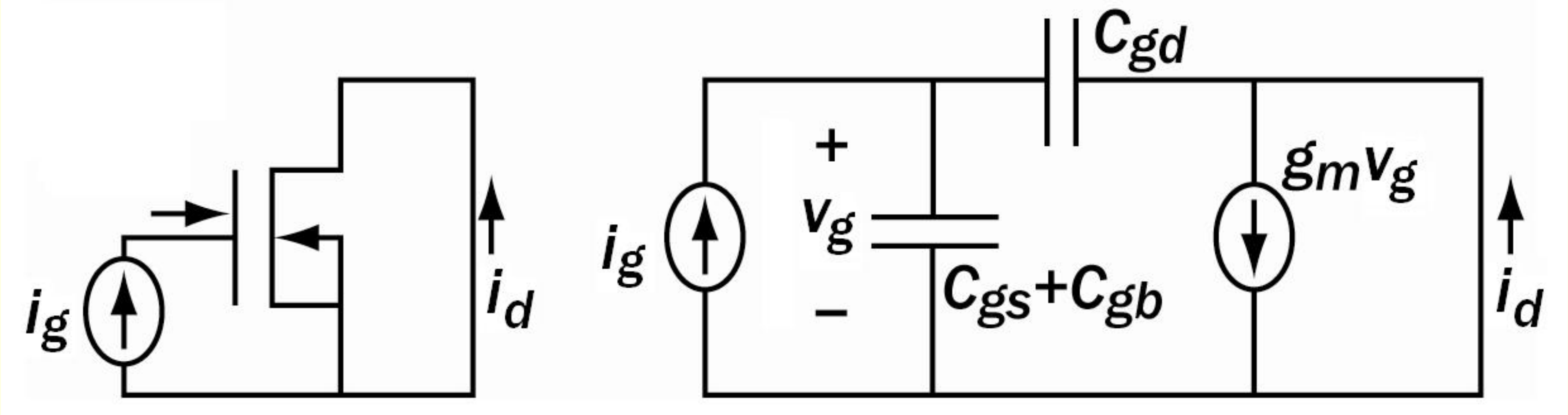
⟹ Channel linearity factor

SMALL-SIGNAL MOSFET MODEL



$$\boxed{C_{dg} - C_{gd} = C_m = (C_{sd} - C_{ds})/n}$$

INTRINSIC TRANSITION FREQUENCY



$$f_T = \frac{g_{mg}}{2\pi\left(C_{gs}+C_{gb}\right)} = \frac{g_{ms}}{2\pi n\left(C_{gs}+C_{gb}\right)}$$

$$\boxed{f_T \cong \frac{\mu\phi_t}{2\pi L^2}2\left(\sqrt{1+i_f}-1\right)}$$

NOISE & MISMATCH

- The spontaneous fluctuations over time of the current and voltage inside a device, which are basically related to the discrete nature of electrical charge, are called electrical noise.
- Time-independent variations between identically designed devices in an integrated circuit due to the spatial fluctuations in the technological parameters and geometries are called mismatch.
- Mismatch (spatial fluctuation) and noise (temporal fluctuation) are similar phenomena, both being dependent on the process, device dimensions, and bias.
- Mismatch can be seen as “dc noise”.

THERMAL NOISE EXCESS FACTOR-1

For $V_{DS}\rightarrow 0$, the transistor is equivalent to a resistor and

$$\frac{\overline{i_d^{\,2}}}{\Delta f} = -4kT\mu \frac{WLQ'_{IS}}{L^2} = 4kTg_{ms}$$

where g_{ms} ($=g_{md}$) is the equivalent conductance of the transistor

In weak inversion

$$\frac{\overline{i_d^2}}{\Delta f} \cong -4kT\mu \frac{W}{L} \frac{\left(Q'_{IS} + Q'_{ID}\right)}{2} = 4kT\frac{g_{ms} + g_{md}}{2}$$

For a saturated transistor (g_{ms}>>g_{md}) in weak inversion

$$\frac{\overline{i_d^2}}{\Delta f} = 2kTg_{ms}$$

THERMAL NOISE EXCESS FACTOR-2

In general, the channel thermal noise is written as

$$\frac{\overline{i_d^2}}{\Delta f} = 4kT\gamma g_{ms}$$

γ is the excess noise factor and its value is 2/3 for a long-channel saturated transistor in strong inversion.

for a short-channel transistor

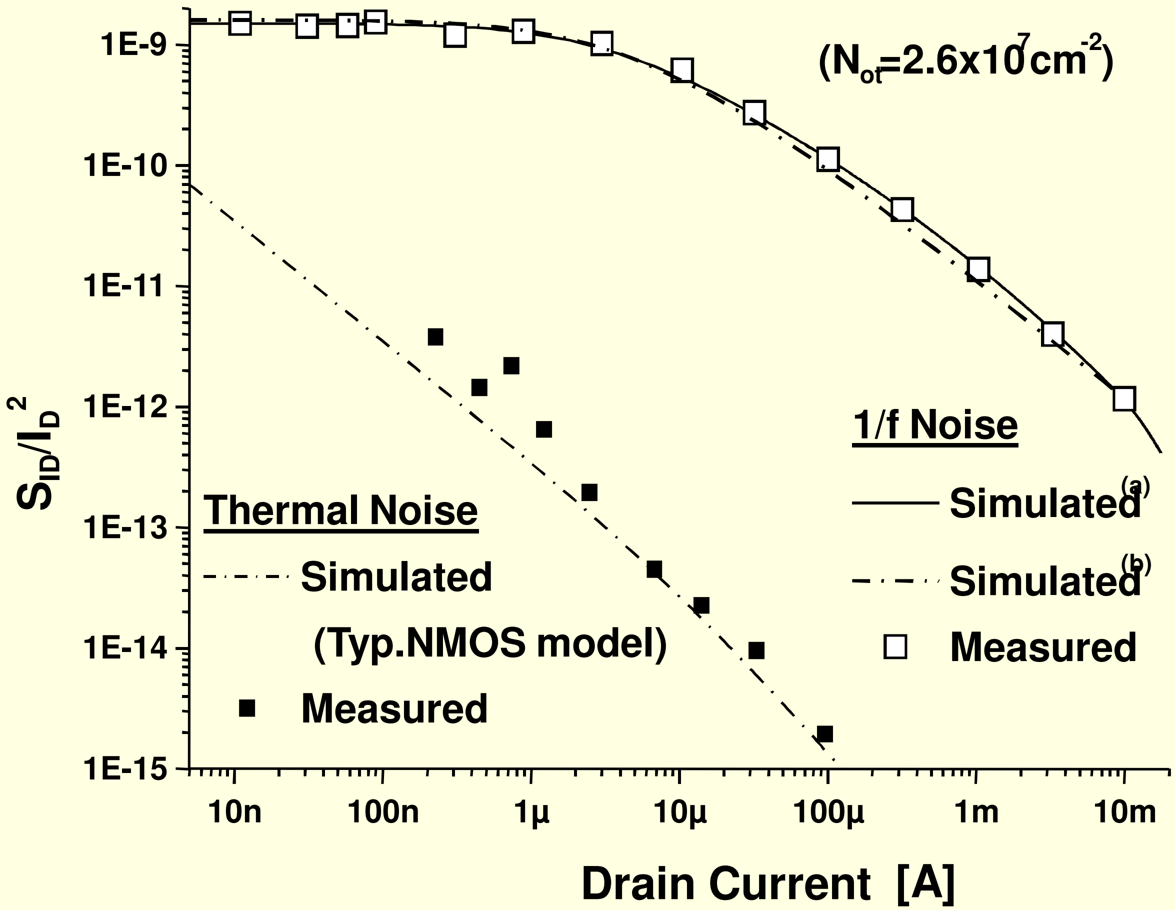
$$\gamma_{short} = \frac{L_e Q_I}{L_{esat}^2 W Q_I'}$$

where L_e and L_{esat} are the electric length of the channel in the linear and the saturation regions, respectively. Considering that $L_{esat} = L_e - \Delta L$, where ΔL is the channel shortening due to CLM, then we can write

$$\gamma_{short} \cong \left(1 + \frac{2\Delta L}{L_e}\right) \frac{Q_I}{W L_e Q_{IS}'}$$

for short-channel transistors it is possible that $\gamma > 1$ due to the CLM effect.

THERMAL AND 1/F NOISE



Normalized flicker and thermal PSD at f=1Hz for saturated NMOS-T (W/L=200/5)

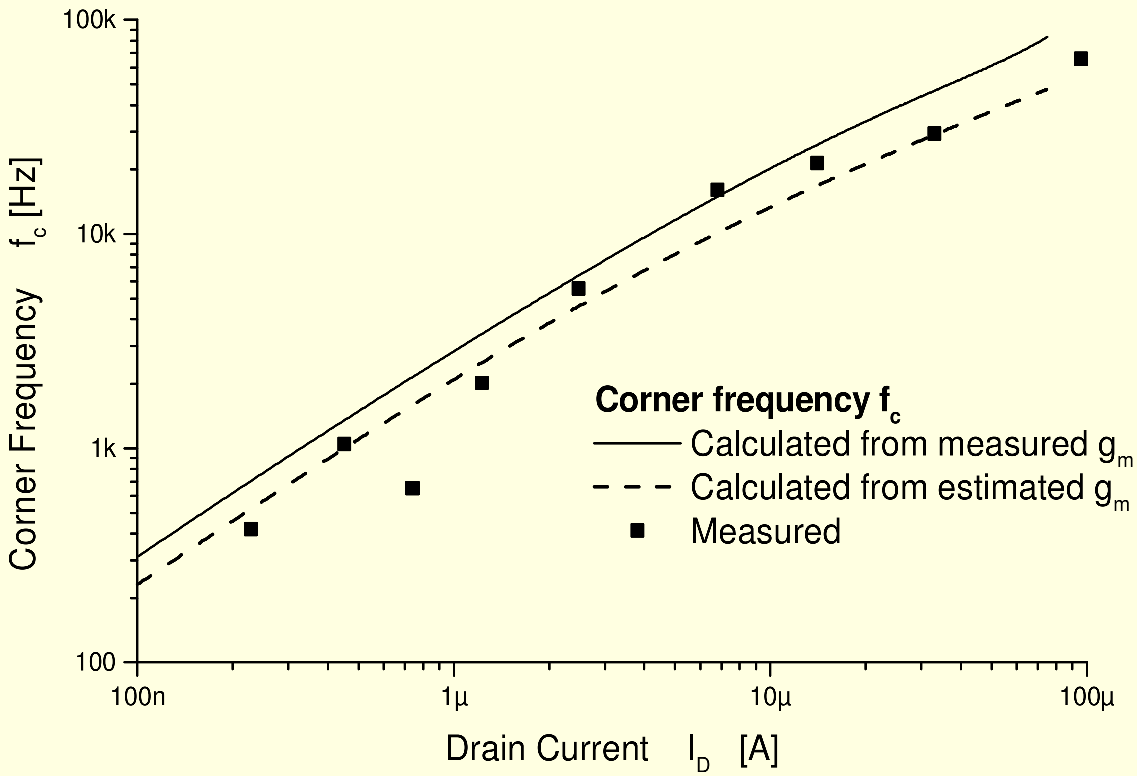
CORNER FREQUENCY

Noise corner frequency (frequency at which the PSD of the 1/f noise equals the PSD of the thermal noise)

$$f_c \approx \frac{\pi}{2} \frac{K_F}{nq\phi_t} f_T$$

K_F SPICE NLEV 2,3

1/f noise constant



PELGROM'S MODEL OF MISMATCH

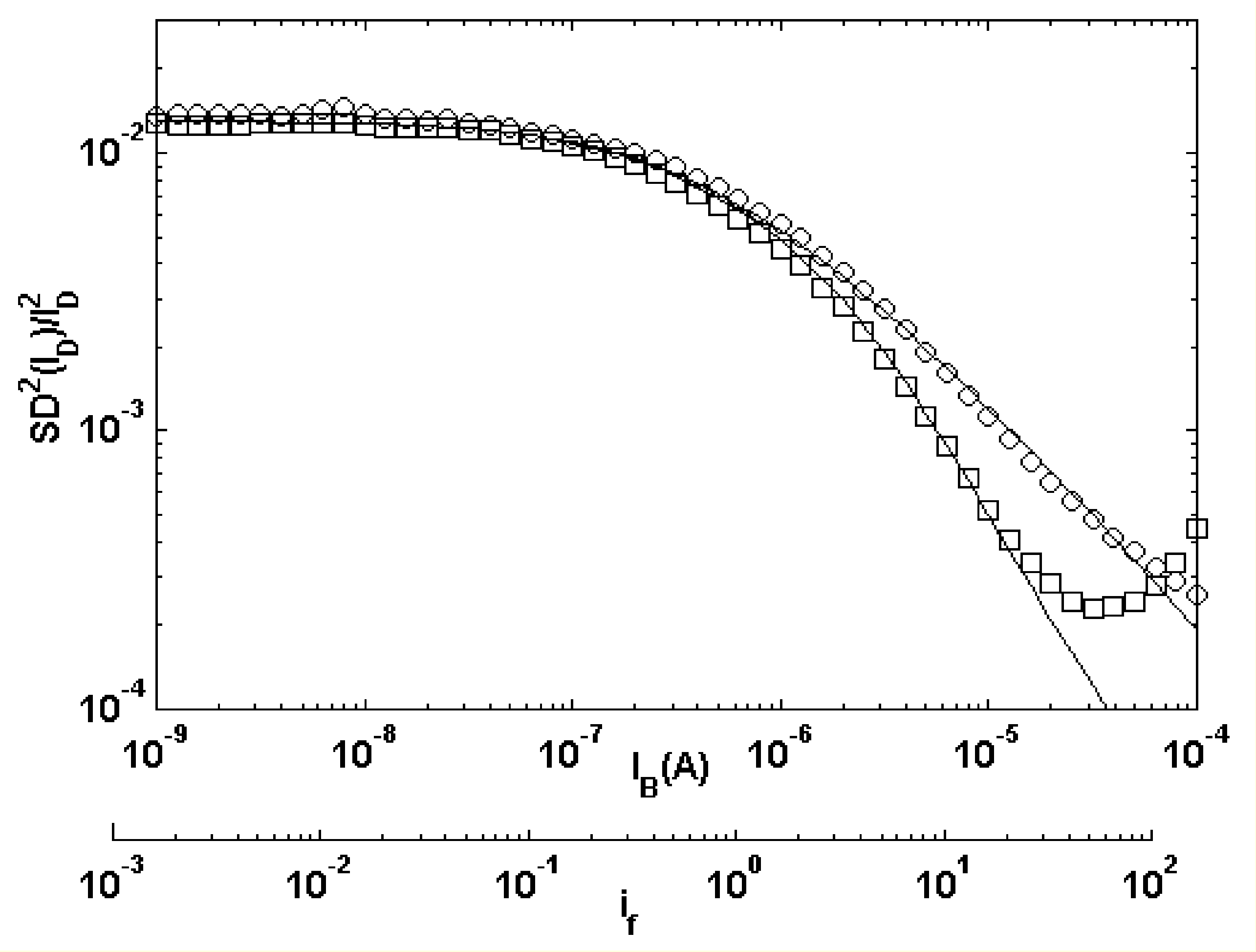
$$\sigma\left(V_{T0}\right) = q\frac{\sigma\left(\text{number of acceptors under gate}\right)}{WLC'_{ox}} = q\sqrt{WLx_d N_A} / (WLC'_{ox})$$

- In most applications: the standard deviation of the difference between the threshold voltages of two identical transistors ($\Delta V_{T0}=V_{T1}-V_{T2}$) is

$$\boxed{\sigma\left(\Delta V_{T0}\right) = \sqrt{2}\sigma\left(V_{T0}\right) = \frac{q\sqrt{2x_d N_A}}{C'_{ox}\sqrt{WL}} = \frac{A_{VT}}{\sqrt{WL}}}$$

$$A_{VT} = \frac{q\sqrt{2x_d N_A}}{C'_{ox}}$$

MISMATCH – EXPERIMENTAL RESULTS



Dependence of mistmatch on inversion level - Linear: □ (V_{DS}=50mV); Saturation: ○ (V_{DS}=1V) regions. Model :—

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CONTENTS

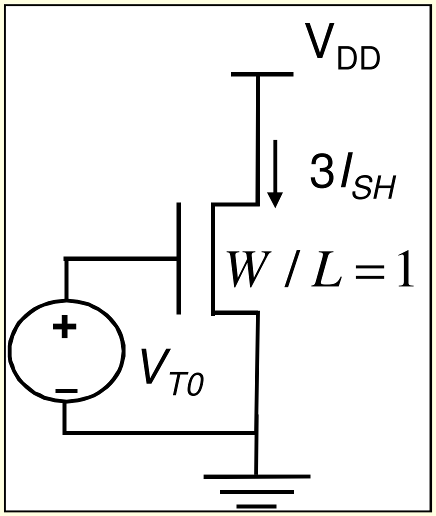
- The intrinsic gain stage
- The source-coupled pair
- The two-transistor current mirror
- A self-biased current source
- A folded cascode amplifier

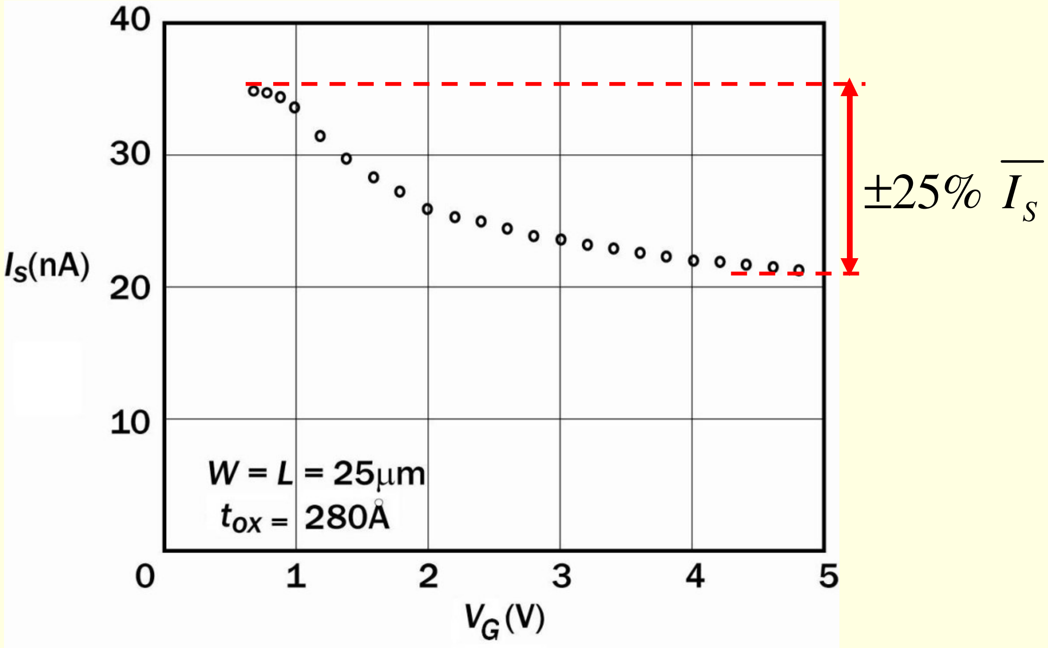
SUMMARY OF MAIN DESIGN EQUATIONS - 1

Sheet specific current

$$I_{SH} = \mu C'_{ox} n \phi_t^2 / 2$$

0.35 um CMOS technology $\begin{cases} \overline{I_{SHN}} \cong 70 \text{ nA} \\ \overline{I_{SHP}} \cong 25 \text{ nA} \end{cases}$





Specific (normalization) current

$$I_S = I_{SH}\left(W/L\right)$$

Forward and reverse currents

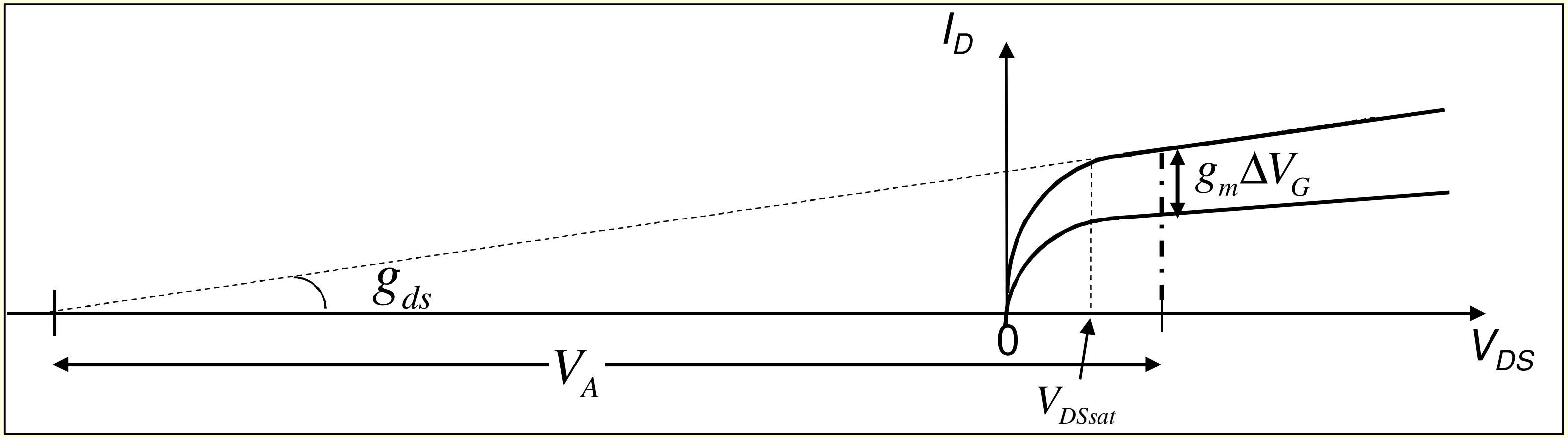
$$I_D = I_F - I_R = I_S\left(i_f - i_r\right)$$

$$I_D \cong I_F = I_S i_f$$ saturation

SUMMARY OF MAIN DESIGN EQUATIONS-2

UICM

$$\frac{V_P - V_{S(D)}}{\phi_t} + 1 = \left(\sqrt{1+i_{f(r)}} - 1\right) + \ln\left(\sqrt{1+i_{f(r)}} - 1\right) \qquad V_P \cong \frac{V_G - V_{T0}}{n}$$



Saturation

$$V_{DS} > V_{DSsat}$$

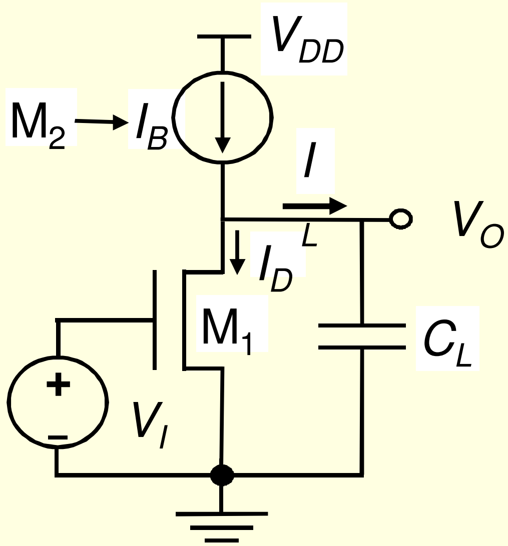
$$V_{DSsat} = \phi_t\left(\sqrt{1+i_f} + 3\right)$$

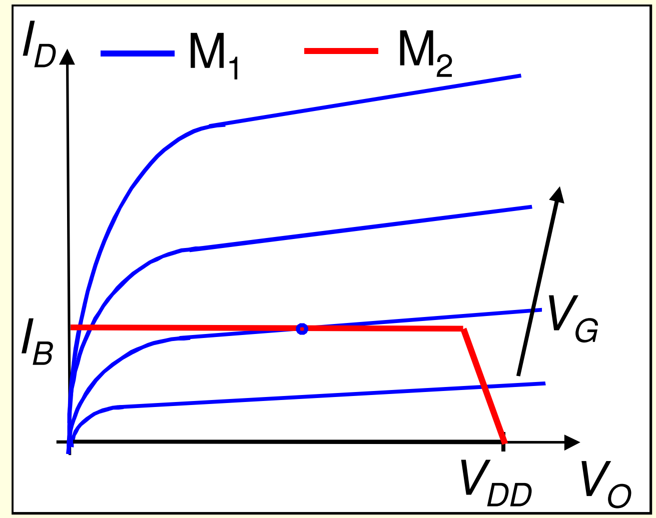
Gate transconductance $\quad g_m = \frac{2I_S}{n\phi_t}\left(\sqrt{1+i_f} - 1\right)$

Output conductance $\quad g_{ds} = I_D / V_A$

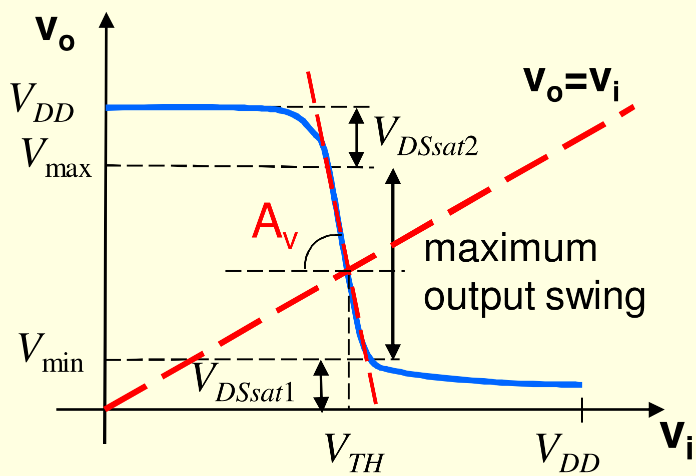
$$\boxed{V_A = V_E L}$$

THE INTRINSIC GAIN STAGE - 1





Output characteristics



Voltage transfer characteristic

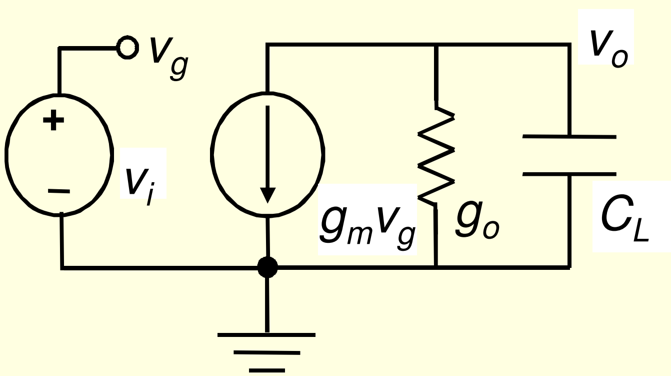
From UICM we find the dc voltage V_{TH} at the input:

$$\boxed{\frac{V_{TH} - V_{T01}}{n_1 \phi_t} \cong \sqrt{1 + i_{f1}} - 2 + \ln\left(\sqrt{1 + i_{f1}} - 1\right)}$$

$$I_D = I_B \cong I_{F1} - \underbrace{\cancel{I_{R1}}}_{0}; \quad i_{f1} \cong \frac{I_B}{I_{S1}}$$

THE INTRINSIC GAIN STAGE - 2

V-I converter (transconductor) followed by an I-V converter (output impedance)



$$\boxed{A_V = \frac{v_o}{v_i} = -g_m\left(\frac{1}{g_o + sC_L}\right) = A_{V0}\frac{1}{1+s/\omega_b}}$$

$$A_{V0} = \frac{-g_{m1}}{g_o} = \frac{-g_{m1}}{g_{ds1}}$$

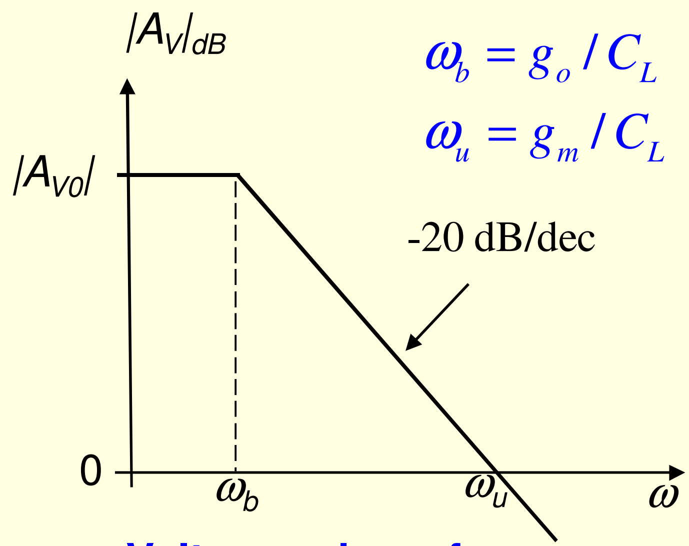
$$g_{ds1} = \frac{I_B}{V_{A1}}$$

$$\boxed{A_{V0} = -\frac{V_{A1}}{n_1\phi_t}\frac{2}{1+\sqrt{1+i_{f1}}}}$$

$$V_{A1} = V_E L_1$$

$$\omega_b = g_o / C_L$$

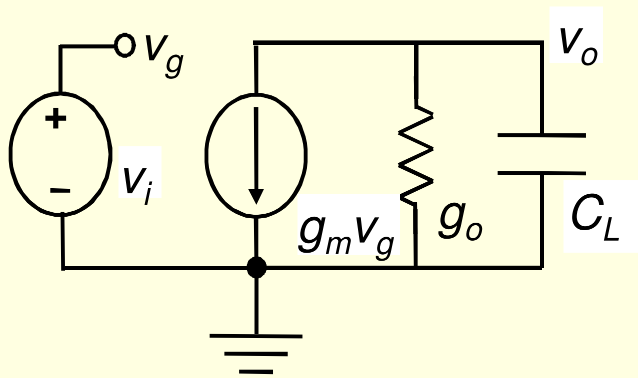
$$\omega_u = g_m / C_L$$



Voltage gain vs frequency

THE INTRINSIC GAIN STAGE - 3

Design example



Specifications: ω_u, C_L, A_{V0}

$$g_m = \omega_u \cdot C_L$$

$$I_D = n\phi_t g_m \frac{\sqrt{1+i_f}+1}{2}$$

How do we choose i_f?

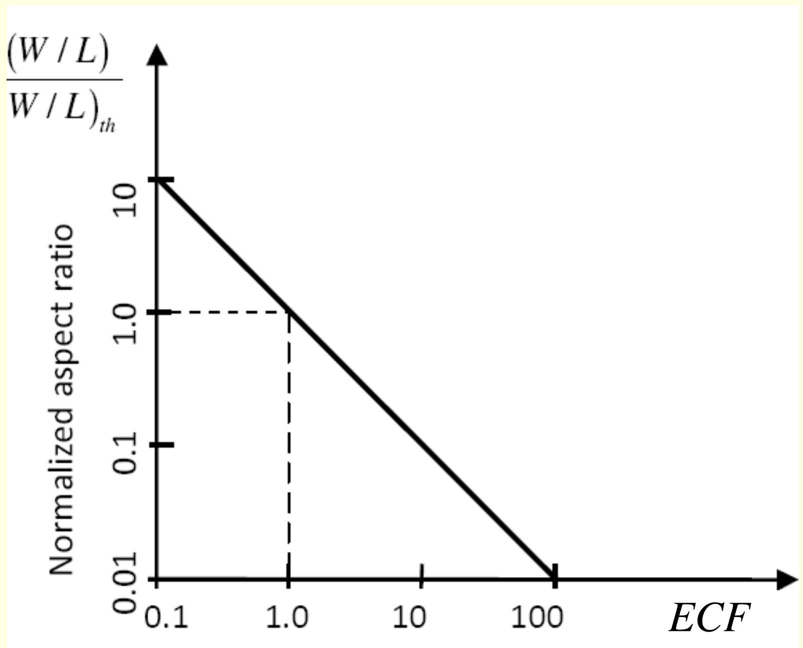
Sizing and biasing: W, L, I_B

$$I_{D\min} = I_{WI} = g_m n\phi_t$$

$$ECF = (I_D - I_{WI})/I_{WI} = \left(\sqrt{1+i_f}-1\right)/2$$

$$\boxed{\frac{W}{L} = \frac{g_m}{2\mu C'_{ox}\phi_t}\frac{1}{ECF}}$$

Power-area tradeoff



$$ECF = (I_D - I_{D\min})/I_{D\min}$$

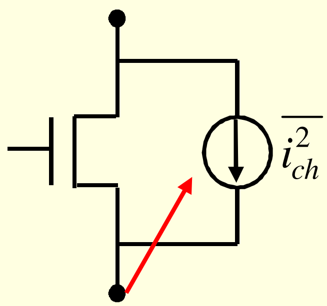
$$A_{V0} = -\frac{V_E L}{n\phi_t}\frac{1}{ECF+1}$$

How long can L be?

C_{IN} and transit time are both proportional to L^2 (for constant W/L)!

THE INTRINSIC GAIN STAGE - 4

MOST noise model



Noise current generator

Thermal **1/f**

$$\boxed{\frac{\overline{i_{ch}^2}}{\Delta f} = 4\gamma kT g_{ms} + \frac{K_F g_m^2}{WLC'_{ox}}\frac{1}{f} \cong 4\gamma kT g_{ms}\left(1+\frac{f_c}{f}\right)}$$

Bias-dependent factor

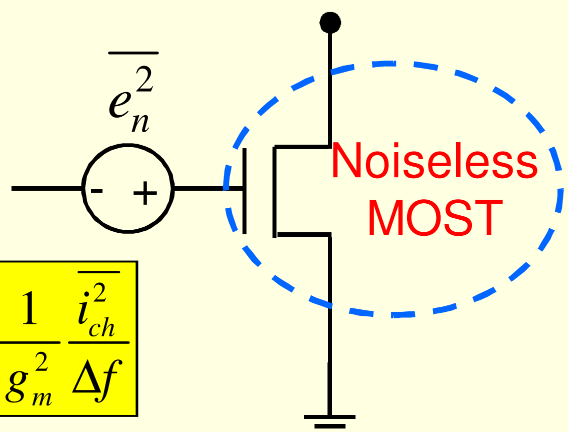
Corner frequency

$$\gamma = \frac{2}{3}\left(1 - \frac{1/2}{\sqrt{1+i_f}+1}\right)$$

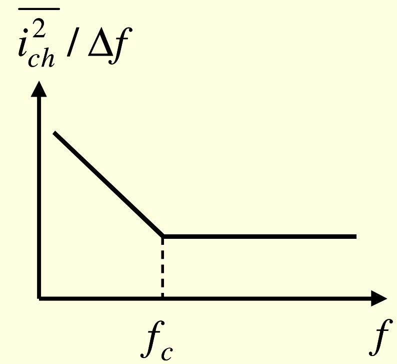
1/2 (WI) **2/3 (SI)**

$$f_c \cong \frac{\pi}{2}\frac{K_F}{nq\phi_t} f_T$$

Input-referred noise model

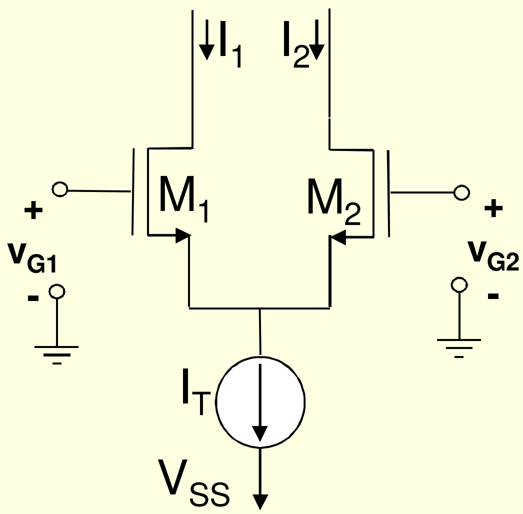


$$\boxed{\frac{\overline{e_n^2}}{\Delta f} = \frac{1}{g_m^2}\frac{\overline{i_{ch}^2}}{\Delta f}}$$



$$f_c \cong \frac{f_T}{2000}$$ ⇒ 0.35 um CMOS technology

THE SOURCE-COUPLED PAIR -1



First order analysis:

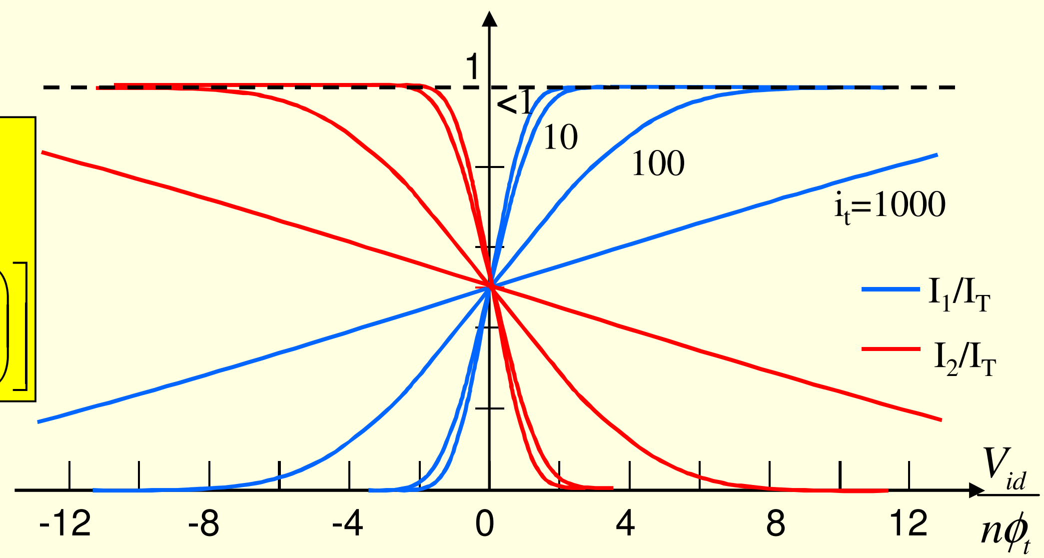
- Ideal current source
- M_1 & M_2 in saturation → I_1 & I_2 independent of drain voltage;

$$I_1 + I_2 = I_T \qquad n_1 \cong n_2 = n$$
$$I_1 - I_2 = I_{OD} \qquad I_{S1} \cong I_{S2} = I_S$$
$$V_{G1} - V_{G2} = V_{id} \qquad i_{r1} = i_{r2} = 0$$

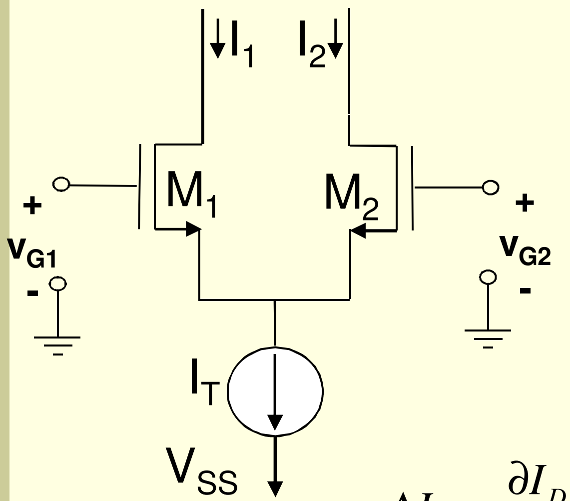
Normalization

$$i_t = I_T / I_S \qquad i_{od} = I_{OD} / I_S$$
$$i_1 = I_1 / I_S \qquad i_2 = I_2 / I_S$$
$$i_t = i_1 + i_2 \qquad i_{od} = i_1 - i_2$$

$$\frac{V_{id}}{n\phi_t} = \sqrt{1+\frac{i_t+i_{od}}{2}} - \sqrt{1+\frac{i_t-i_{od}}{2}} + \ln\left[\left(\sqrt{1+\frac{i_t+i_{od}}{2}}-1\right)\Big/\left(\sqrt{1+\frac{i_t-i_{od}}{2}}-1\right)\right]$$



THE SOURCE-COUPLED PAIR - 2



Offset voltage $V_{OS} = \Delta V_G = V_{G2} - V_{G1}$ such that $\Delta I_D = I_2 - I_1 = 0$

Simple model $V_{T02} = V_{T01} + \Delta V_T; \quad I_{S2} = I_{S1} + \Delta I_S$

$$I_D = I_S \left[i_f - \cancel{i_r}^{\,0} \right] = I_S f(V_G - V_{T0}, V_S)$$

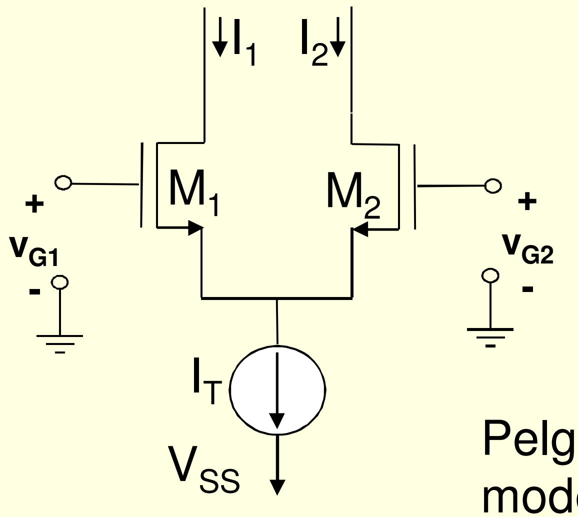
$$\Delta I_D \cong \frac{\partial I_D}{\partial I_S}\Delta I_S + \frac{\partial I_D}{\partial V_G}\Delta V_G + \frac{\partial I_D}{\partial V_{T0}}\Delta V_{T0} = \frac{I_D}{I_S}\Delta I_S + g_m\left(\Delta V_G - \Delta V_{T0}\right) \quad @V_S$$

$$\boxed{\frac{\Delta I_D}{I_D} \cong \frac{\Delta I_S}{I_S} + \frac{g_m}{I_D}\left(\Delta V_G - \Delta V_{T0}\right)}$$

The differential input voltage at the input required for $\Delta I_D = 0$ is

$$\boxed{\Delta V_G = V_{OS} = \Delta V_T - \frac{I_T}{2g_m}\frac{\Delta I_S}{I_S}}$$

THE SOURCE-COUPLED PAIR - 3



$$\Delta V_G = V_{OS} = \Delta V_T - \frac{I_T}{2g_m}\frac{\Delta I_S}{I_S}$$

Uncorrelated Δ V_T & Δ I_S

$$\boxed{\sigma^2(V_{OS}) = \sigma^2(\Delta V_T) + \left(\frac{I_T}{2g_m}\right)^2 \frac{\sigma^2(\Delta I_S)}{I_S^2}}$$

Pelgrom's model $\quad \sigma^2(\Delta V_T) \cong \frac{A_{VT}^2}{WL}; \quad \frac{\sigma^2(\Delta I_S)}{I_S^2} \cong \frac{A_{IS}^2}{WL}$

$$\boxed{\sigma^2(V_{OS}) = \underbrace{\frac{A_{VT}^2}{WL}}_{\text{(I)}} + \underbrace{\left(\frac{I_T}{2g_m}\right)^2 \frac{A_{IS}^2}{WL}}_{\text{(II)}}}$$

Reminder $\quad \frac{I_T}{2g_m} = \frac{I_D}{g_m} = n\phi_t\left(\frac{\sqrt{1+i_f}+1}{2}\right)$

$$A_{IS} = A_\beta$$

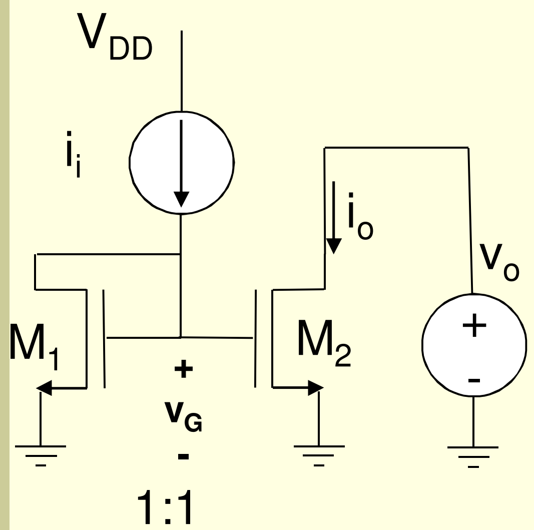
(I) is dominant over (II) for $\quad \sqrt{1+i_f}+1 < \frac{2}{n\phi_t}\frac{A_{VT}}{A_{IS}} \Rightarrow$

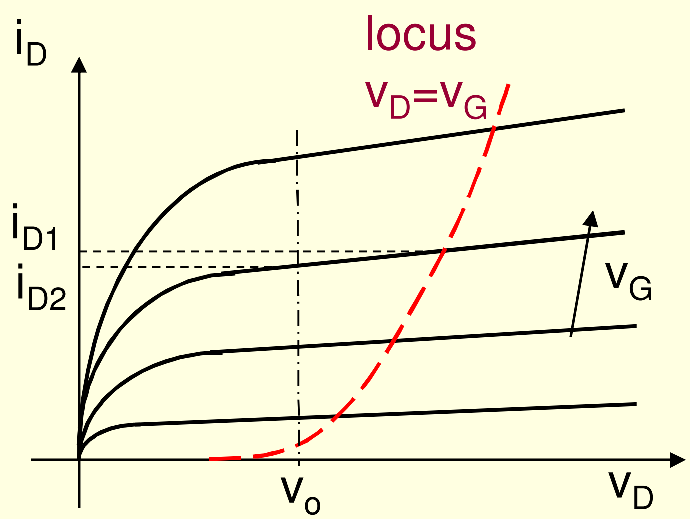
$i_f < 580 \;\; (V_G < V_{T0} + 0.8 \text{ V}) \;$ for $n\phi_t = 32$ mV,

$A_{VT} = 8 \text{ mV} \cdot \mu\text{m}, \; A_\beta = 2 \; \% \cdot \mu\text{m}$

$\sigma(V_{OS}) \cong 2$ mV for $WL = 16\mu\text{m}^2 \quad \& \; i_f < 100$

THE TWO-TRANSISTOR CURRENT MIRROR - 1





M_1: i→v converter
M_2: v→i converter

Basic principle
$V_{G1}=V_{G2}$; $V_{S1}=V_{S2}$;
$v_{out}>V_{Dsat} \rightarrow i_o \cong i_i$

Error due to difference in V_D values

$$I_D \cong I_S i_f \left(V_G - V_{T0}, V_S\right)\left(1+V_D/V_A\right) \quad V_D > V_{Dsat}$$

$$\boxed{\frac{\Delta i}{i_i} = \frac{i_o - i_i}{i_i} \cong \frac{v_o - v_i}{V_A} \cong \frac{v_o - v_i}{V_E L}}$$

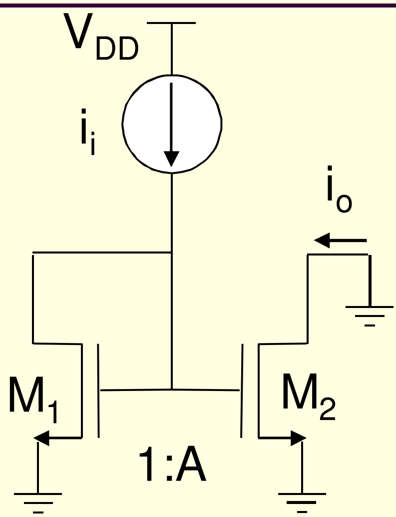
Error due to mismatch

$$\frac{\Delta I_D}{I_D} \cong \frac{1}{I_D}\left(\frac{\partial I_D}{\partial I_S}\Delta I_S + \frac{\partial I_D}{\partial V_{T0}}\Delta V_{T0}\right)$$

$$\cong \frac{\Delta I_S}{I_S} - \frac{g_m}{I_D}\Delta V_{T0}$$

$$\boxed{\frac{\sigma^2\left(\Delta I_D\right)}{I_D^2} = \left(\frac{g_m}{I_D}\right)^2 \sigma^2\left(\Delta V_T\right) + \frac{\sigma^2\left(\Delta I_S\right)}{I_S^2} = \frac{1}{WL}\left[\left(\frac{g_m}{I_D}\right)^2 A_{VT}^2 + A_{IS}^2\right]}$$

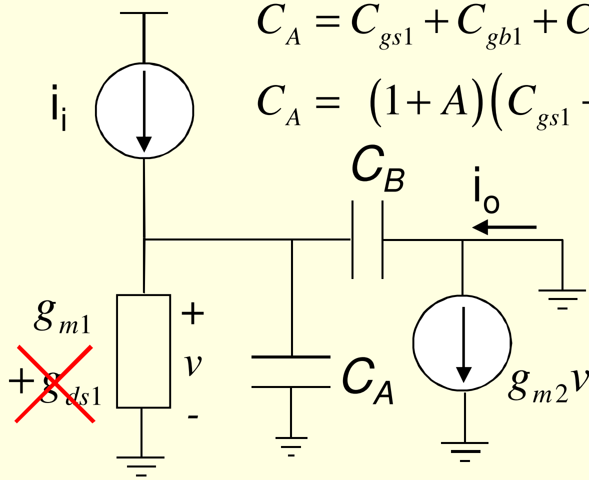
THE TWO-TRANSISTOR CURRENT MIRROR - 2



ac analysis

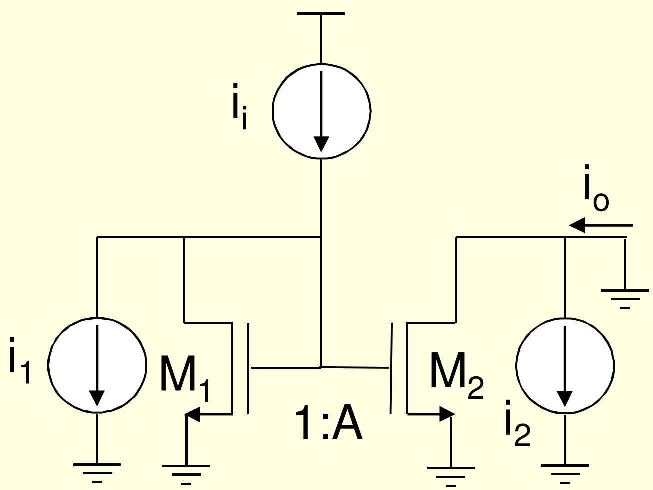
$$C_A = C_{gs1} + C_{gb1} + C_{gs2} + C_{gb2} + C_{db1} + C_B$$

$$C_A = (1+A)\left(C_{gs1} + C_{gb1}\right) + C_{db1} + C_{ovd2}$$



$$\frac{I_o}{I_i}(s) \cong \frac{A}{1+\tau s} \qquad \tau = \frac{C_A + C_B}{g_{m1}} \approx \frac{1+A}{2\pi f_T}$$

Noise analysis



Uncorrelated noise sources

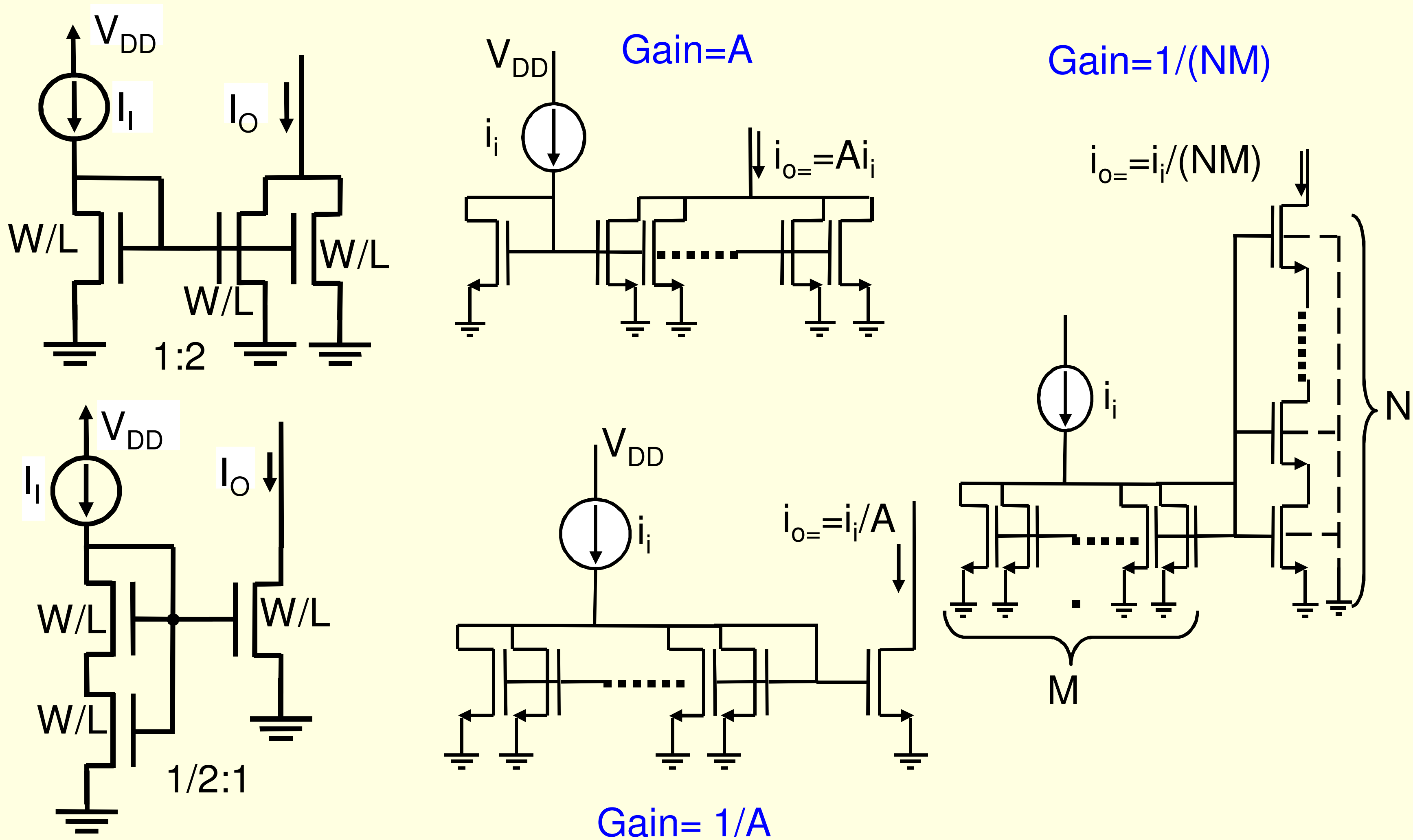
$$\overline{i_o^2} = \left(\overline{i_i^2} + \overline{i_1^2}\right)\left(\frac{g_{m2}}{g_{m1}}\right)^2 + \overline{i_2^2} \qquad \frac{g_{m2}}{g_{m1}} = A$$

$$\overline{i_o^2} = A^2\left(\overline{i_i^2} + \overline{i_1^2}\right) + A\overline{i_1^2}$$

The effect of M_1 on noise is A times greater than that of M_2

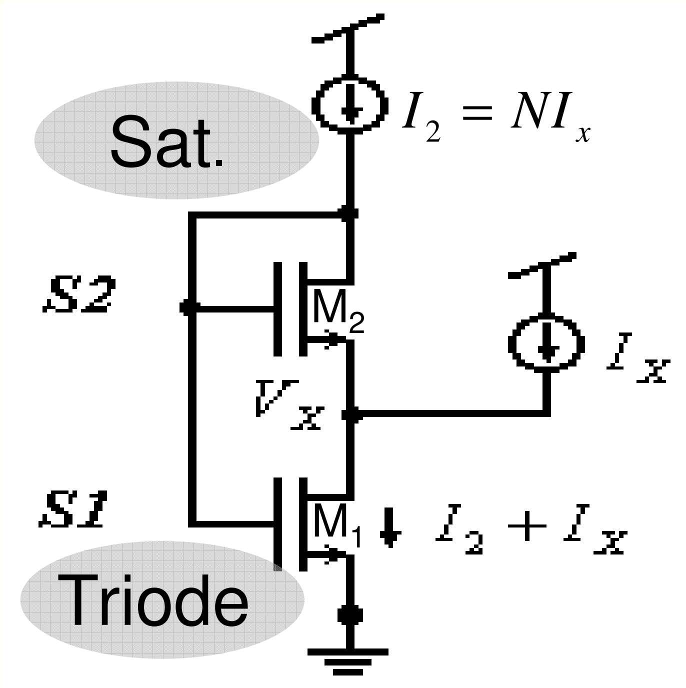
CURRENT MIRROR: GAIN SCHEMES

Gain-of-two current mirrors



A SELF-BIASED CURRENT SOURCE – 1

SELF-CASCODE MOSFET (SCM)



$$I_{S2}\left(i_{f2} - \cancel{i_{r2}}^{\,0}\right) = NI_x \qquad i_{f2} = i_{r1}$$

$$I_{S1}(i_{f1} - i_{f2}) = (N+1)I_x$$

$$\Downarrow$$

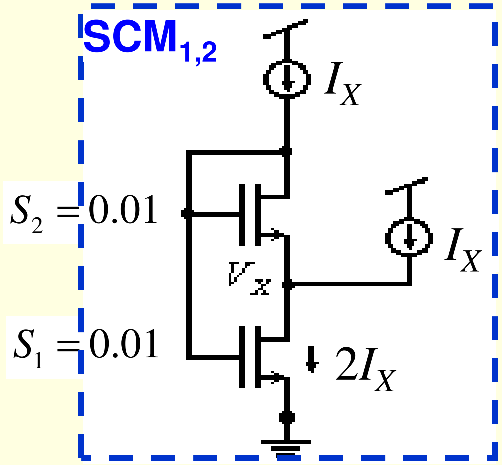
$$i_{f1} = \left[1 + \frac{S_2}{S_1}\left(1 + \frac{1}{N}\right)\right] i_{f2} = \alpha i_{f2}$$

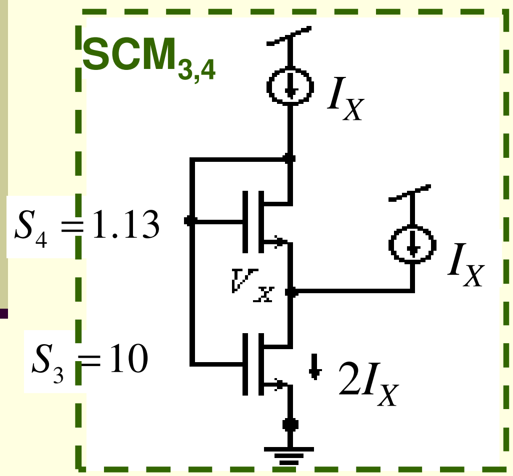
Applying UICM to both M_1 & M_2

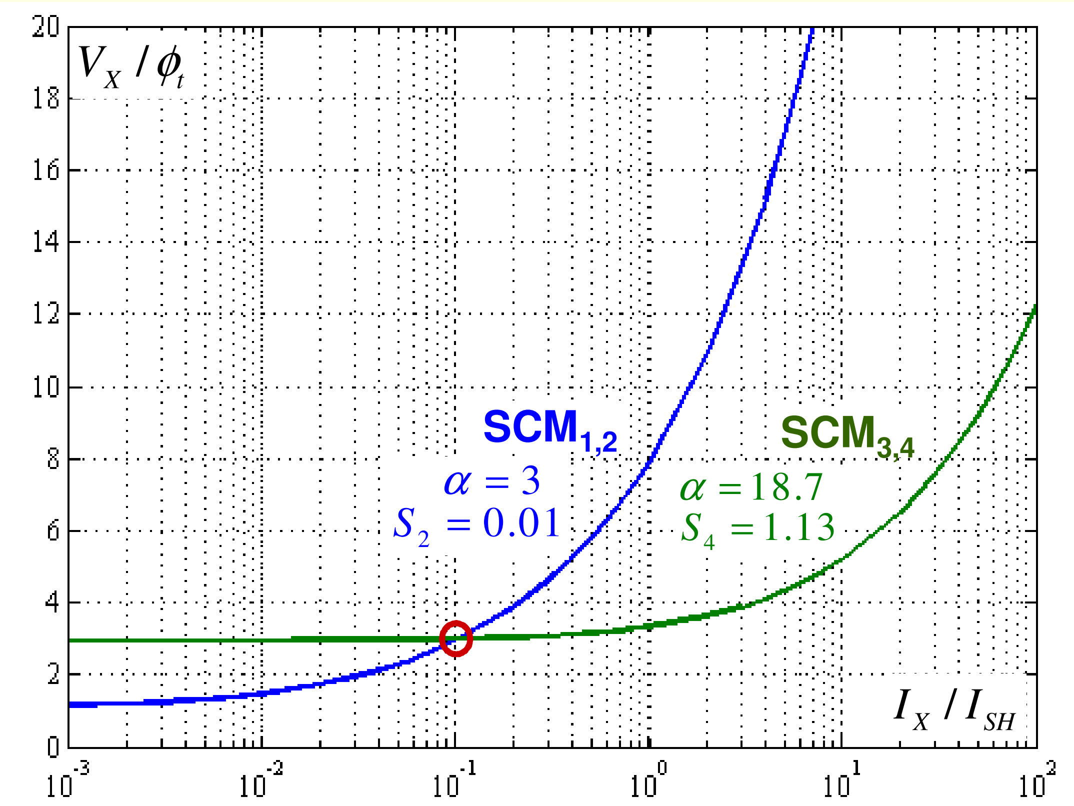
$$\boxed{\frac{V_X}{\phi_t} = \sqrt{1+\alpha i_{f2}} - \sqrt{1+i_{f2}} + \ln\left(\frac{\sqrt{1+\alpha i_{f2}}-1}{\sqrt{1+i_{f2}}-1}\right)}$$

where $\boxed{i_{f2} = \frac{NI_X}{I_{S2}} = \frac{NI_X}{S_2 I_{SH}}}$

A SELF-BIASED CURRENT SOURCE – 2





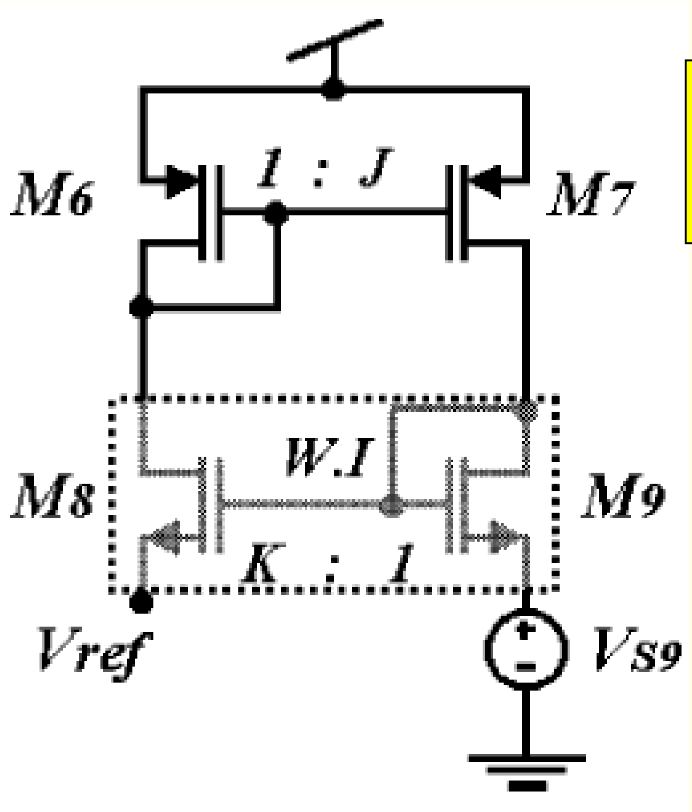


$$\alpha = 1 + \frac{S_{even}}{S_{odd}}\left(1 + \frac{1}{N}\right)$$

$$\frac{V_X}{\phi_t} = \sqrt{1 + \alpha \frac{I_X}{S_{even} I_{SH}}} - \sqrt{1 + \frac{I_X}{S_{even} I_{SH}}} + \ln\left(\frac{\sqrt{1 + \alpha \frac{I_X}{S_{even} I_{SH}}} - 1}{\sqrt{1 + \frac{I_X}{S_{even} I_{SH}}} - 1}\right)$$

A SELF-BIASED CURRENT SOURCE – 3

VOLTAGE FOLLOWING (NMOS) CURRENT MIRROR (PMOS)[1]



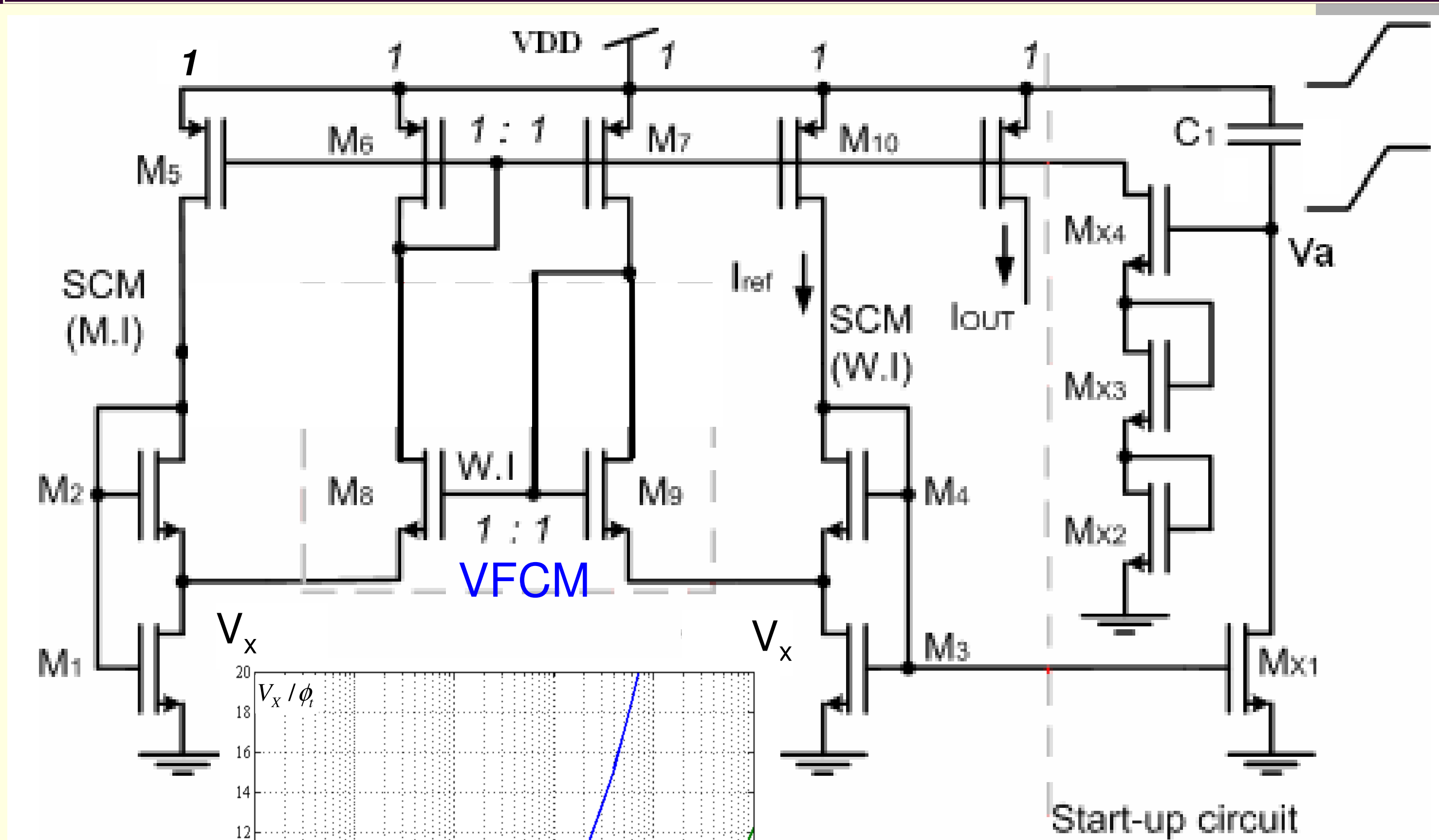
$$\frac{V_{ref} - V_{S9}}{\phi_t} = \sqrt{1 + JKi_{f8}} - \sqrt{1 + i_{f8}} + \ln\left(\frac{\sqrt{1 + JKi_{f8}} - 1}{\sqrt{1 + i_{f8}} - 1}\right)$$

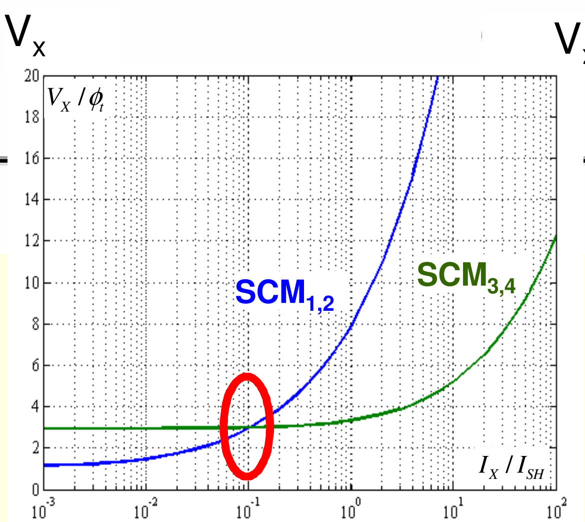
When both M_8 & M_9 operate in WI:

$$V_{ref} = V_{S9} + \phi_t \ln(JK)$$

[1] B. Gilbert, AICSP vol. 38, pp. 83-101, Feb. 2004

A SELF-BIASED CURRENT SOURCE – 4





VFCM is a positive feedback circuit ⟶ return ratio must be < 1 for stability

A SBCS – 5: DESIGN

Output current: I_{ref}=10 nA

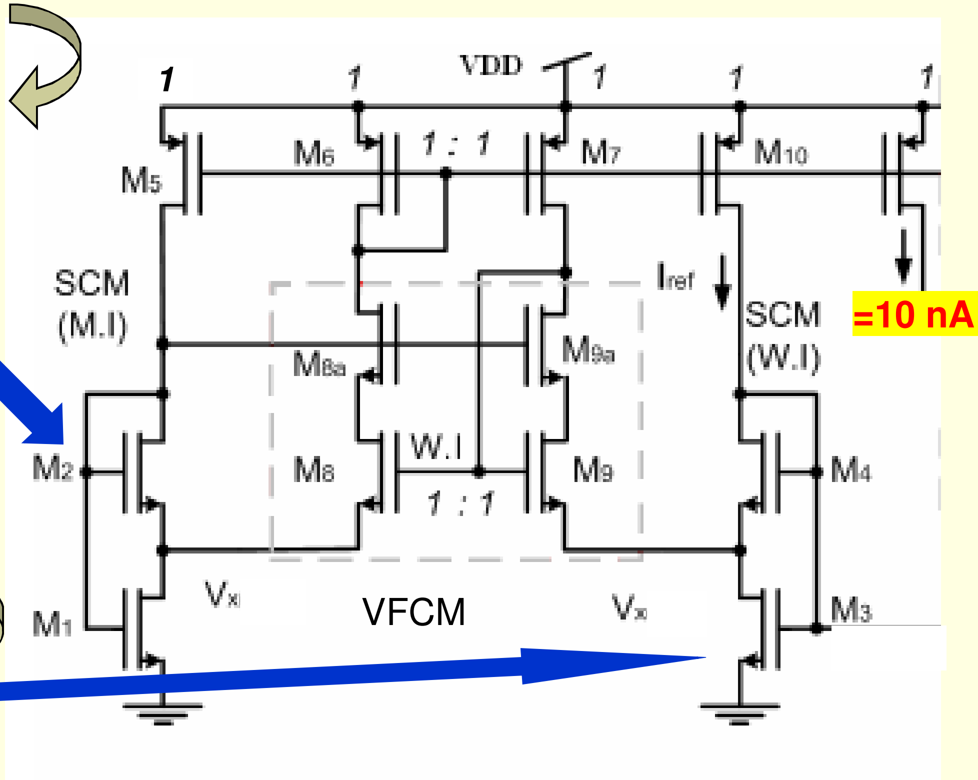
$I_{SHn\text{-}channel} \cong 100$ nA, $I_{SHp\text{-}channel} \cong 40$ nA

Let us choose $i_{f2} = 10$, $S_2 = S_1$

$$I_{S2} i_{f2} = 10 \text{ nA} \rightarrow I_{S2} = 1 \text{ nA} \rightarrow S_2 = S_1 = 0.01$$

$$\alpha_{1-2} = 1 + \frac{S_2}{S_1}\left(1 + \frac{1}{N}\right) = 3$$

$$\frac{V_X}{\phi_t} = \sqrt{1+30} - \sqrt{1+10} + \ln\left(\frac{\sqrt{1+30}-1}{\sqrt{1+10}-1}\right) = 2.93$$



Let us choose $i_{f3(4)} << 1$ (WI)

$$\frac{V_X}{\phi_t} \cong \ln \alpha_{3-4} \Rightarrow \alpha_{3-4} = e^{2.93} \cong 18.7$$

$$\alpha_{3-4} = 1 + \frac{S_4}{S_3}\left(1 + \frac{1}{1}\right) \Rightarrow \frac{S_4}{S_3} = 8.85$$

Let us choose $i_{f3} = 0.187 \rightarrow i_{f4} = i_{f3} / \alpha_{3-4} = 0.01$

$$I_{S4} i_{f4} = 10 \text{ nA} \rightarrow I_{S4} = 1\ \mu\text{A} \rightarrow S_4 = 10$$

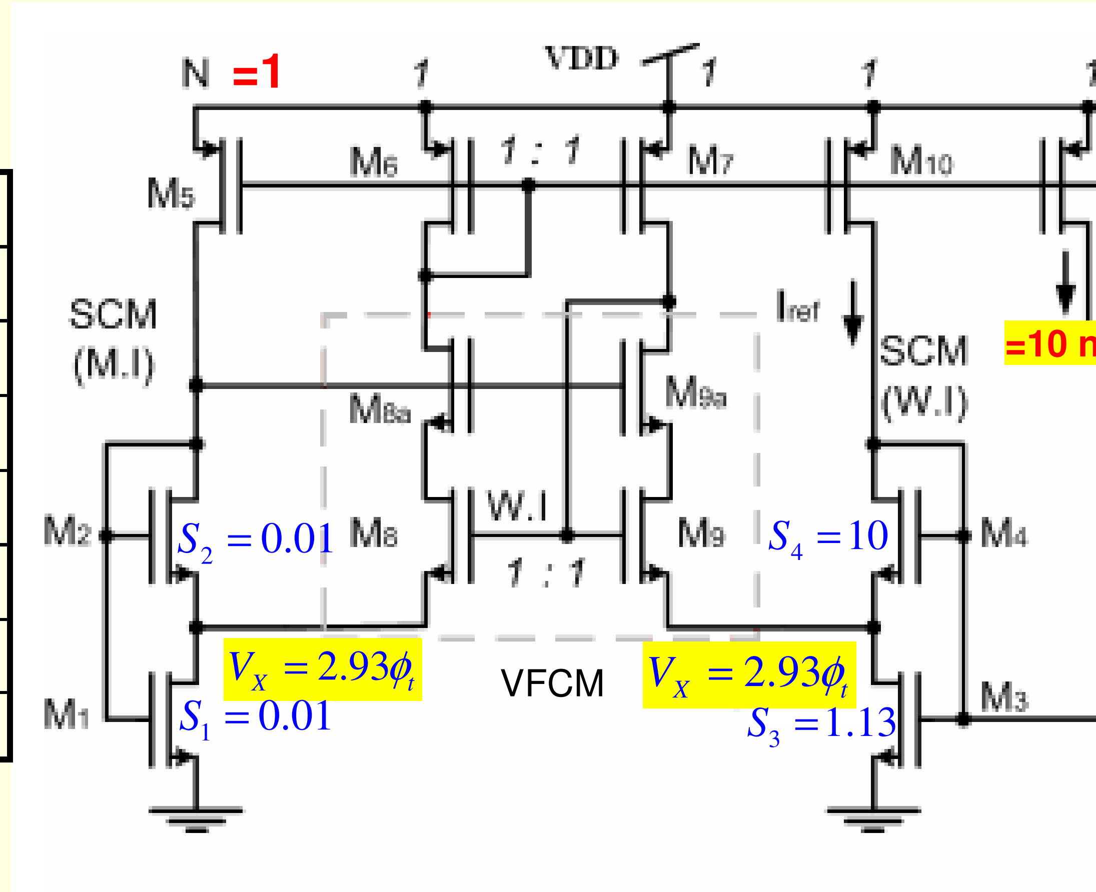
$$S_3 = \frac{S_4}{8.85} = 1.13$$

$$\boxed{\frac{V_X}{\phi_t} = \sqrt{1+\alpha i_{f2(4)}} - \sqrt{1+i_{f2(4)}} + \ln\left(\frac{\sqrt{1+\alpha i_{f2(4)}}-1}{\sqrt{1+i_{f2(4)}}-1}\right)}$$

A SBCS – 6: DESIGN

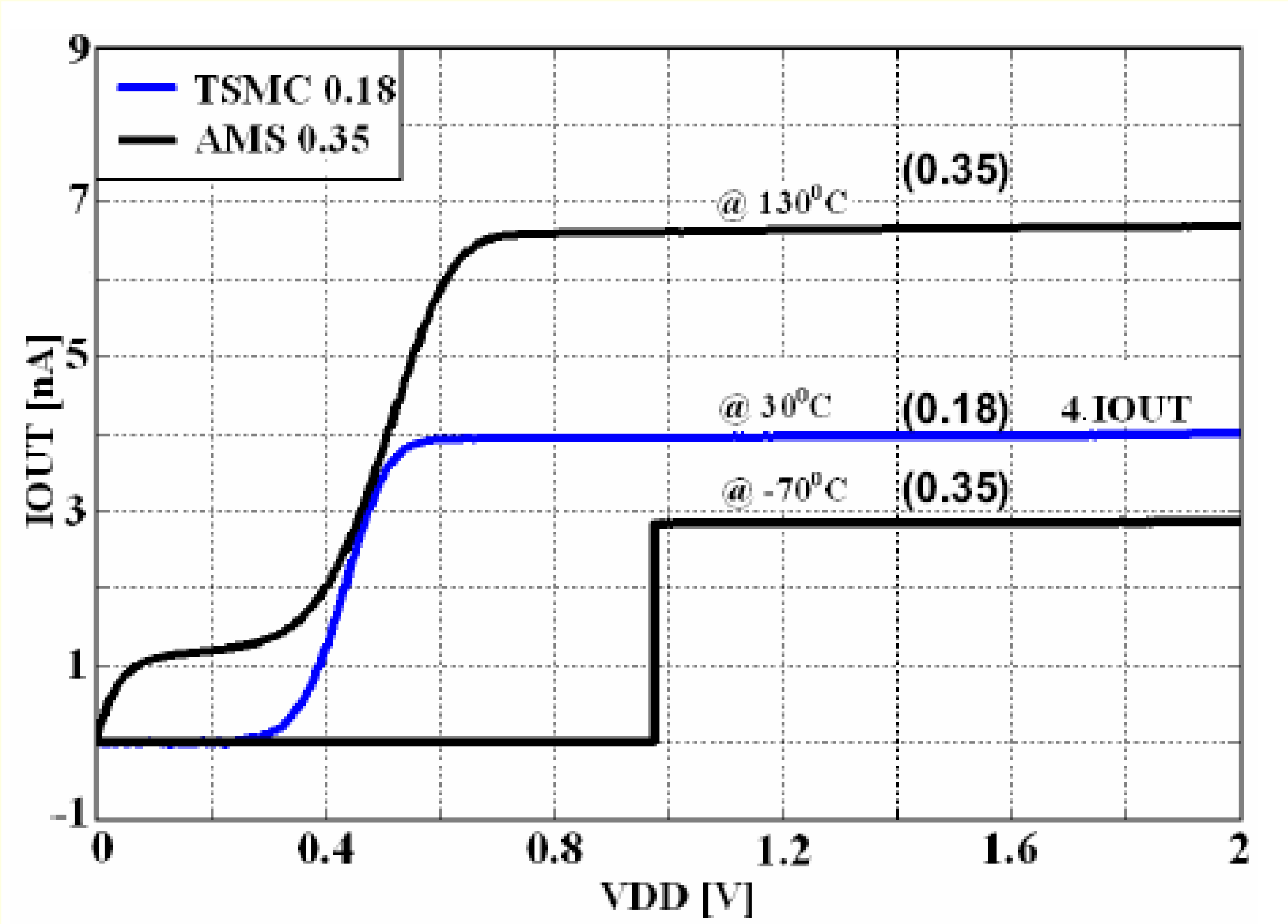
Summary

	S	i_f	i_r
M_1	0.01	30	10
M_2	0.01	10	0
M_3	1.13	0.187	0.01
M_4	10	0.01	0
M_8, $M_{8(a)}$	1	0. 1	0
M_9, $M_{9(a)}$	1	0. 1	0
M_P (all)	2.5	0.1	0

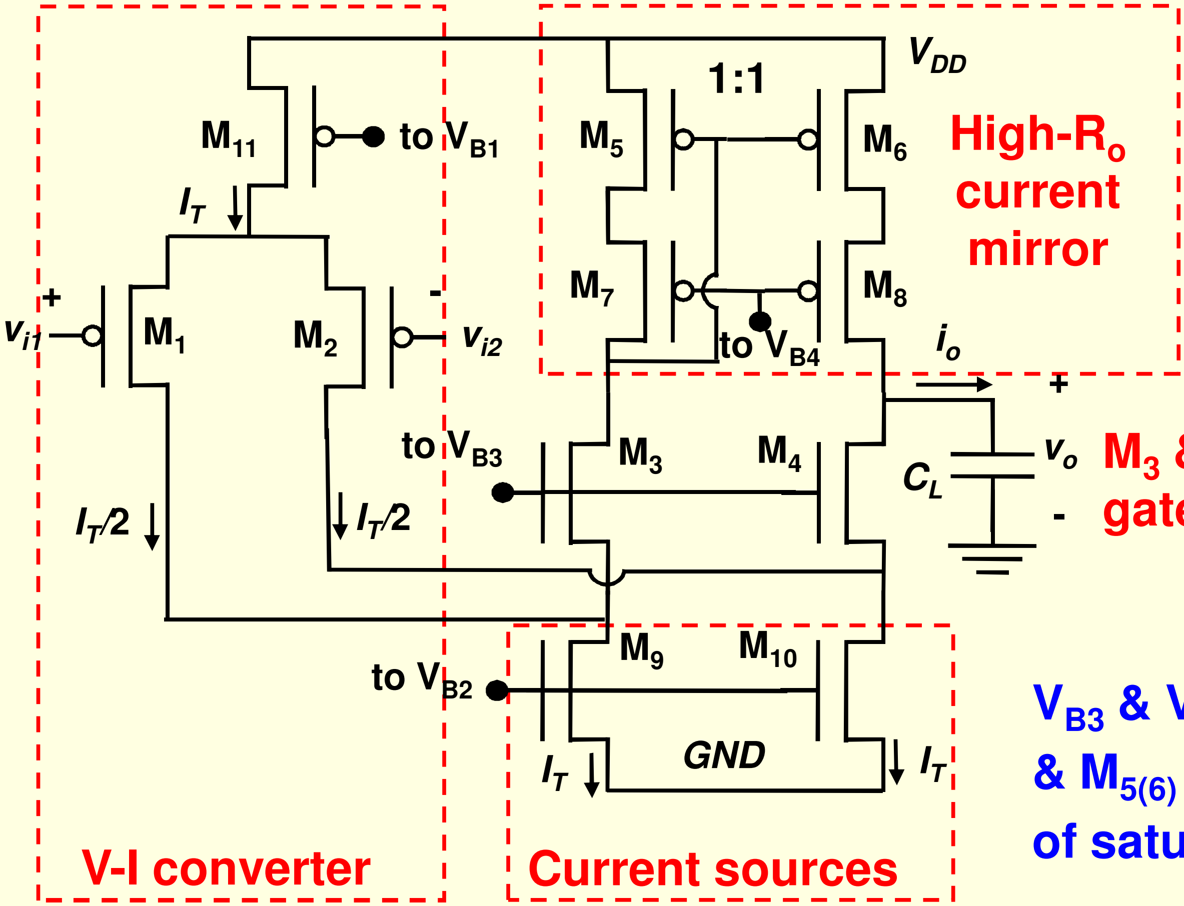


Core area in 0.35µm CMOS ≈ 0.02 mm²

A SBCS – 7 : I_{OUT} vs. V_{DD} AT CONSTANT T



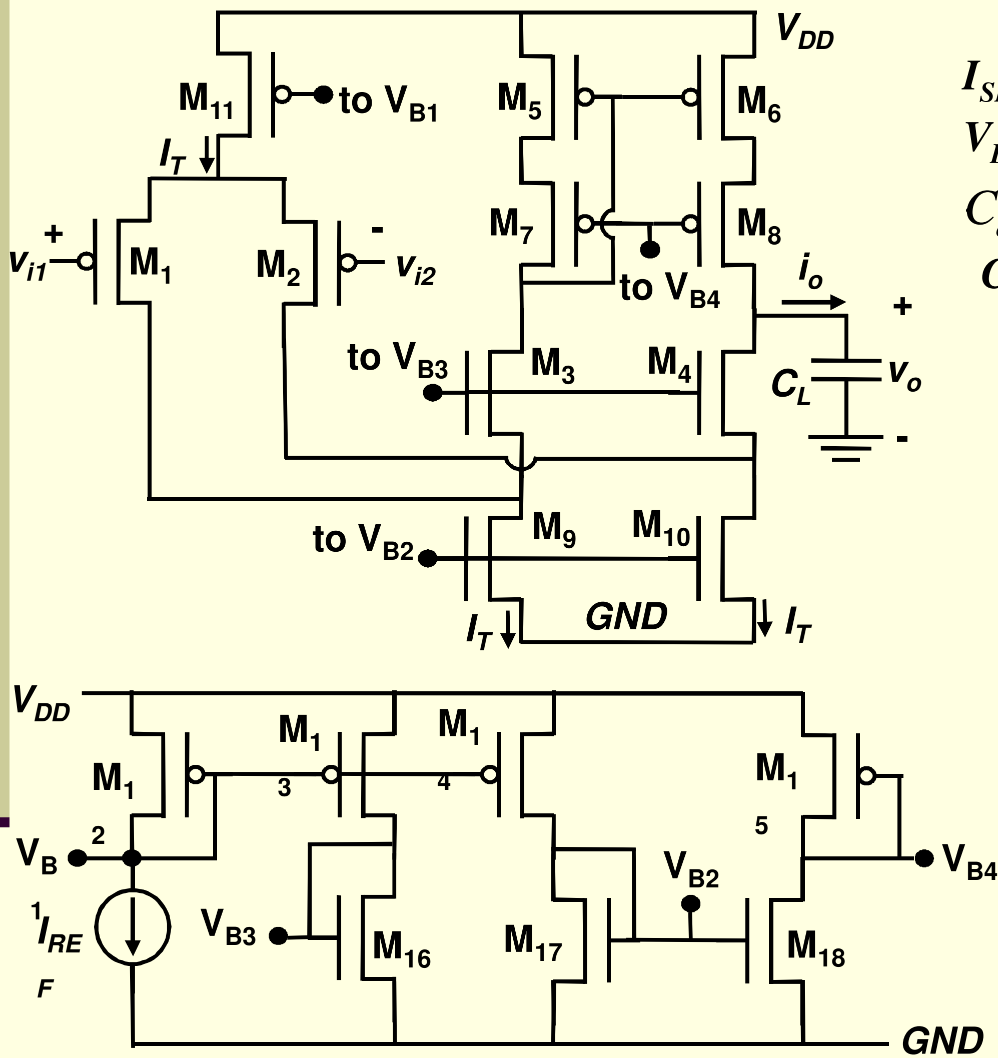
A FOLDED CASCODE AMPLIFIER - 1



M_3 & M_4 – common-gate configuration

V_{B3} & V_{B4} are such that $M_{9(10)}$ & $M_{5(6)}$ operate on the edge of saturation

A FOLDED CASCODE AMPLIFIER - 2



0.5 µm CMOS

$I_{SHN} \cong 40$ nA, $I_{SHP} \cong 16$ nA, $n_N \cong n_P \cong 1.2$,

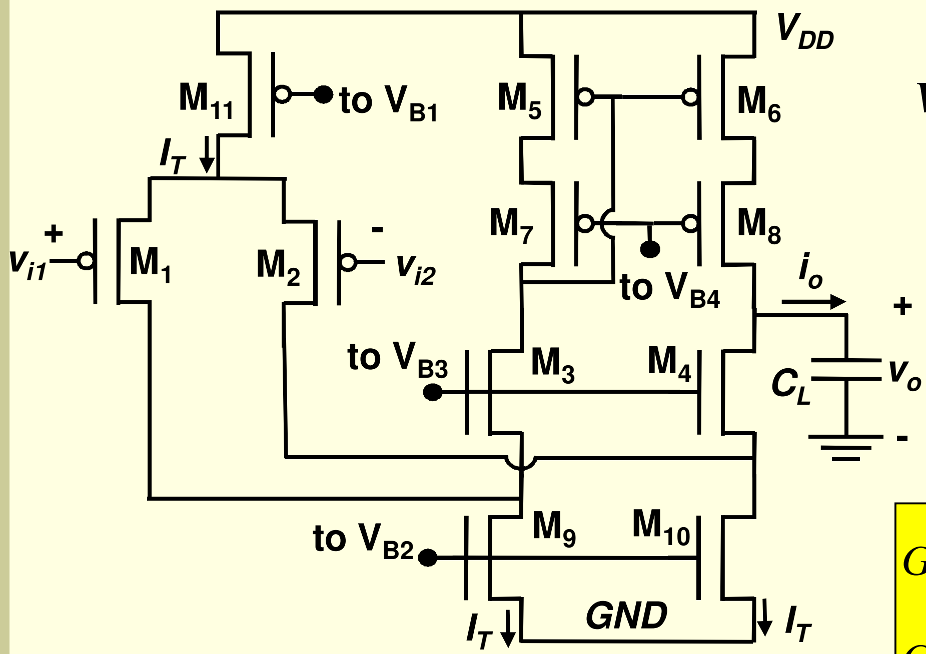
$V_{EN}=V_{EP}=10$ V/µm, $V_{T0N}=0.7$ V, $V_{T0P}=-0.9$ V,

$C'_{ox}=2.5$ fF/µm^2

$C_L=1$ pF, $V_{DD}=5$ V, $I_{REF}=0.6$ µA.

Transistor	W (µm)	L (µm)	I_D (µA)	i_f
M_1,M_2, M_5-M_8	12.5	1	3	15
M_3,M_4	5	1	3	15
M_9,M_{10}	10	1	6	15
M_{11}	25	1	6	15
M_{12}-M_{14}	10	4	0.6	15
M_{15}	6	16	0.6	100
M_{17}, M_{18}	4	4	0.6	15
M_{16}	7.5	50	0.6	100

A FOLDED CASCODE AMPLIFIER - 3



$I_{SHN} \cong 40$ nA, $I_{SHP} \cong 16$ nA, $n_N \cong n_P \cong 1.2$,
$V_{EN}=V_{EP}=10$ V/µm, $C'_{ox}=2.5$ fF/µm², $C_L=1$ pF

Amplifier transconductance

$$\boxed{g_{m1} = \frac{2I_{SHP}(W/L)_1}{n\phi_t}\left(\sqrt{1+i_{f1}}-1\right)} = 40\ \mu\text{A/V}$$

Output conductance

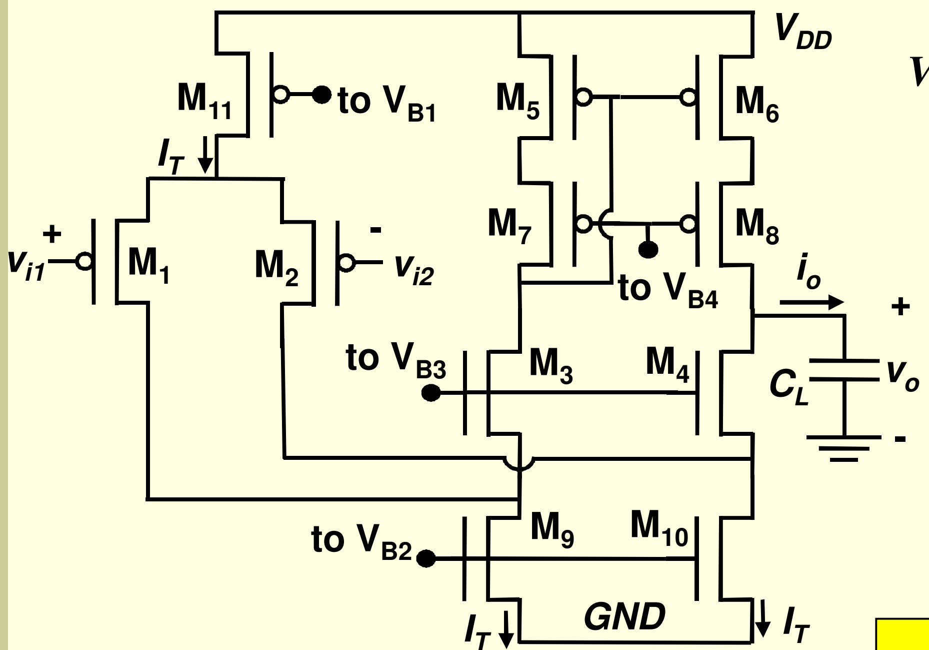
$$\boxed{G_o \cong \frac{g_{ds10}+g_{ds2}}{g_{ms4}/g_{ds4}} + \frac{g_{ds6}}{g_{ms8}/g_{ds8}} = \frac{0.6+0.3}{48/0.3} + \frac{0.3}{48/0.3} \qquad G_o \cong 7.5\text{ nA/V}}$$

Transistor	W (µm)	L (µm)	I_D (µA)	i_f
M_1,M_2, M_5-M_8	12.5	1	3	15
M_3,M_4	5	1	3	15
M_9,M_{10}	10	1	6	15

Voltage gain

$$\boxed{A_{V0} = g_{m1}/G_o \cong 5,330\text{ V/V}}$$

A FOLDED CASCODE AMPLIFIER - 4



$I_{SHN} \cong 40$ nA, $I_{SHP} \cong 16$ nA, $n_N \cong n_P \cong 1.2$,
$V_{EN}=V_{EP}$=10 V/µm, C'_{ox} =2.5 fF/µm², C_L=1 pF

Gain-bandwidth product

$$GB = g_{m1}/C_L = 40/1 \ \ \mu\text{A/V/pF} = 40 \text{ Mrad/s}$$ (*)

Slew rate

$$SR = \left.\frac{\Delta V_o}{\Delta t}\right|_{\max} = \frac{I_T}{C_L} = 6 \ \ \text{V}/\mu\text{s}$$

Offset voltage

$$\sigma^2(V_{OS}) \cong \sigma^2(V_{T01}) + \left(\frac{g_{m5}}{g_{m1}}\right)^2 \sigma^2(V_{T05}) + \left(\frac{g_{m9}}{g_{m1}}\right)^2 \sigma^2(V_{T09})$$

$$\sigma^2(V_{T0}) = A_{VT}^2/WL; \quad A_{VT} = 10 \text{ mV}\cdot\mu\text{m}$$
$$g_{m5}/g_{m1} = 1 \qquad g_{m9}/g_{m1} = 2$$
$$\sigma^2(V_{T01,5,9}) = 8,\ 8,\ 10 \ \ \text{mV}^2 \rightarrow \sigma(V_{OS}) \cong 7.5 \text{ mV}$$

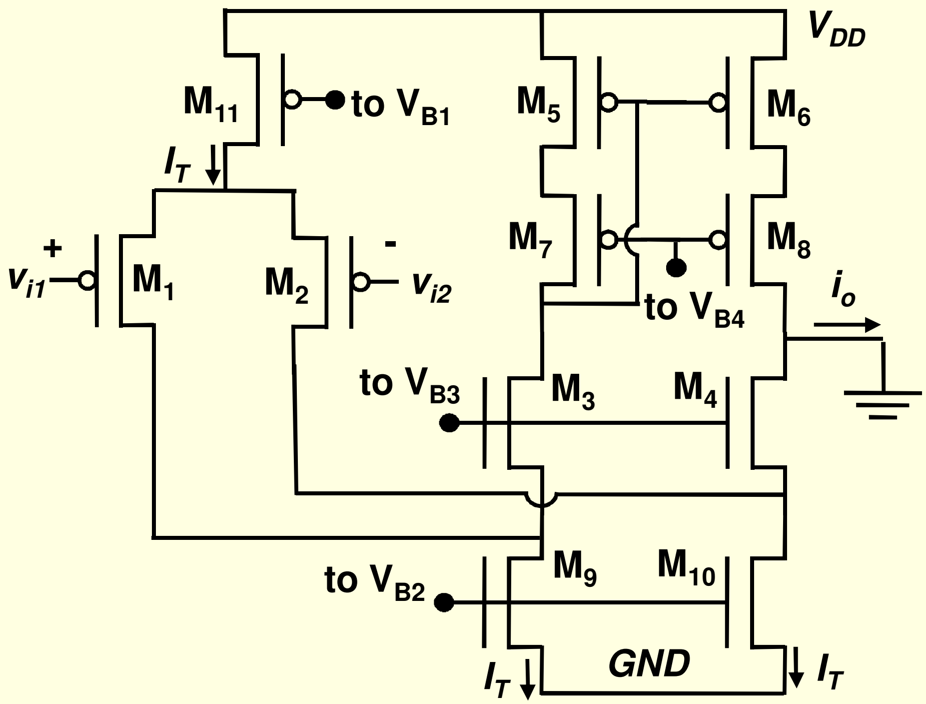
Transistor	W (µm)	L (µm)	I_D (µA)	i_f
M_1,M_2, M_5-M_8	12.5	1	3	15
M_3,M_4	5	1	3	15
M_9,M_{10}	10	1	6	15

Pairs M_3-M_4 & M_7-M_8 contribute negligibly to the offset voltage

(*) : For this design I_T=2.5*I_{Tmin}

A FOLDED CASCODE AMPLIFIER - 5

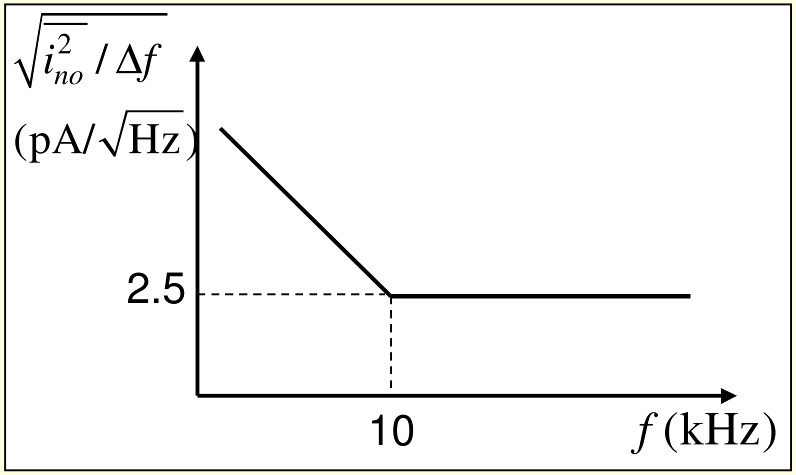
NOISE ANALYSIS

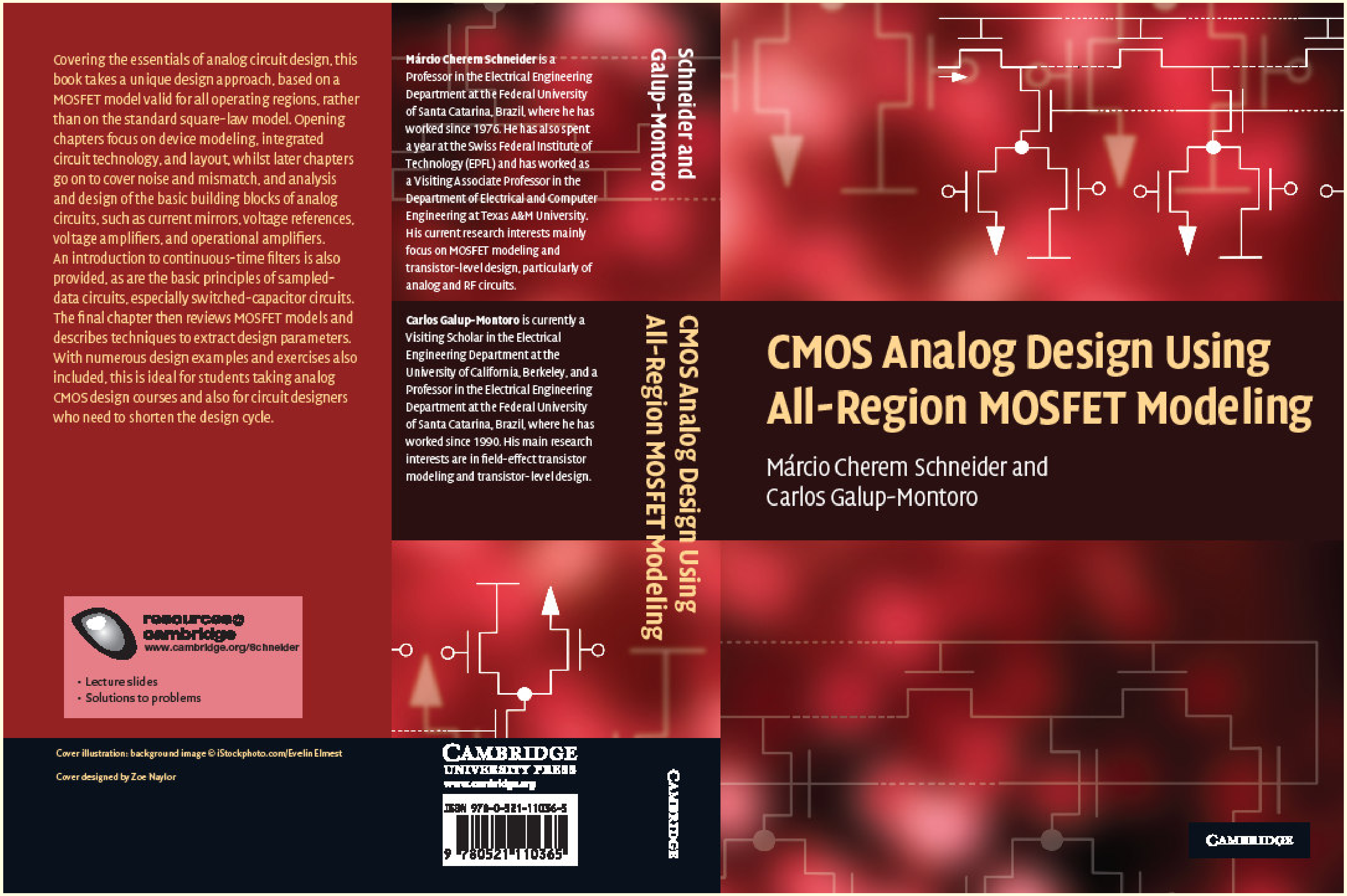


PSD of the output noise current

$$\frac{\overline{i_{no}^2}}{\Delta f} \cong 2\left(\frac{\overline{i_{n1}^2}}{\Delta f}+\frac{\overline{i_{n5}^2}}{\Delta f}+\frac{\overline{i_{n9}^2}}{\Delta f}\right)$$

Pairs M_3-M_4 & M_7-M_8 contribute negligibly to amplifier noise




Covering the essentials of analog circuit design, this book takes a unique design approach, based on a MOSFET model valid for all operating regions, rather than on the standard square-law model. Opening chapters focus on device modeling, integrated circuit technology, and layout, whilst later chapters go on to cover noise and mismatch, and analysis and design of the basic building blocks of analog circuits, such as current mirrors, voltage references, voltage amplifiers, and operational amplifiers. An introduction to continuous-time filters is also provided, as are the basic principles of sampled-data circuits, especially switched-capacitor circuits. The final chapter then reviews MOSFET models and describes techniques to extract design parameters. With numerous design examples and exercises also included, this is ideal for students taking analog CMOS design courses and also for circuit designers who need to shorten the design cycle.
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