A Precision Trim Technique for Monolithic Analog Circuits

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Abstract—A technique for permanent adjustment of precision analog circuits at wafer test by selective shorting of Zener diodes is presented. Analytical details of the trimming procedure and a physical description of diode short-circuiting are given. The method is applied to a precision operational amplifier with input offset voltage reduced to 10 μV. The necessity of optimizing other related parameters is demonstrated. Practical considerations limiting wafer test accuracy are discussed. Circuit performance is summarized.

Introduction

THE character of the monolithic analog circuit is essentially established once it has emerged from wafer processing. Hybrid and modular devices, on the other hand, usually undergo some adjustment procedure before final assembly. These facts explain why monolithic IC's enjoy significant cost advantages, while hybrid and modular circuits have the potential for better performance. To bridge this performance gap, several trim techniques for monolithic devices have been developed in recent years, resulting in the adjustment and improvement of a critical variable.

Laser trimming has received the most attention of all of these schemes. Although most of the early technical problems are apparently being solved [1], laser adjustment sacrifices some of the cost advantages of the monolithic process. It does require a high initial investment for equipment that can only be applied to thin or thick film resistors (more expensive to manufacture than diffused resistors). In most cases the adjustment cannot be made at wafer test, but only after the device has been die-attached and bonded—further increasing costs.

Trimming with fusible links is a well-established procedure, primarily for programming memories. However, it also needs additional processing steps for the formation of the fuse. Several attempts have been made [2], [3] to use standard linear process metal (1000-Å thick aluminum) as fusible links. Although the production-worthiness of this scheme is difficult to judge, metal regrowth due to electromigration and/or thermal expansion [4] after the fuse is blown is a possible problem area. In addition, the current levels required are in the ampere range resulting in a fast deterioration of the wafer test probes and unsightly—and therefore often unacceptable—blown metal connections.

The selective shorting of emitter-base diodes (in the avalanche or Zener mode) to adjust monolithic circuits does not require extra processing, it can be implemented at the wafer test phase, with minimal increase in manufacturing cost. The shorting of diodes for programming circuits was first proposed in 1962 [5] and used extensively in digital circuits since then. Analog designs employing this trimming method have appeared only recently. Examples are an FET operational amplifier [6] developed concurrently with the precision op amp described below [7], and other unpublished, and therefore unsubstantiated, applications.

In the following sections a trim technique utilizing shorted diodes and its application to a precision operational amplifier are described. Details of the diode shorting procedure are delineated in the Appendix.

Manuscript received May 16, 1975; revised July 14, 1975. This paper was presented at the International Solid-State Circuits Conference, Philadelphia, Pa., February 1975.

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Offset Voltage Adjustment

Improvements in monolithic operational amplifier design have decreased the input referred error contribution of most parameters, such as bias and offset currents, common-mode and power-supply rejection, voltage gain, to the order of microvolts. One exception has been input offset voltage (V_{os}). Even a V_{os} of a few hundred microvolts will dominate the error budget, and thus represents an unacceptably large error term in many applications. External V_{os} adjustment by potentiometers is expensive and potentially unreliable. In addition, field-servicing is difficult, since the faulty device cannot be replaced by a substitute without extensive recalibration. Permanent V_{os} adjustment at wafer test eliminates all of the above difficulties.

The equivalent circuit of Fig. 1 represents an operational amplifier with a resistor-loaded input stage. Offset voltage is defined by

$$V_{os} = (V_{BE1} - V_{BE2})\Big|_{V_{out}=0} = \frac{kT}{q} \ln \frac{I_1}{I_2} \frac{I_{s2}}{I_{s1}}. \quad (1)$$

I_{s1} and I_{s2} are saturation currents of $Q1$ and $Q2$, respectively.

If V_{os2}, the offset voltage of the second stage $\ll I_1 R_L$, then $I_1 R_L = I_2 R_R$ and (1) reduces to

$$V_{os} = \frac{kT}{q} \ln \frac{R_R}{R_L} \frac{I_{s2}}{I_{s1}}. \quad (2)$$

Hence, the causes of V_{os} are readily identified as mismatches between R_R and R_L, I_{s1}, and I_{s2}.

V_{os} can be altered by changing the ratio R_R/R_L, and, in particular, if $(R_R/R_L)(I_{S2}/I_{S1}) = 1$, V_{os} will be zero.

Offset trim at wafer test is accomplished by the additional circuitry of Fig. 2. Zener diodes Z_0 to Z_n are normally nonconducting. The differential stage is balanced, since nominally:

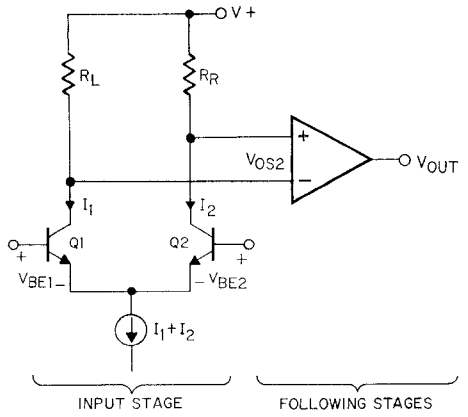

Fig. 1. Equivalent circuit of operational amplifier.

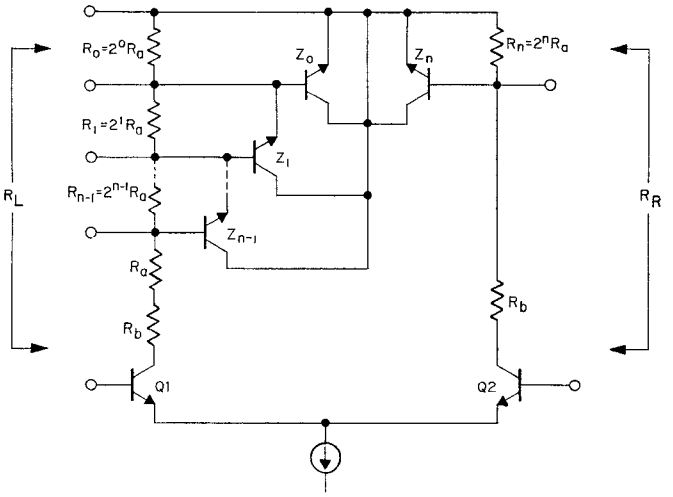

Fig. 2. Offset adjustment by selective shorting of Zener diodes.

$$R_L = R_b + R_a(1 + 2^0 + 2^1 + \cdots + 2^{n-1}) = R_b + 2^n R_a = R_R. \tag{3}$$

V_{os} is adjusted by the selective shorting of Z_0 to Z_n. Irrespective of the Z_i shorted, the resistance difference between the two sides, $\Delta R \equiv R_L - R_R \leqslant 2^n R_a$. If $2^n R_a \ll R_b$, and since $R_b \leqslant R_L$, the change in V_{os}, ΔV_{os}, from (2) is

$$\Delta V_{os} = \frac{kT}{q} \ln \frac{R_L + \Delta R}{R_L} \simeq \frac{kT}{q} \frac{\Delta R}{R_L}. \tag{4}$$

The following equations describe the maximum and minimum changes in V_{os} in the positive (ΔV_{os}^+ max, ΔV_{os}^+ min) and negative (ΔV_{os}^- max, ΔV_{os}^- min) directions. Because of the conclusions of (4), all equations can be reduced from a logarithmic to a linear form.

If $Z_0, Z_1, \cdots, Z_{n-1}$ are shorted,

$$\Delta V_{os}^+ \max = \frac{kT}{q} \ln \frac{R_b + 2^n R_a}{R_b + R_a} \simeq \frac{kT}{q}(2^n - 1)\frac{R_a}{R_b}. \tag{5}$$

If Z_n is shorted,

$$\Delta V_{os}^- \max = \frac{-kT}{q} \ln \left(1 + 2^n \frac{R_a}{R_b}\right) \simeq \frac{-kT}{q} 2^n \frac{R_a}{R_b}. \tag{6}$$

If Z_0 is shorted,

$$\Delta V_{os}^+ \min = \frac{kT}{q} \ln \frac{R_b + 2^n R_a}{R_b + (2^n - 1)R_a} \simeq \frac{kT}{q} \frac{R_a}{R_b}. \tag{7}$$

If all Zeners are shorted,

$$\Delta V_{os}^- \min = \frac{-kT}{q} \ln \left(1 + \frac{R_a}{R_b}\right) \simeq \frac{-kT}{q} \frac{R_a}{R_b}. \tag{8}$$

If the initial, unadjusted V_{os} varies between

$$-(\Delta V_{os}^+ \max + \tfrac{1}{2} \Delta V_{os}^+ \min) \leqslant V_{os} \leqslant -(\Delta V_{os}^- \max + \tfrac{1}{2} \Delta V_{os}^- \min), \tag{9}$$

then V_{os} can be changed by appropriately selected shorting of Z_i to

$$\tfrac{1}{2} \Delta V_{os}^- \min \leqslant V_{os} \leqslant \tfrac{1}{2} \Delta V_{os}^+ \min. \tag{10}$$

From (5)-(10) all negative V_{os} values can be improved $(2^{n+1} - 1)$ times, all positive offset voltages $(2^{n+1} + 1)$ times.

The discussion above is concerned specifically with operational amplifiers. However, the conclusions are quite general and can be directly applied to other types of analog circuits, such as comparators, instrumentation amplifiers, and analog multipliers.

Precision Operational Amplifier

As a specific example, a precision operational amplifier[1] was designed with $R_a = 230\ \Omega$, $R_b = 50\ \text{k}\Omega$, $n = 3$. Assuming $kT/q = 26$ mV at room temperature, from (7) and (8)

$$\Delta V_{os}^+ \min \simeq -\Delta V_{os}^- \min = 120\ \mu\text{V}.$$

From (5)

$$\Delta V_{os}^+ \max \simeq 840\ \mu\text{V}.$$

From (6)

$$\Delta V_{os}^- \max \simeq -960\ \mu\text{V}.$$

Therefore, from (9) and (10) offset voltages ranging from $-900\ \mu$V to $+1020\ \mu$V can be improved to $-60\ \mu\text{V} \leqslant V_{os} \leqslant 60\ \mu$V. Offset voltage reduction is accomplished by dividing the untrimmed V_{os} range into sixteen equal, $120\ \mu$V wide, sorting sections, each one is covered by one of the sixteen shorting combinations available from Z_0, Z_1, Z_2, and Z_3.

Practical considerations govern the selection of both the maximum boundaries of adjustment, and the resultant V_{os}. The approximately ± 1-mV range was chosen because most of the devices manufactured fall within these limits. In addition, those few units with V_{os} exceeding 1 mV are not considered

[1] Precision Monolithics mono OP-07 technical data, June 1974.

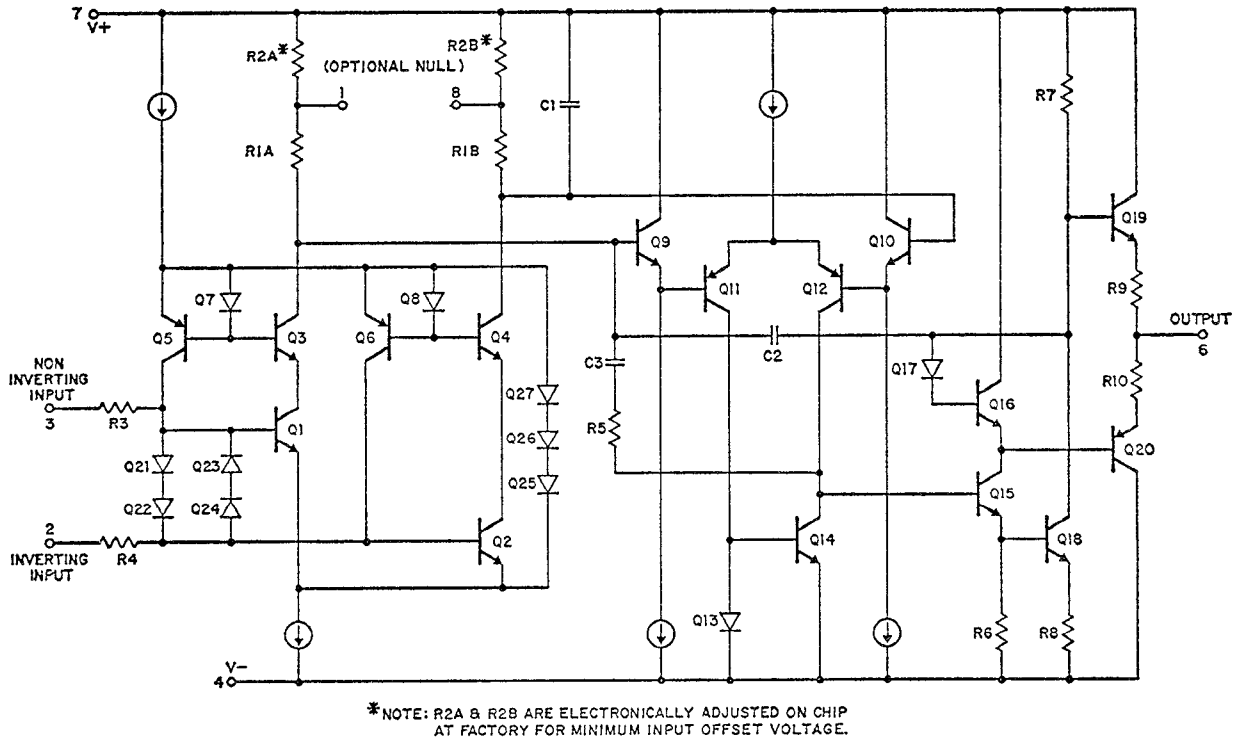

Fig. 3. Simplified schematic of complete operational amplifier.

to have adequate reliability for a final specification of less than 60 μV. In other words, the device must have some serious imperfection, leading to the relatively high-offset voltage. One more Zener diode could have been used to lower the trimmed limits to ± 30 μV. However, several error terms, each amounting to 3 to 10 μV, would negate the possible benefits of a ± 30-μV reduced range. These are measurement inaccuracies at wafer test; changes through assembly, particularly due to die-attach; increased chip temperature in the packaged device; warm-up drift, since by necessity the amplifier is measured a few milliseconds after turnon at wafer test.

The procedure at wafer sort starts with the measurement of V_{os} by an automated tester; if V_{os} is within the adjustable range, the appropriate preprogrammed Zener diode combination is shorted. The heat generated in the fused Zener diodes (see Appendix) creates a pattern of thermal gradients across the chip. Although the isothermal layout with cross-connected input devices (Fig. 4) eliminates most of the temperature differentials, the measurement of V_{os} to microvolt accuracies would still be effected. The test sequence is organized to evaluate less sensitive parameters immediately after Zener shorting, and thus, several hundred milliseconds elapse before V_{os} is remeasured, allowing the gradients to decay.

Since the V_{os} of most devices is less than 60 μV, a prime grade with 25 μV of guaranteed offset voltage can be defined with reasonable yields. However, a 25-μV V_{os} specification is meaningful only if two other V_{os}-related parameters are optimized: V_{os} drift with temperature (TCV_{os}) and time (V_{os}/t). Even relatively good TCV_{os} or V_{os}/t performance, such as 2 μV/°C and 20 μV/month can render the initial offset voltage guarantee worthless with temperature and time variations. A monolithic operational amplifier [8], which has been in production for years, has excellent input specifications, including TCV_{os} and V_{os}. Therefore, its basic design was retained, with the trimming circuitry of Fig. 2 added to facilitate V_{os} adjustment.

A simplified schematic is shown in Fig. 3. The asterisks of $R2A$ and $R2B$ indicate that these resistors were altered at wafer test using the technique described above.

The three-stage amplifier is internally compensated with feedforward capacitor C_3. C_2 sets the dominant pole. Low bias currents are achieved with the bias current cancellation network of $Q1$, $Q3$, $Q5$, $Q7$ and $Q2$, $Q4$, $Q6$, $Q8$. Additional circuit design details are described in [8].

The photomicrograph of the device (Fig. 4) illustrates the symmetrical layout [9] which is essential for precision operational amplifier design. The cross-coupled input transistor connection on the left side of the chip cancels gradients due to wafer processing and thermal effects generated by variations in power dissipation in the driver and output stages located on the right side of the device. Fig. 5 shows an enlarged view of the trimming circuitry. The chip area assigned to the pads contacting the four Zener diodes is larger than the area of the diodes themselves, due to the fact that the Zeners are in a common isolation pocket. Since as many as eight pads could be employed to contact four shorting diodes, another advantage of the trim technique of Fig. 2 is the significant area reduction represented by the use of only four pads in addition to the ones needed for device operation.

Circuit Performance

The performance attained with this design is detailed in Table I. The 25-μV guaranteed offset voltage (60 μV maximum over the -55°C to 125°C temperature range) no longer

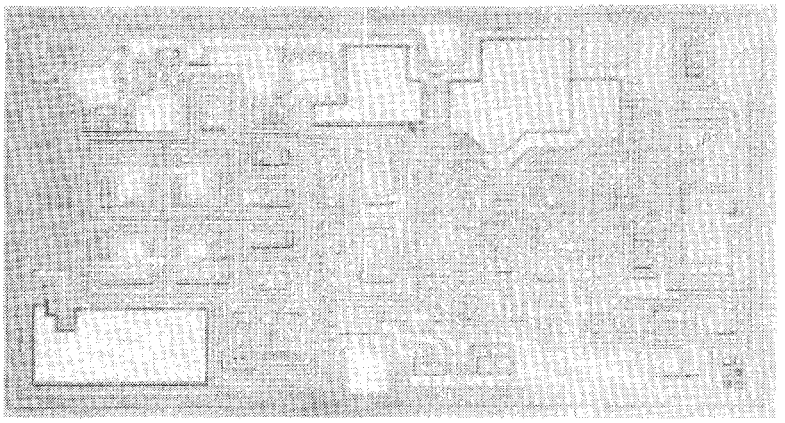

Fig. 4. Chip photomicrograph of precision operational amplifier (100 X 53 mils^2).

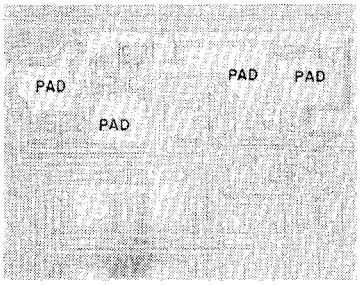

Fig. 5. Detailed view of trimming circuitry.

TABLE I

PRECISION OPERATIONAL AMPLIFIER PERFORMANCE @ $V_S = \pm 15V$, $T_A = 25°C$

PARAMETER	TYPICAL	MIN/MAX	UNITS
Offset voltage, V_{os}	10	25	μV
drift with temperature	0.2	0.6	μV/°C
drift with time	0.2	1.0	μV/mo
Offset current, I_{os}	0.3	2.0	nA
drift with temperature	5	25	pA/°C
Input bias current, I_B	0.7	2.0	nA
drift with temperature	8	25	pA/°C
Noise voltage 0.1 Hz to 10 Hz	0.35	0.6	μV p-p
Noise current 0.1 Hz to 10 Hz	14	30	pA p-p
Input resistance--differential	80	30	MΩ
Input resistance--common mode	200	--	GΩ
Common-mode rejection	126	110	dB
Power supply rejection	110	100	dB
Voltage gain	500	300	V/mV
Slew rate	0.25	--	V/μsec
Unity gain bandwidth	1.2	--	MHz

dominates the error budget. Indeed, a worse case 25°C dc analysis of the voltage follower circuit of Fig. 6 shows that the individual error contributions of V_{os}, bias current, voltage gain, common-mode and power supply rejection all are within 20 μV and 33 μV. Therefore, offset voltage has been successfully reduced to the level of other error sources.

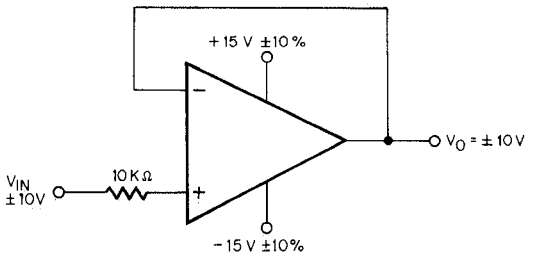

Fig. 6. Voltage follower circuit for error analysis.

Reliability

Reliability data for shorted Zeners are claimed [6] to be superior to other trimming methods. For the precision operational amplifier reliability is further enhanced by the fact that the shorted diodes only carry 8 μA, the input stage current of the amplifier.

In excess of 200 000 device-hours of operation at 125°C yielded only one failure. The cause was unrelated to the trimming circuitry. In general, reliability differences between the device and its predecessor without shorted diodes described in [8] are indistinguishable, providing additional proof of the basic soundness of the offset adjustment scheme.

Conclusion

A precision trim technique which has significantly improved the performance of a monolithic operational amplifier has been described. It is a general method; therefore it can be

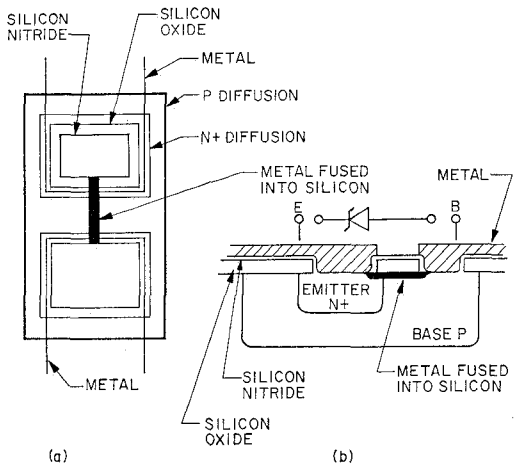

Fig. 7. Short-circuiting of Zener diodes. (a) Top view. (b) Side view.

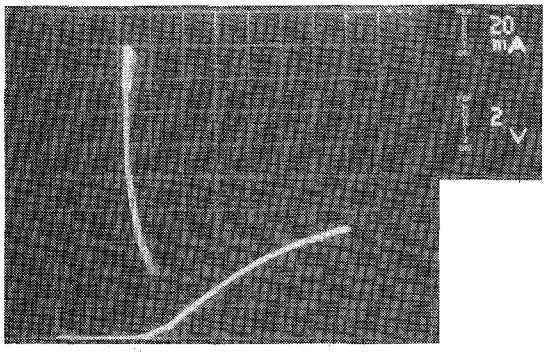

Fig. 8. Curve-tracer photograph of Zener diodes being shorted.

used to adjust other types of analog circuits. On wafer trimming, however, it is not a panacea: careful attention must be paid to other parameters, before the full benefits of the technique can be realized.

Appendix

When large current is passed through the emitter-base diode in the avalanche-mode, the localized power dissipation at the junction reaches such a magnitude that the junction will be destroyed. As shown in Fig. 7, a narrow link of metal fused into the silicon will be created. In addition, due to the large electric field present, metal will be swept across the silicon surface, beneath the oxide layer. In effect, a double short is produced: one as a result of the destroyed junction, the other due to the metal bridging. The typical resistance between the emitter and base contacts is 1 Ω. The curve-tracer photograph of Fig. 8 illustrates the chain of events required to short-circuit a Zener diode. Diode voltage is swept at a 120-Hz rate. Avalanche breakdown occurs at 6.3 V. Beyond this voltage, to 18 V, the diode behaves as a 170-Ω resistor, which is the resistance of the emitter and the 200-Ω per square base region between the contacts. At 18 V the instantaneous power dissipation exceeds 1.2 W. If the voltage is increased, the diode will switch into an oscillatory, thermal runaway condition. This state lasts less than a second, after which the Zener is destroyed and a 1-Ω resistor results. It is apparent from Fig. 8 that a necessary condition for shorting Zeners is that sufficient voltage and current has to be provided to exceed the "knee" of the curve at 18 V and 70 mA.

Using an automated tester, a current pulse train can be applied to the device [10], and as the avalanched junction is progressively degraded, the resistance can alternately be monitored. When a predetermined resistance is reached the pulse train is terminated.

The shorting method selected for the precision operational amplifier described above was to experimentally arrive at a set of conditions which will short the Zeners without fail considering all possible manufacturing variations. Application for 80 ms of a 25-V power supply, current-limited at 300 mA consistently shorted the Zener diodes.

Acknowledgment

The author wishes to thank J. Biran, J. Lundstrom, and S. Saylor for their assistance in testing the device and B. Dunaway for the chip layout.

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