Design of Oscillator and Charge Pump for the Startup of Ultra-Low-Voltage Energy Harvesters

Franciele Nornberg, *Macnica DHW* , Marcio B. Machado, *Member, IEEE,* Rafael L. Radin, *Member, IEEE,* Carlos Galup-Montoro, *Senior Member, IEEE,* Marcio C. Schneider, *Senior Member, IEEE.*
francielefnornberg@gmail.com, marciomachado@pelotas.ifsul.edu.br, rafaelradin@gmail.com, carlosgalup@gmail.com, marcio.cherem.schneider@gmail.com

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***Abstract*—This paper presents a design procedure for the minimization of the startup voltage of energy-harvesting boost converters. The analysis of both an LC oscillator and a charge pump under ultra-low-voltage operation, based on the physics-based MOSFET and diode models, is performed. Considering the interaction between these two blocks, a routine that minimizes the startup voltage of boost converters is proposed. The technique provides the oscillator characteristics, number of stages and sizing of the charge-pump devices. The methodology, applied to a cold startup in a 180 nm CMOS technology, provides a fully integrated design with a minimum input voltage of only 53 mV, for an output of 500 mV at 100 nA of current consumption.**

***Index Terms*—LC-oscillator, startup, boost converter, fully-integrated, ultra-low voltage, ultra-low power, energy harvesting.**

I. Introduction

THERMAL energy harvesting is a suitable option to supply emerging circuits in biomedical and wireless body area network (WBAN) applications. Due to the low voltage level provided by thermoelectric generators (TEGs), many papers have addressed the boost conversion from voltages under 100 mV in the recent years.

To comply with the requirements of very low startup voltages and elevated power conversion efficiency, a topology such as that shown in Fig. 1 (a), comprised of a cold starter (CS) and a second, more efficient main converter, has been adopted by several authors [1], [2], [3], [4]. In a complete energy harvesting interface, the CS is employed as an auxiliary converter designed to provide a temporary V_{DD}, much higher than the input voltage, which powers the auxiliary circuits of the main converter, allowing it to start-up. The CS is commonly implemented with an ultra-low-voltage (ULV) oscillator whose outputs are connected to a charge pump [1], [3], [4], providing a temporary DC voltage. Although charge pumps can provide reasonable conversion efficiency at higher input voltages [5], for the voltage levels obtained when harvesting thermal energy from the human body, the operation of charge pumps is inefficient, restraining its use as a main converter of an energy harvesting interface.

An equivalent electric circuit of a CS is shown in Fig. 1 (b). The CS design targets a reduction in the converter startup voltage and the maximization of the temporary V_{DD} under the load imposed by the auxiliary circuits of the main converter. The main design challenge of the CS arises from the mutual dependence between the amplitude of the ULV oscillator (V_A) and the charge pump input resistance (R_{IN}). On the one hand, the charge-pump input loads the output nodes of the oscillator, thus causing the oscillation amplitude to decrease. On the other hand, the charge pump input resistance is a function of the amplitude. Although the use of this type of CS is a common solution in the technical literature, no optimization procedure is reported for this circuit to minimize the input voltage for the converter startup. Instead, the CS is generally designed by simulation through a trial-and-error process.

In this brief, we present a computer-aided routine for the optimization of the CS, based on a classical LC oscillator, targeting the minimization of the converter startup voltage. Using the DC equations of the MOS transistor model [6] for the ULV oscillator and a physics-based model [7] for the charge pump under ULV operation, the optimization procedure provides the number of charge-pump stages and the sizing of the charge-pump diodes. To validate the proposed design methodology, a CS was designed in a 180 nm process and compared with state-of-the-art fully integrated start-up designs.

II. Basic Blocks

To develop the CS design methodology, firstly, we analyzed some topologies for the two blocks that compose the CS, namely the ultra-low-voltage LC oscillator and the charge pump/voltage multiplier.

A. The Ultra-Low-Voltage LC Oscillator

Besides oscillating at very low input voltages, LC oscillators also can increase the voltage levels to values higher than the DC voltage supplied by the harvesters, making them a common solution in cold starters. This is an important advantage over the ULV CMOS ring oscillators, which occupy a much smaller area, but provide oscillating amplitudes that are

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Franciele Nornberg is with the Macnica DHW, Florianopolis, Brazil
Marcio B. Machado is with Federal Institute of Sao Paulo, Campinas, SP Brazil.
Rafael L. Radin, Carlos Galup-Montoro and Marcio C. Schneider are with Electrical and Electronic Engineering Department of Federal University of Santa Catarina, Florianopolis, Brazil.

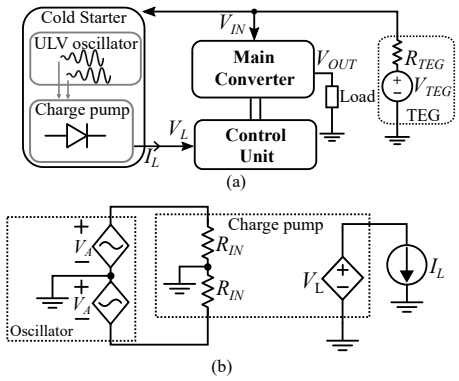

Fig. 1. (a) Hybrid ULV boost topology composed of the cold starter and the main converter; (b) A simplified equivalent circuit of the cold starter.

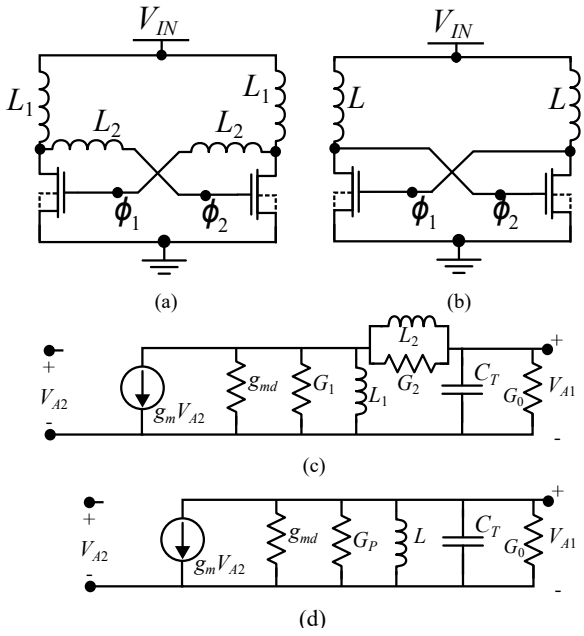

Fig. 2. Schematic of the (a) ESRO and (b) IRO, and small-signal equivalent circuit of a single stage of the (c) ESRO and (d) IRO.

smaller than the supply voltage. Furthermore, the performance of LC oscillators is closely related to the quality factor of inductors; improvements in more advanced technologies can further enhance the performance of LC oscillators, decreasing the minimum DC input voltage to generate oscillations.

To choose the most advantageous oscillator topology, we perform a comparison between two common LC oscillators, namely the enhanced-swing ring oscillator (ESRO) and the inductive ring oscillator (IRO), depicted in Fig. 2. The choice of oscillator should target the minimization of the input voltage required to achieve oscillations under the charge-pump load and avoid excessive silicon consumption.

Using the simplified small-signal circuit of the IRO shown in Fig. 2(d), the derivation presented in [8], and assuming that the transistors operate in weak inversion [6] with a slope factor $n \approx 1$, the minimum V_{IN} for achieving oscillations with the IRO can be approximated by

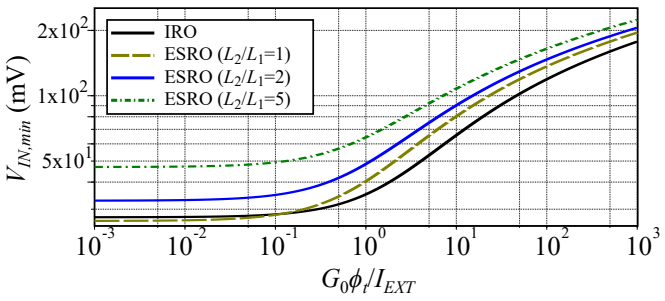

Fig. 3. Minimum V_{IN} for achieving oscillations using the ESRO (different inductors ratio) and the IRO. $Q = 8.8$, $L = L_2 = 18.8$ nH, ϕ_t=25.7 mV, I_{ext}=106 μA, and C_T=21 pF.

$$\frac{V_{IN}}{\phi_t} = \frac{V_{DS}}{\phi_t} \approx \ln\left(2 + \frac{G_{EQ}}{g_{md}}\right) \approx \ln\left(2 + \frac{\phi_t G_{EQ}}{I_{ext}}\right), \quad (1)$$

where $g_{md} = \frac{\partial I_D}{\partial V_D}$ is the transistor output conductance, ϕ_t is the thermal voltage, and I_{ext} is the extrapolated current in saturation for V_G=V_S=0 V, which is dependent on technological parameters and the transistor aspect ratio [6]. In (2), G_{EQ} is given by

$$G_{EQ} = \frac{\sqrt{\frac{C_T}{L}}}{Q} + G_0, \quad (2)$$

where C_T is the total capacitance seen in transistor gate, Q is the inductor quality factor, and G_0 is the load conductance, which represents the input of the charge pump in the CS arrangement of Fig. 1(b). In Fig. 2(c), g_m is the gate transconductance, and G_P is the inductor parallel conductance.

Using the small signal of Fig. 2(c), we apply a similar method for the ESRO, yielding

$$\frac{V_{IN}}{\phi_t} \approx \ln\left(1 + \frac{1}{1 + \frac{L_2}{L_1}} + \frac{\phi_t G_{EQ,ESRO}}{I_{ext}}\right), \quad (3)$$

$$G_{EQ,ESRO} = \frac{\sqrt{\frac{C_T}{L_2}}}{Q}\sqrt{\frac{L_2}{L_1}\left(1 + \frac{L_2}{L_1}\right)} + G_0\left(1 + \frac{L_2}{L_1}\right). \quad (4)$$

As (3) and (4) suggest, the adoption of the ESRO with high L_2/L_1 ratio in off-chip designs, as well as wide transistors (high I_{ext}), can provide ultra-low startup voltages [3] due to the high inductance values and high quality factor provided by off-the-shelf inductors. However, in a fully-integrated design, both the maximum inductance value and Q are limiting factors that compromise the low-voltage startup. Figure 3 shows the minimum value of V_{IN} for achieving oscillations, calculated from expressions (1) to (4). Practical values for L and Q available in the technology are used, whereas the definition of C_T and I_{ext} was based on the extracted parameters of the implemented oscillator transistor, as explained in Section III. As can be seen in Fig. 3, for the 180 nm technology, due to

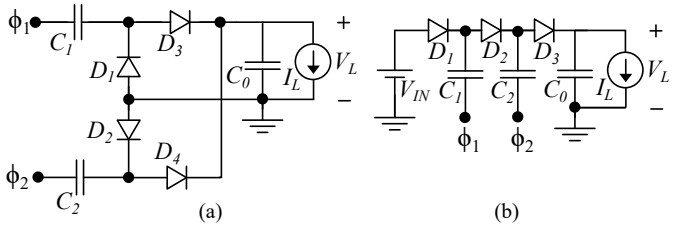

Fig. 4. (a) A single stage of the symmetrical voltage multiplier and (b) a three-stage DCP.

the limited values of inductance and Q, the IRO can provide better results than the ESRO, especially under load, with the advantage of using less area. Therefore, in this research we used the IRO for the ULV oscillator in the fully-integrated CS.

B. The ULV Charge Pump

In this paper, two charge pump topologies were considered, the Dickson charge pump (DCP) and the full-wave voltage multiplier. In the next section, both charge-pumps are used in the routine to verify which topology provides the lower startup voltage.

The input of the charge pump loads the output of the oscillator, impairing the oscillation condition as well as the oscillation amplitude. Therefore, an analytical model of the charge pump under ULV operation is required to determine its input resistance as well as the DC output voltage.

In [9], the basic voltage multiplier is analyzed using the Shockley equation for the diodes, given by

$$I_D = I_{sat}\left[e^{\left(\frac{V_D}{n\phi_t}\right)} - 1\right]. \tag{5}$$

where I_{sat} is the diode reverse saturation current and V_D is the diode across voltage. Using a similar method applied in [9] for the half-wave voltage multiplier, we analyse the full-wave voltage multiplier shown in Fig. 4(a), which is a more adequate topology for operation from two complementary signals provided by the oscillator. Since the average current through the diodes is equal to the $I_L/2$, the output voltage and the input resistance of the full-wave multiplier are given, respectively, by

$$V_L = 2Nn\phi_t \ln\left[\frac{I_0\left(\frac{V_A}{n\phi_t}\right)}{1+\frac{I_L}{2I_{sat}}}\right], \tag{6}$$

and

$$R_{IN} = \frac{V_A}{2N(2I_{sat}+I_L)}\frac{I_0\left(\frac{V_A}{n\phi_t}\right)}{I_1\left(\frac{V_A}{n\phi_t}\right)}. \tag{7}$$

Here, I_0 and I_1 are the modified Bessel functions of the first kind of order zero and one, respectively and N is the number of charge pump stages.

Also using the Shockley equation, the output voltage and the input resistance of an N-stage DCP shown in Fig. 4 (b) are given by [7]

$$V_L = V_{IN} + 2n\phi_t \ln\left[\frac{I_0\left(\frac{V_A}{n\phi_t}\right)}{1+\frac{I_L}{I_{sat}}}\right] + (N-2)n\phi_t \ln\left[\frac{I_0\left(\frac{2V_A}{n\phi_t}\right)}{1+\frac{I_L}{I_{sat}}}\right], \tag{8}$$

$$R_{IN} = \frac{V_A}{2(I_{sat}+I_L)\left[\frac{I_1\left(\frac{V_A}{n\phi_t}\right)}{I_0\left(\frac{V_A}{n\phi_t}\right)} + (N-2)\frac{I_1\left(\frac{2V_A}{n\phi_t}\right)}{I_0\left(\frac{2V_A}{n\phi_t}\right)}\right]}. \tag{9}$$

These expressions of V_L and R_{IN} are used in the algorithms of Section III to find the N and I_{sat} pair which minimizes the input voltage to achieve the output specification, thus minimizing the startup voltage of the energy harvesting converter.

III. The Design Methodology

The design of a step-up converter composed of a ULV oscillator and a charge pump has many degrees of freedom due to several parameters involving the design of inductors, oscillator transistors, number of stages and size of devices of the charge pump. Also, the oscillator and the charge pump cannot be designed independently since the oscillator amplitude depends on the converter input resistance, which, in turn, depends on the oscillator amplitude. To comply with this mutual dependence, we developed an algorithm that determines the converter time response and generates a plot of the converter output voltage as a function of the charge pump parameters: diode saturation current and the number of stages.

A. Computer-Aided Routine

From the specification of the charge pump, voltage and current at the output (V_L and I_L), and the voltage at the input, provided by the TEG, one can define the initial circuit values to begin the design procedure. Following the flowchart shown in Fig. 5(a), the values of the inductor and transistor in Fig. 5(b) can be defined by simulation, in order to find the initial circuit values that provide the lowest input voltage for starting up the oscillator. Also, an arbitrary value of the charge-pump input resistance (R_{IN}) can be used in the simulation to start the procedure.

Once the oscillator devices have been defined, the inductor and transistor's main physical parameters are extracted by the electrical simulator and used by the routine. The algorithm then solves the time domain analysis, which calculates the oscillation frequency and amplitude.

Using the i-v relationship of capacitors, inductors, resistors, and transistors [6], we calculate the response of the equivalent circuit in Fig. 5(b) applying the KCL to the four circuit nodes. For this, we set an initial value of R_{IN} (G_0^{-1}) and start the procedure by calculating the oscillation amplitude V_A for a given N and I_{sat}. From the V_A obtained, an updated value of R_{IN} is calculated, generating a new value for the

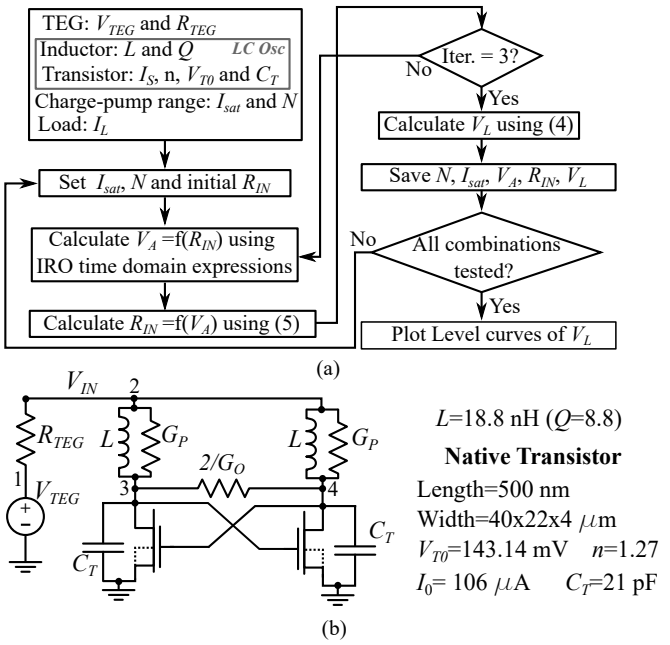

Fig. 5. (a) Flowchart of the programming routine developed to find the values of I_{sat} and N and (b) schematic used in the optimization routine.

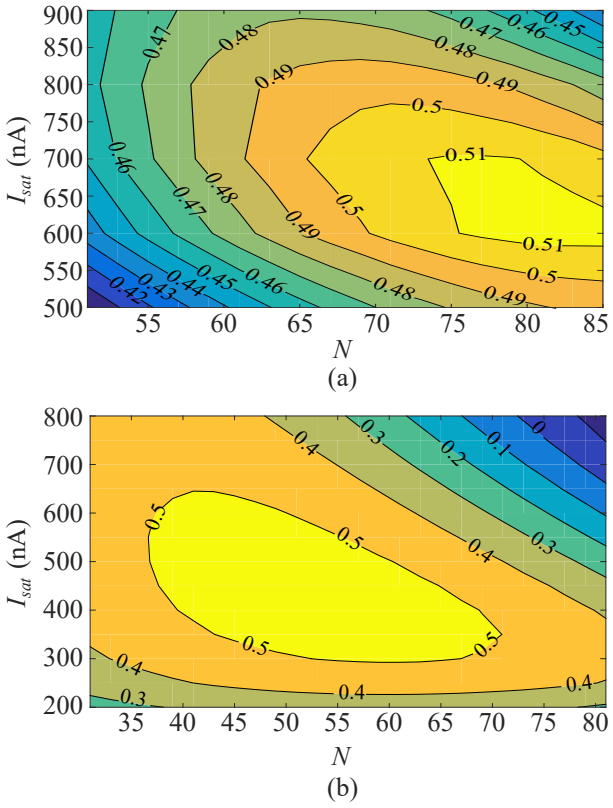

Fig. 6. Level curves of the converter output voltage V_L for (a) V_{TEG}= 49 mV, using the voltage multiplier and (b) V_{TEG}=46.5 mV, using the Dickson charge pump.

oscillator amplitude. This procedure is repeated until R_{IN} and V_A converge within specified limits, which, in our case, was observed after three interactions. After convergence, V_L can be calculated for the given I_{sat} and N, and the system restarts the procedure for a different I_{sat} and N pair.

B. Design and Implementation

The CS specifications were determined for the boost converter described in [10]. For this converter, the CS should provide a temporary V_{DD} of 500 mV for a load current of 100 nA required to properly supply both the auxiliary circuits and the switching losses of the boost converter.

Following the flowchart of Fig. 5(a), from the oscillator specifications shown in Fig. 5(b), we found a set of charge-pump parameters that allowed us to achieve the minimum startup voltage at the specified load (V_L = 500 mV and I_L = 100 nA). The resulting output characteristics of the Dickson charge pump and the voltage multiplier, as a function of N and I_{sat}, can be seen in the level curves shown in Fig. 6. The desired output specifications were achieved for V_{TEG} equal to 46.5 mV for the DCP and 49 mV for the voltage multiplier; therefore, the use of the DCP favored the low-voltage startup, and a DCP with 45 stages and diodes with I_{sat} = 340 nA was chosen for this design. The diodes were implemented using zero-VT devices with W/L =6 μm/0.5 μm.

IV. Results and Discussion

To validate the methodology, the CS was implemented in EDA tools using the TSMC 180 nm process design kit. The circuit layout is shown in Fig. 7, with an active area of 1.47 mm^2.

For the simulations, as shown in Fig. 5(b), the TEG was emulated with a voltage source (V_{TEG}) in series with a 5 Ω resistance (R_{TEG}). The schematic simulations closely agree with the method, and the circuit delivers the output specs for V_{TEG}=48 mV. This value is increased in post-layout simulations due to the introduction of parasitics. The converter starts-up for V_{IN}= 47.5 mV (V_{TEG} = 52 mV) and the load condition (V_L=500 mV and I_L=100 nA) is reached for V_{IN}= 53 mV (V_{TEG} = 58 mV) using the typical process parameters for the simulations (TT). Fig. 8(a) shows the oscillator phases, V_{TEG} and V_{IN} during the startup transient, and Fig 8(b) shows the complete build-up of the DCP output voltage, reaching the steady-state value of V_L=528 mV. The oscillator frequency

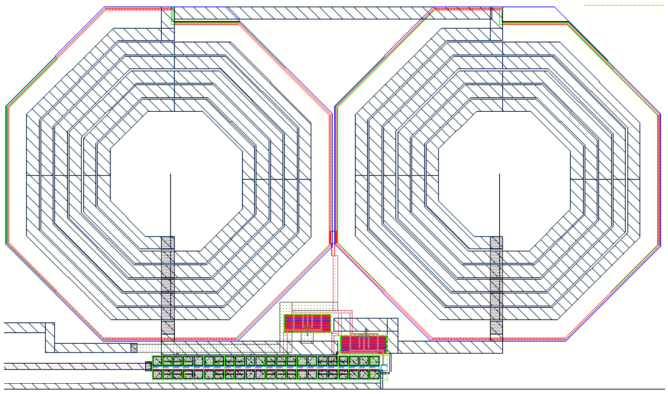

Fig. 7. The layout of the active area of the optimized CS, including the IRO and a 45-stage DCP.

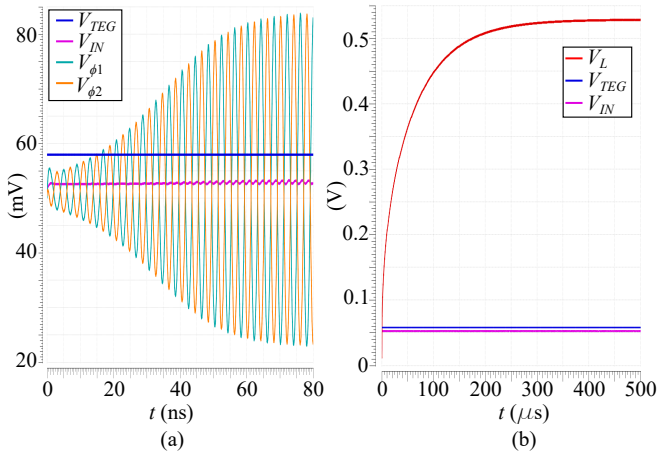

Fig. 8. Post-layout simulation results of (a) the initial transient of the oscillator output voltages, V_{TEG} and V_{IN}, and (b) the output voltage V_L buildup, V_{TEG} and V_{IN}. V_{TEG}=58 mV

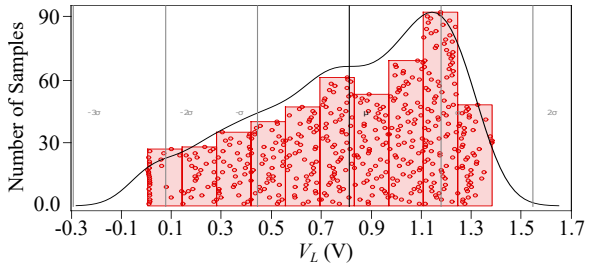

Fig. 9. Monte Carlo simulation results of V_L for V_{IN}=53 mV.

obtained was 240 MHz.

To evaluate the performance of the CS regarding mismatch and process variations, Fig. 9 shows the results of a Monte Carlo simulation, where V_{IN} is kept fixed at 53 mV and V_L is measured in steady state. For this condition, simulating 500 samples, the mean value of V_L is 809.6 mV with a standard deviation of 367.32 mV. As can be seen in Fig. 9, a few samples could not reach the output specification for V_{IN} = 53 mV. For these samples, an increment of a few millivolts at the input would be necessary. In any case, a voltage limiter should be included at the output.

Table I shows the comparison with state-of-the-art fully-integrated CS. As can be seen, the use of the proposed methodology provides further reduction in the startup voltage of energy harvesting converters.

TABLE I
BENCHMARK WITH THE RECENT FULLY-INTEGRATED STARTUP CONVERTERS.

Ref.	$V_{IN,min}$	Process	Startup solution
[1]	100 mV	65 nm	IRO+voltage multiplier
[4]	60 mV	65 nm	IRO+CP
[11]	60 mV	180 nm	Modified RO+CP
[12]	57 mV	180 nm	Stacked RO+CP
[13]	70 mV	130 nm	Schmitt-trigger+CP
[14]	60 mV*	180 nm	RO+CP
This Work	53 mV*	180 nm	IRO+DCP

* Post-layout results.

V. CONCLUSION

A design procedure that allows a reduction in the startup voltage of energy harvesting converters was proposed. The results obtained from the analysis of both the ULV oscillator and charge pump based on the physics of the transistor and diodes were used to develop a design methodology, which takes into account the interaction between the two blocks. The results showed that the proper association between the designs of the oscillator and charge pump provided by the proposed optimization method opens space for a further reduction in the startup voltage of boost converters, enabling the startup of the converter at lower thermal gradients.

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