LOW POWER DESIGN TECHNICS for RF in FDSOI

Sylvain BOURDEL, IMEP-LAHC

Context

G-INP & IMEP-LAHC

Minatec

CEA – CNRS – G-INP - UGA

GRENOBLE

5th innovative city in the World (6.23 Patents / 10 000 citizens)

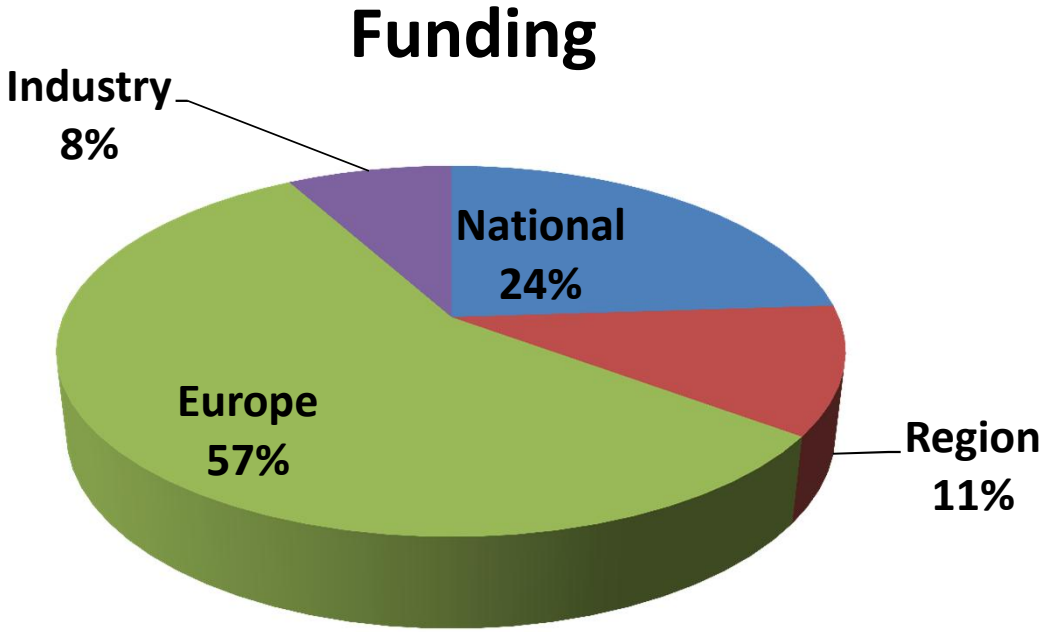
Context

- ***Academic – National***

- ***Academic – International***

- ***Compagnies***

Context



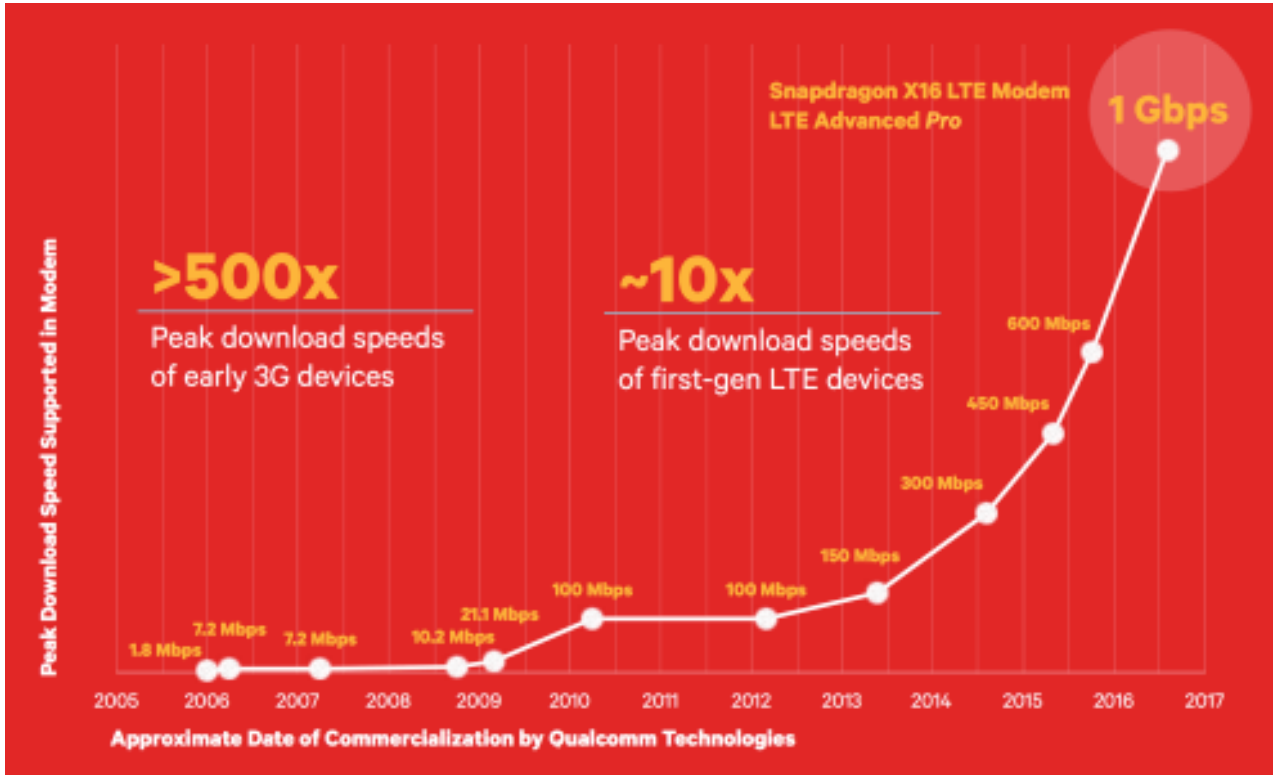
7 full time researchers
350 KE/Year
- **Half of the PHD Salaries**
- **Investissement (Equipement)**

Objectives :

- Make an overview of the different possibilities to reduce power consumption in RF systems

- Focus on technics suited to FDSOI

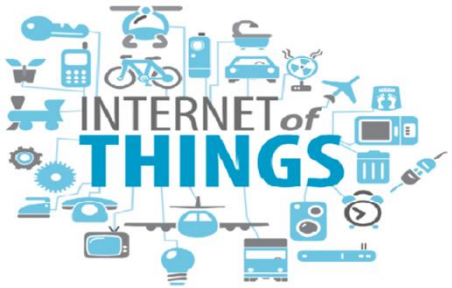
Introduction : Why

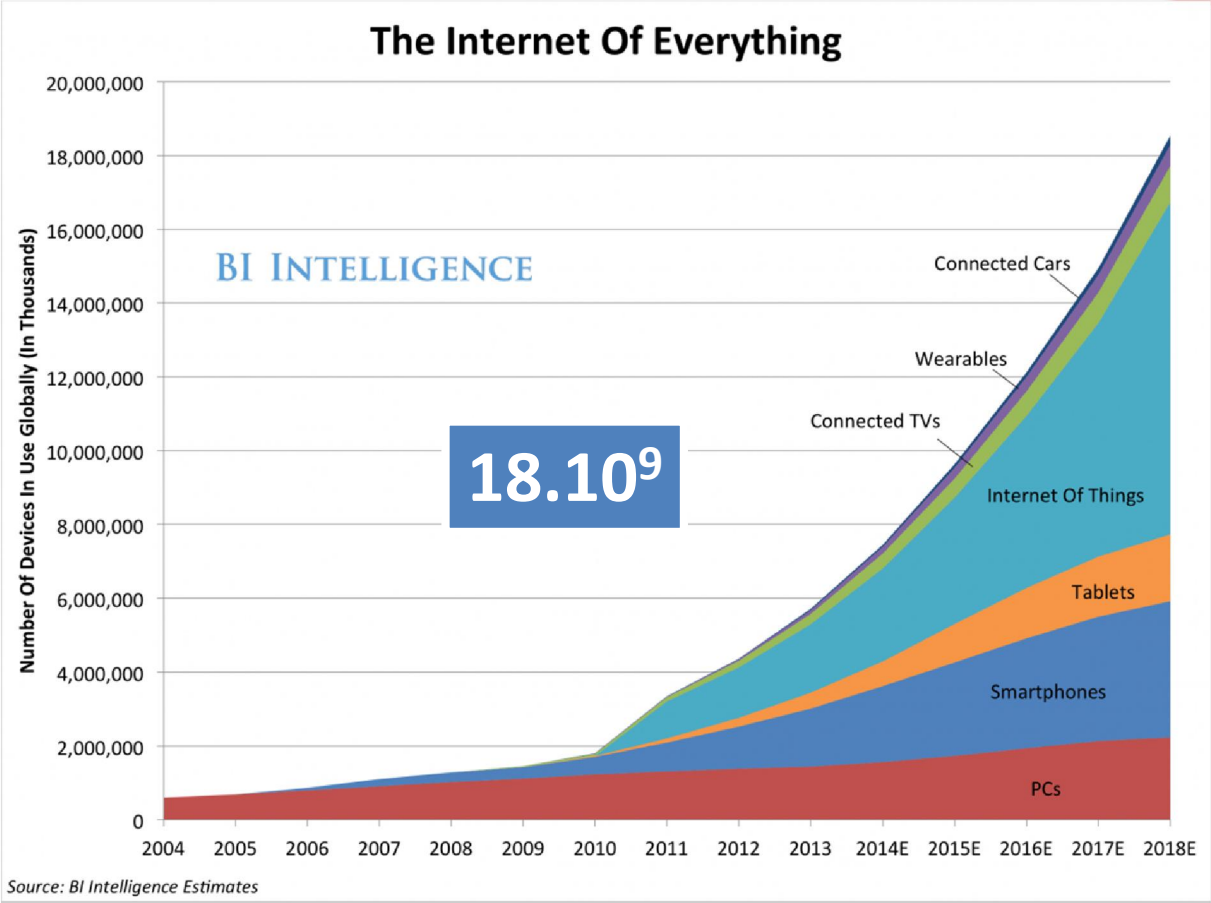


!!!! 10mW@10Mbps => 1W@1Gbps !!!!

Needs for high efficiency (J/bit)

Introduction : Why

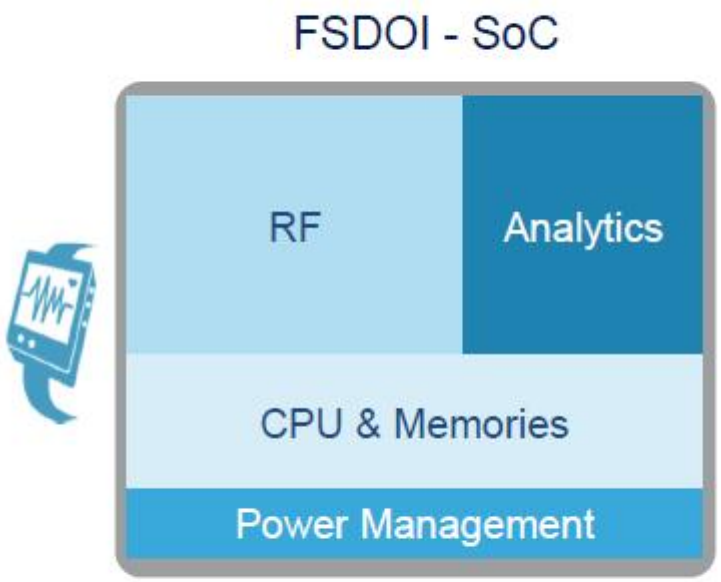




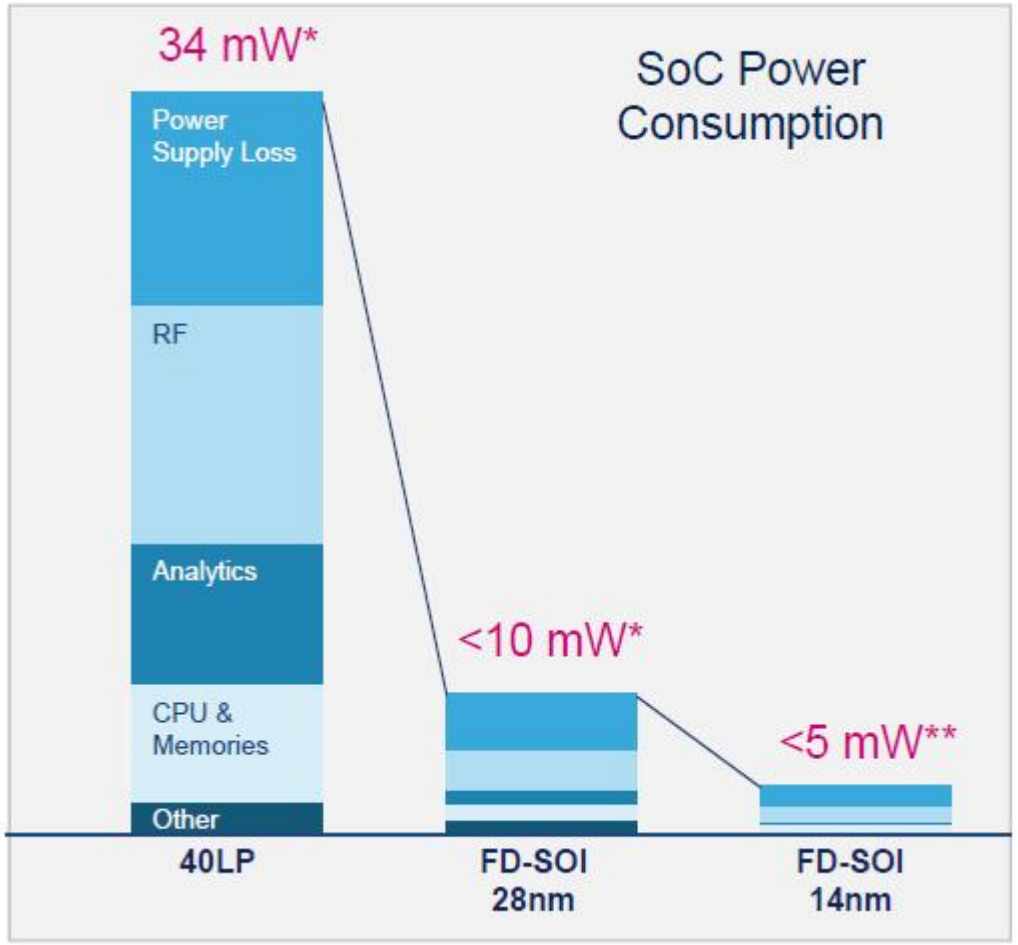
Who will change the cells ?

??? What will we do with worn cells ???

Introduction : Why



RF IP's consume 1/3 to 1/2 of the entire power budget



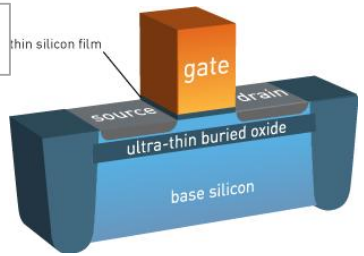
[« RFSOI and FDSOI enabling smarter and IoT applications » Kirk Ouellette, *Digital Products Group STMicroelectronics*]

Introduction : How

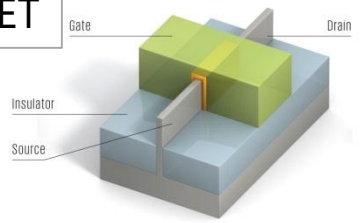
Several Levels

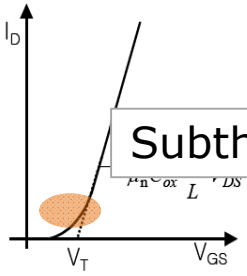
- Technological Level
- Electrical Level
- System Level
- Protocol Level

FDSOI



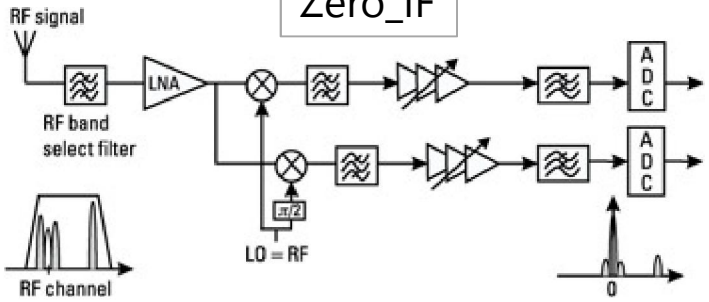
FinFET

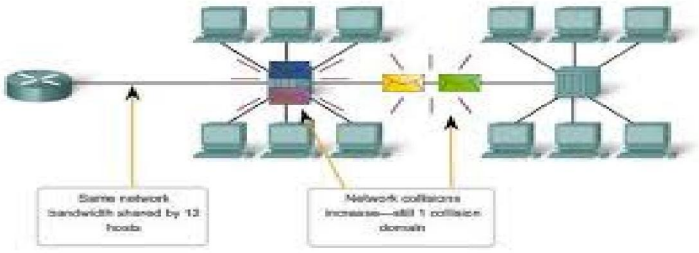




Subthreshold

Zero_IF





SUMMARY

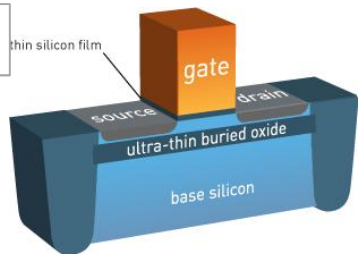
- Introduction
- Technological Level
  - Digital Functions
  - Analog Functions
- Electrical Level (Bloc Design)
  - Subthreshold technics
  - LNA design
- System Level
  - Direct Conversion
  - Duty Cycling
- Concluding remarks

Technolgies : FinFET & FDSOI for Digital

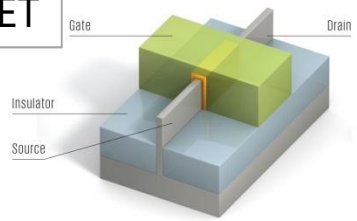
New technology properties:

- Low leakages :
  ⇒ Static Power Reduction
- Threshold variability is better controlled
  ⇒ Static and dynamic power reduction

FDSOI

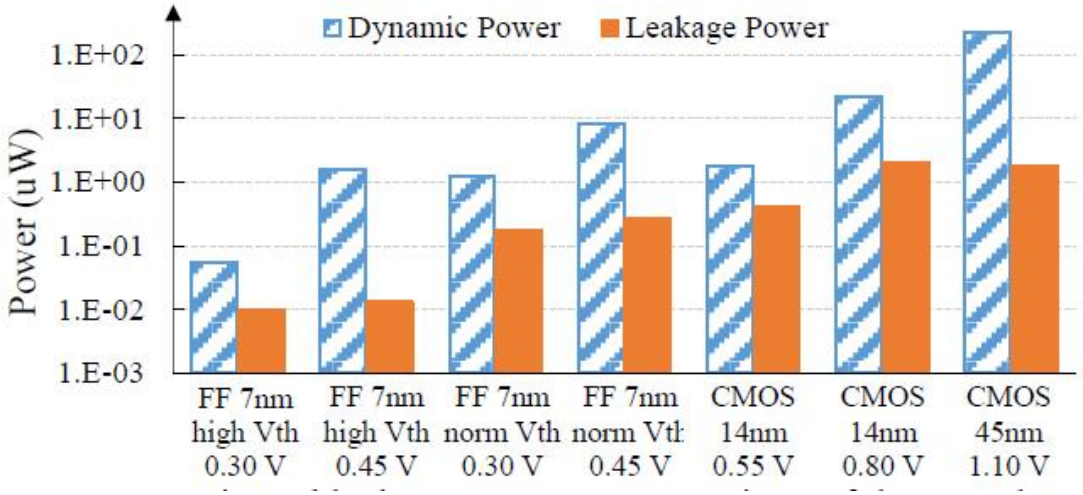


FinFET



Power of Digital Circuits

$$P_{digital} = P_{stat} + P_{dyn} = I_{leak}.V_{dd} + \alpha.C_L.f_{clk}.V_{dd}^2$$



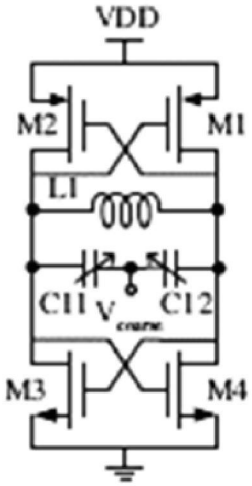
Vdd => Pd

Technolgies : FDSOI for Analog

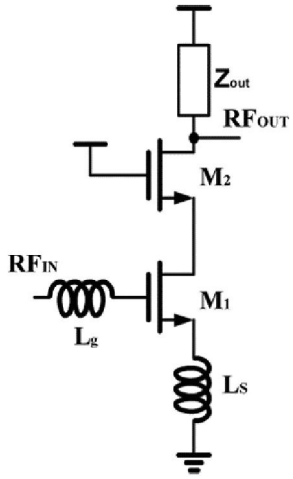
Design comparison:

- LNA & VCO
- BTLE (2,4GHz)

[B. Martineau, « UTBB-FDSOI 28nm : RF Ultra Low Power technology for IoT » International Forum on FDSOI IC Design]



FoM	CMOS 65nm	UTBB-FDSOI 28nm
Frequency (GHz)	2.4	2.4
PNoise @ 1MHz (dBc/Hz)	-119	-126
P_{DC} (mW)	1	1



FoM	CMOS 65nm	UTBB-FDSOI 28nm
NFmin (dB)	1	1
Gain (dB)	23	24
S11 (dB)	-10	-10
P_{DC} (mW)	0.4@1.2V	0.1@0.55V*
IIP3 (dBm)	-30	-26
ICP1 (dBm)	-39	-36

*Using body bias = 350mV

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Electrical Level (Bloc Design) :
Introduction

- **Current reuse technics**
- **Passive components**
- **Region of operation**

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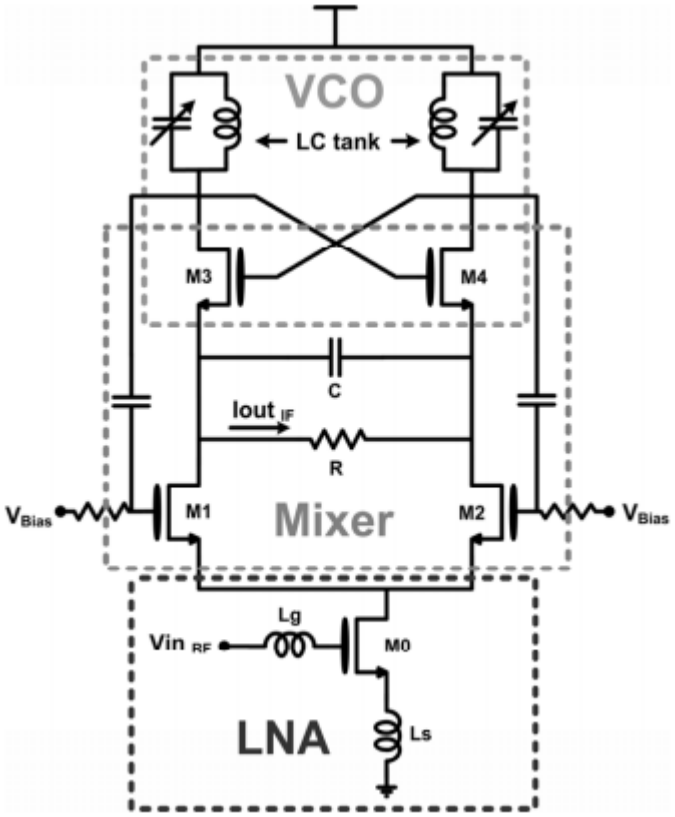

[Antonio Liscidini , Andrea Mazzant et *al.*, "A 5.4mW GPS CMOS Quadrature Front-End Based on a Single-Stage LNA-Mixer-VCO," IEEE ISSCC 2006.]

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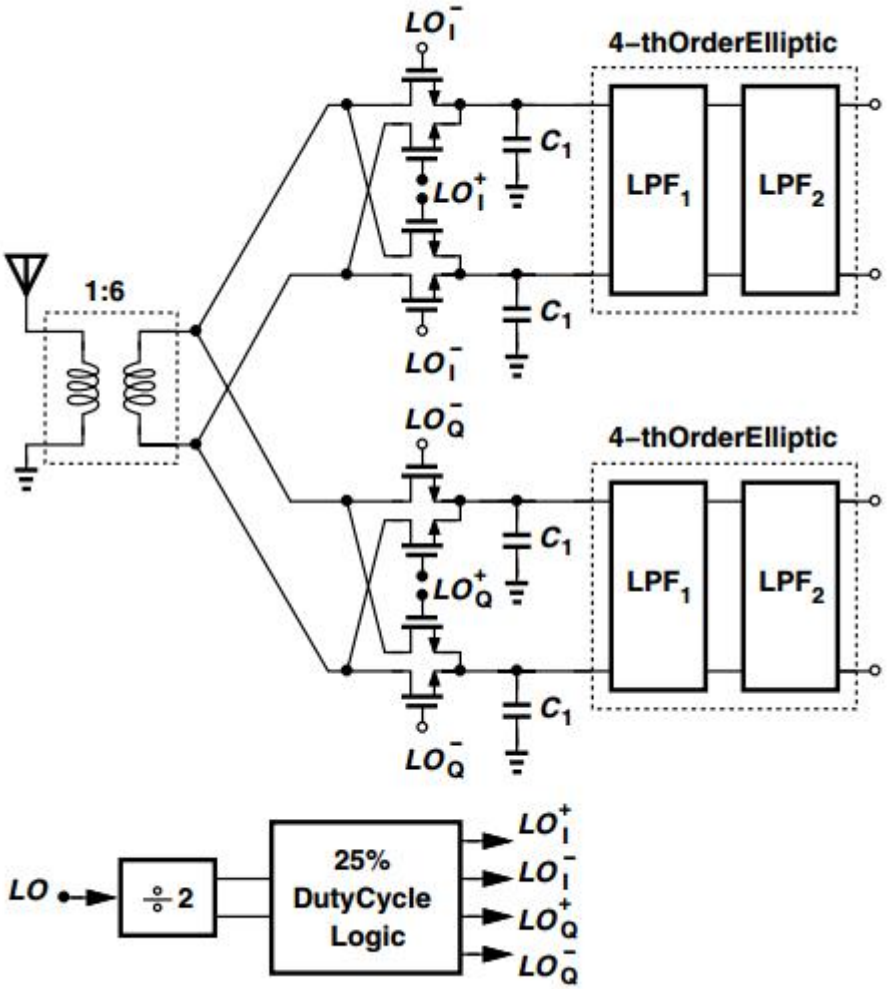
Electrical Level (Bloc Design) :

Introduction

- **Current reuse technics**
- **Passive components**
- **Region of operation**



[A. Homayoun, B. Razavi; "A 5-GHz 11.6-mW CMOS receiver for IEEE 802.11a applications", IEEE CICC 2013]

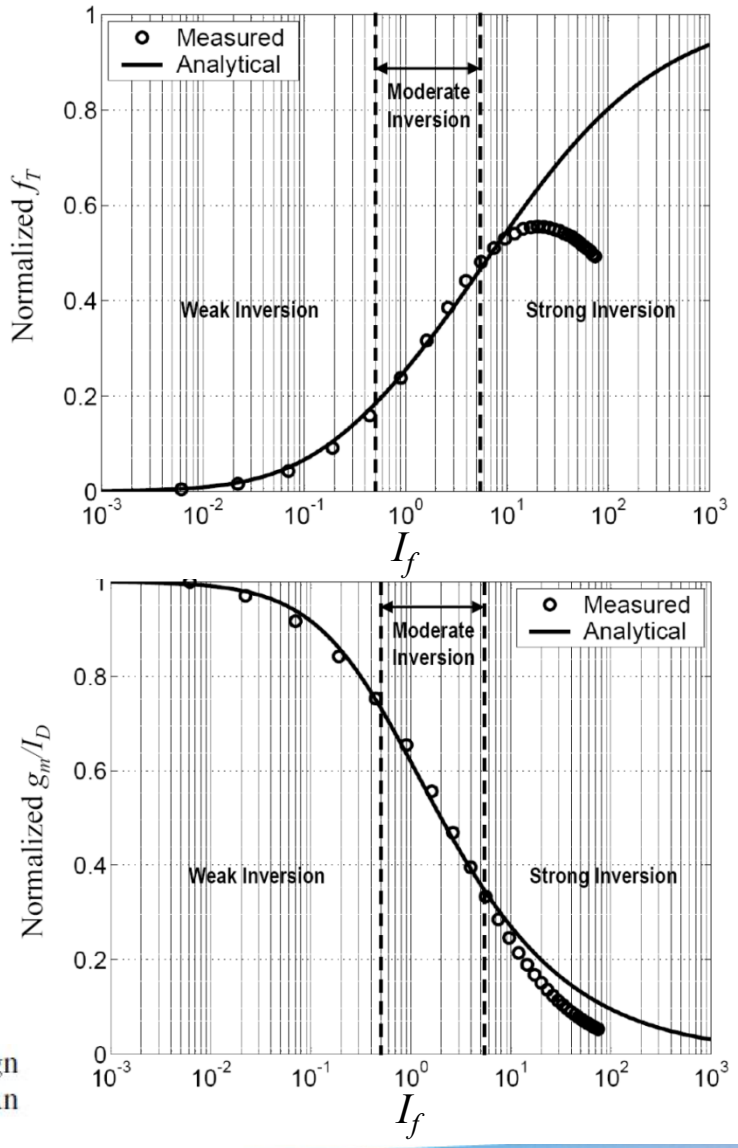
Region of operation : FOM

Inversion factor

[Araujo, Schneider, Galup – JSSC 1998]:

- I_f represents the region of operation
- Several FOM depends on I_f
  - f_T;
  - g_m/I_D
- Traditional RFIC are designed in strong inversion

$$I_f = \frac{I_D}{I_{spec}} = \frac{I_D}{\frac{W}{L} n \mu_0 C_{ox} \frac{U_T^2}{2}}$$



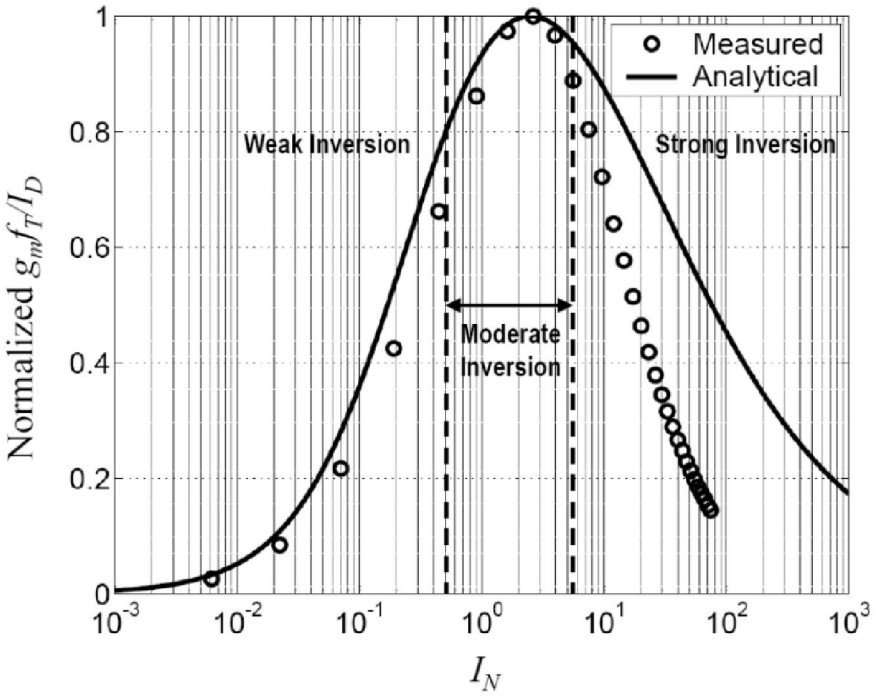
A. Shameli et P. Heydari, « Ultra-Low Power RFIC Design Using Moderately Inverted MOSFETs: An Analytical/Experimental Study », *RFCI*, 2004.

Region of operation : FOM

Gain-Bandwith-Product :

$$\frac{g_m f_T}{I_D}$$

- Allows to take into account f_T
- For a fixed bias current
  $\Rightarrow$ Best Gain-Bandwidth-Product (GBW)
- Maximum in the moderate inversion region



A. Shameli et P. Heydari, « Ultra-Low Power RFIC Design Using Moderately Inverted MOSFETs: An Analytical/Experimental Study », *RFCI*, 2004.

Region of operation : FOM

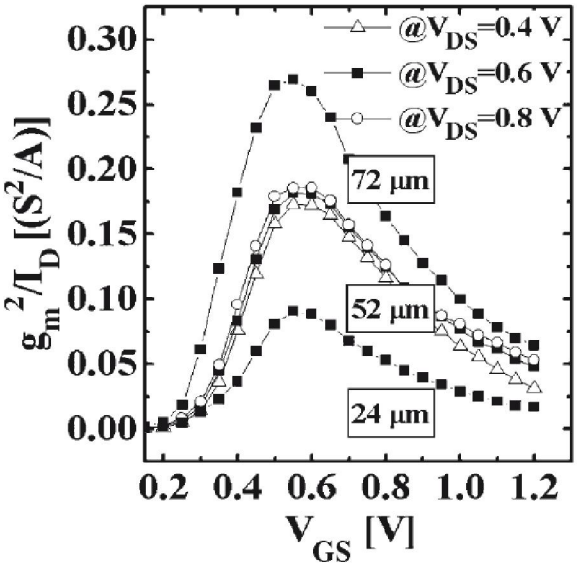
Dedicated FoM :

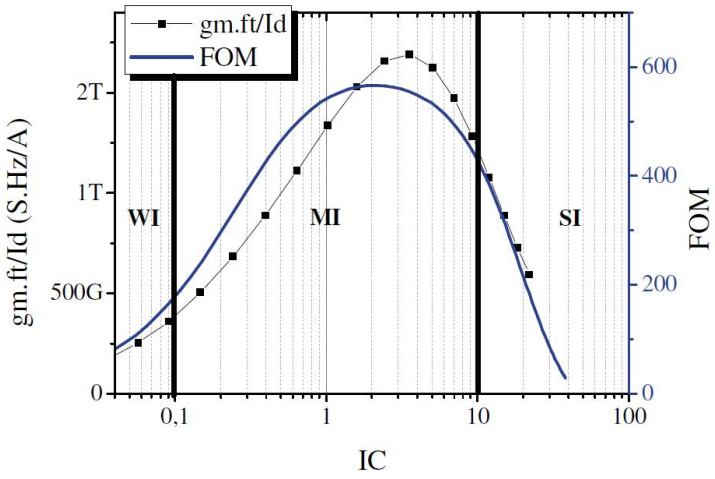
$$\mathrm{FoM_{LNA}} = \frac{G}{(F-1)\cdot P} \propto \frac{g_m^2}{\left(\frac{I_D}{g_m^2}\right)\cdot I_D} \propto \left(\frac{g_m^2}{I_D}\right)^2 .$$

I. Song et B.-G. Park, « A Simple Figure of Merit of RF MOSFET for Low-Noise Amplifier Design », *Electron Device Lett. IEEE*, vol. 29(12), 2008.

$$FOM = \frac{Av_{abs}.freq_{GHz}}{(F_{\min}-1)_{abs}.(I_D.Vdd)_{mW}}$$

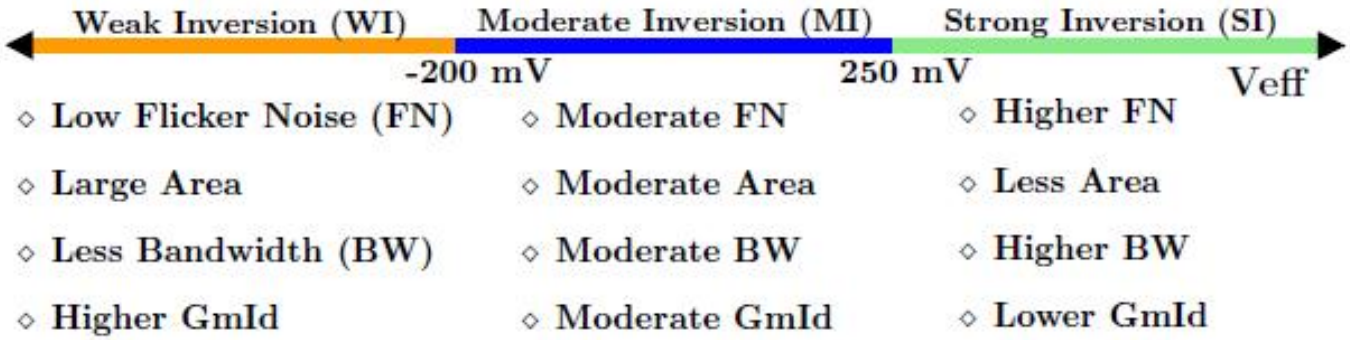
Fadhuile, F., Taris, T., Deval, Y., De Matos M., Belot D., Enz C.; "Design methodology for low power RF LNA based on the figure of merit and the inversion coefficient" AICSP, Vol 87, pp 275-287, 2016





- Maximum in moderate inversion
- Do not take into account NL

Region of operation : FOM



	Tech (nm)	GV (dB)	NF (dB)	IIP3 (dBm)	Power (mW)	Supply (V)	Area (mm^2)
[2]	65	8.7	3.74	n/a	0.315	0.7	0.442
[3]	90	12.6	5.5-6.5	-6∼-9	0.75	0.5	0.23
[4]	90	9.7	4.36	-4	0.684	1.2	0.9126

[2] Vinaya. M M, Paily. R.P, and Mahanta. A, "A Low-Power Subthreshold LNA for Mobile Applications", IEEE VLSI Design and Test Symposium, jun 2015.
[3] M. Parvizi, K. Allidina, and M. El-Gamal, "A sub-mw, ultra-low-voltage, wideband low-noise amplifier design technique," IEEE Trans.Very Large Scale Integr. (VLSI) Syst., vol. 23, no. 6, pp. 1111–1122, Jun. 2015.
[4] R. Fiorelli, F. Silveira, and E. Peralias, "MOST moderate-weak-inversion region as the optimum design zone for CMOS 2.4-GHz CS-LNAs," Microwave Theory and Techniques, IEEE Transactions on, vol. 62, no. 3, pp. 556–566, March 2014.

? What about gm/Id design methods in RF? ?

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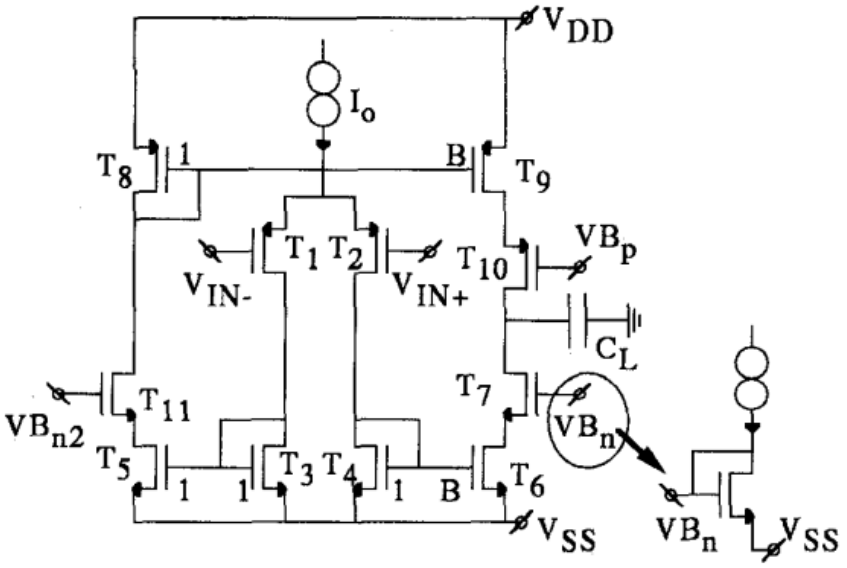
Region of operation : g_m/I_D based Methodology

General Principle

[Silveira, Flandre, Jespers – JSSC 1996]

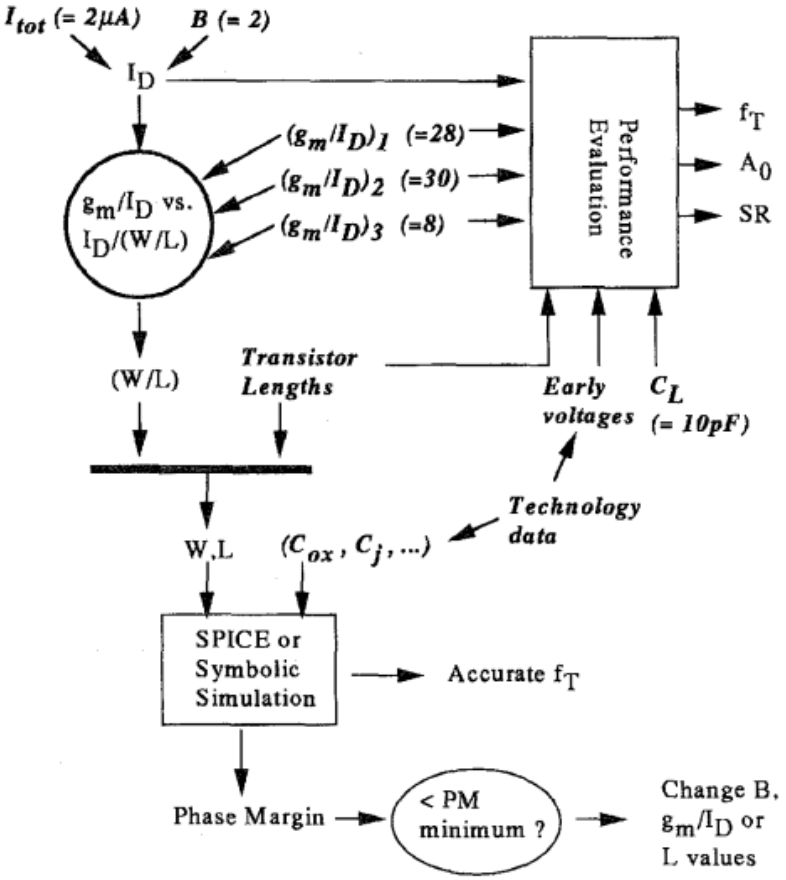
- For a given structure



Region of operation : g_m/I_D based Methodology

The History …

[Silveira, Flandre, Jespers – JSSC 1996]



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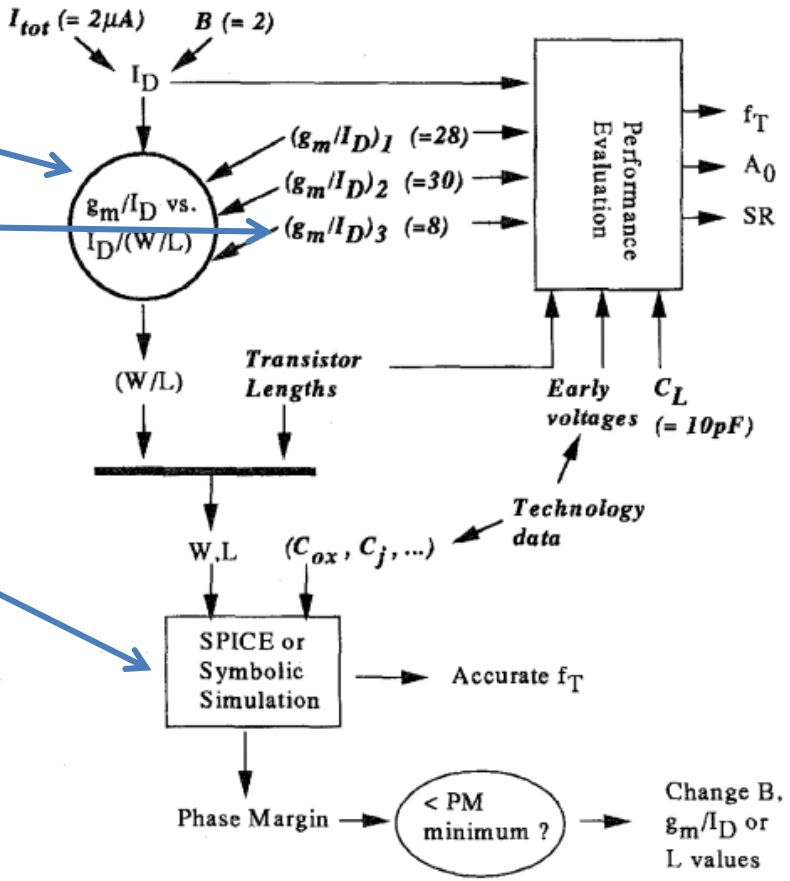
Region of operation : g_m/I_D based Methodology

The History … is the past

[Silveira, Flandre, Jespers – JSSC 1996]

- Time Consuming
- Lakes of precision (parametric set of characteristics)
- Long optimization sequence



Need for a model based approach

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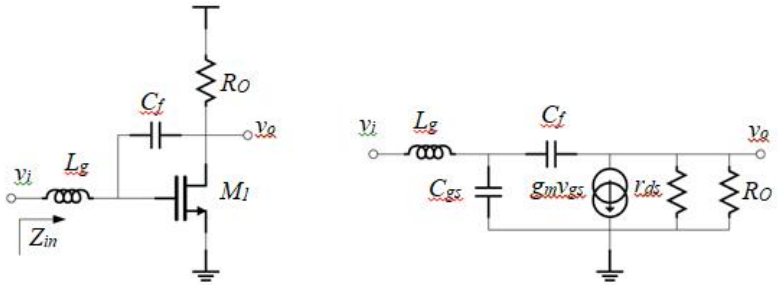
Region of operation : g_m/I_D based Methodology

Model based gm/Id methodology

[Subias – Larroze – Galup – Bourdel]



- ACM model (LCI – UFSC) [**Galup – Schneider**]

$$\frac{g_m}{I_d} = \frac{2}{n\,U_t\,(\sqrt{1+i_f}+1)}$$

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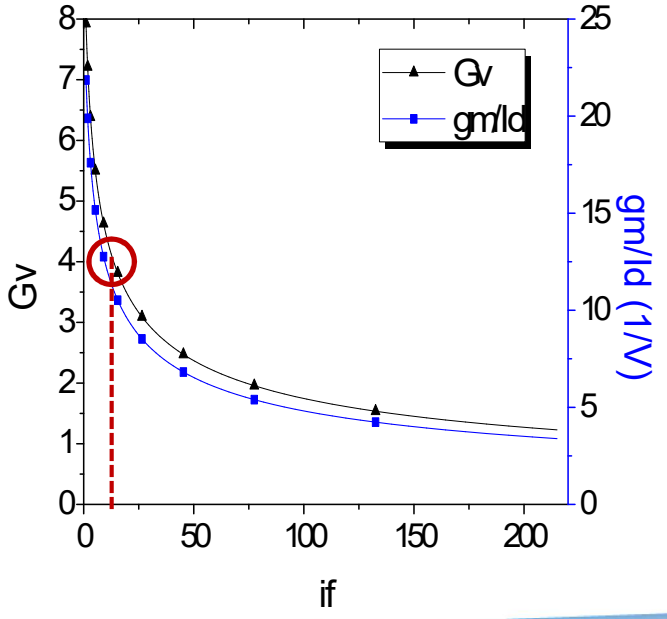
- Set of equations for Gv

$$G_{\ln a} = \frac{V_o}{V_i} = g_m * (r_{ds} \,||\, R_O) * \sqrt{1+Q_e^2}$$

For a given Vds



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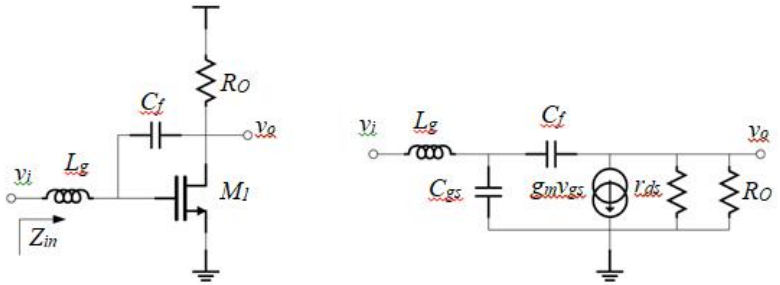
Region of operation : g_m/I_D based Methodology

Model based gm/Id methodology



- ACM model (LCI – UFSC) [**Galup – Schneider**]

$$C_{ds}(i_f) = \frac{2}{15} n\, C_{ox} \frac{\left(1 + 3\frac{1}{\sqrt{1+i_f}} + \frac{1}{1+i_f}\right)}{\left(1 + \frac{1}{\sqrt{1+i_f}}\right)^3} \frac{\left(\sqrt{1+i_f} - 1\right)}{\sqrt{1+i_f}} \frac{L^2\, g_m\, n\, U_t \left(\sqrt{1+i_f} + 1\right)}{I_{sq} i_f}$$

$$C_{db}(i_f) = \frac{K_c\, L\, g_m\, n\, U_t \left(\sqrt{1+i_f} + 1\right)}{2\, I_{sq} i_f}$$

- Set of equations for BW

$$B_w(i_f) = \frac{1}{2\pi\, R_0(i_f)\, (C_l(i_f) + C_f(i_f))}$$

$$C_f(i_f) = \frac{1}{2\pi R_0(i_f)\, BW_{max}}$$

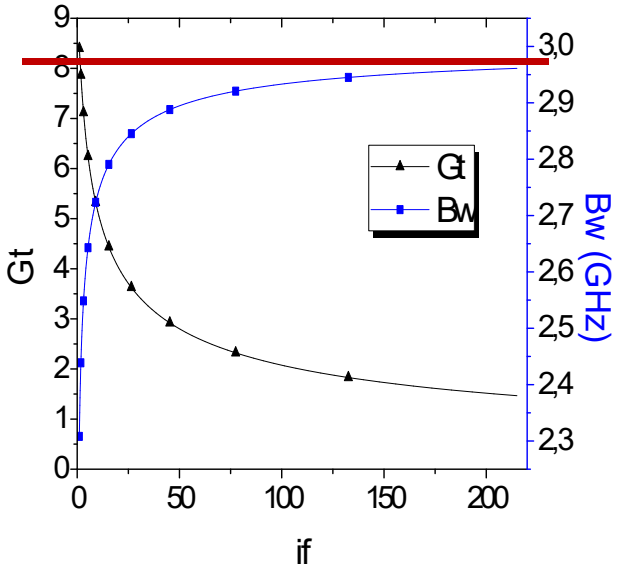
$$R_l(i_f) = \frac{V_{dd} - V_{ds}}{I_d} = \frac{2\,(V_{dd} - V_{ds})}{g_m n\, U_t \left(\sqrt{1+i_f} + 1\right)}$$

$$C_l(i_f) = C_{lo} + C_{ds}(i_f) + C_{db}(i_f)$$

BW_{max}

At this step :

- G
- BW
- if
- BW_{max}



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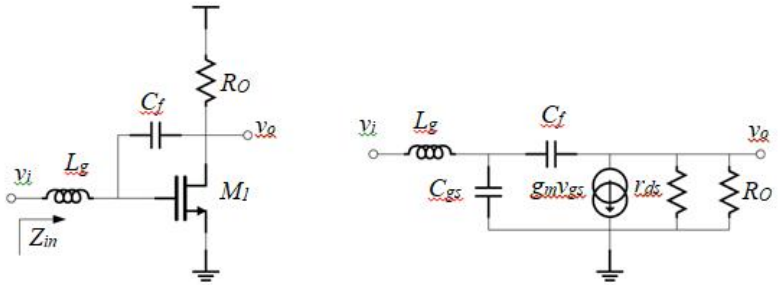
Region of operation : g_m/I_D based Methodology

Model based gm/Id methodology



- Set of equations NF

$$F = 1 + \frac{\gamma}{R_g g_m} + \frac{1}{R_g R_l \, {g_m}^2}$$

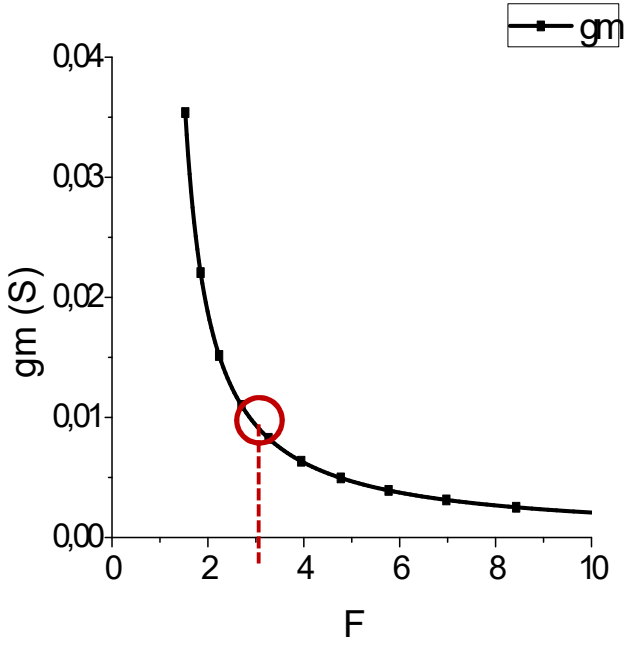
At this step :
- G (application)
- BW (application)

⇒ If

⇒ Bw_{max}

- F(application)

⇒ g_m



- g_m => I_D
- I_D => R_O for a given V_{ds}
- C_f and L_g are set to have Z_0=50Ω

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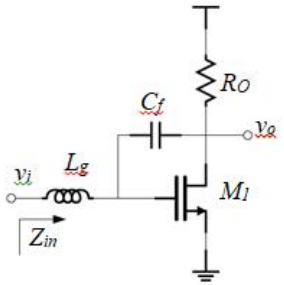
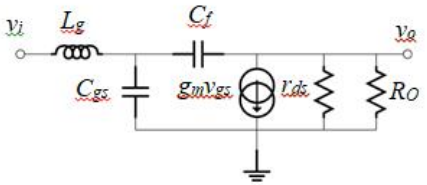
Region of operation : g_m/I_D based Methodology

Model based gm/Id methodology





	Calculus	Simualtion	
W	57.920	57.920	um
Id	497	499	µA
gm	9.9	10.3	mA/V
gm/Id	19.9	20.7	1/V
Lg	7.2		nH
Rl	1123		W
Cf	71	50	fF
Cs	131		fF
Gt	10.7	10.6	
Q	2.3	2.1	
Rin	50	55	W
F	2.3*	1.7**	
Bw	3.2	3.3	GHz

* Q=0; ** Q=2.1

High Accuracy

Low discrepancy between Analytical calculus and simulations

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System Level

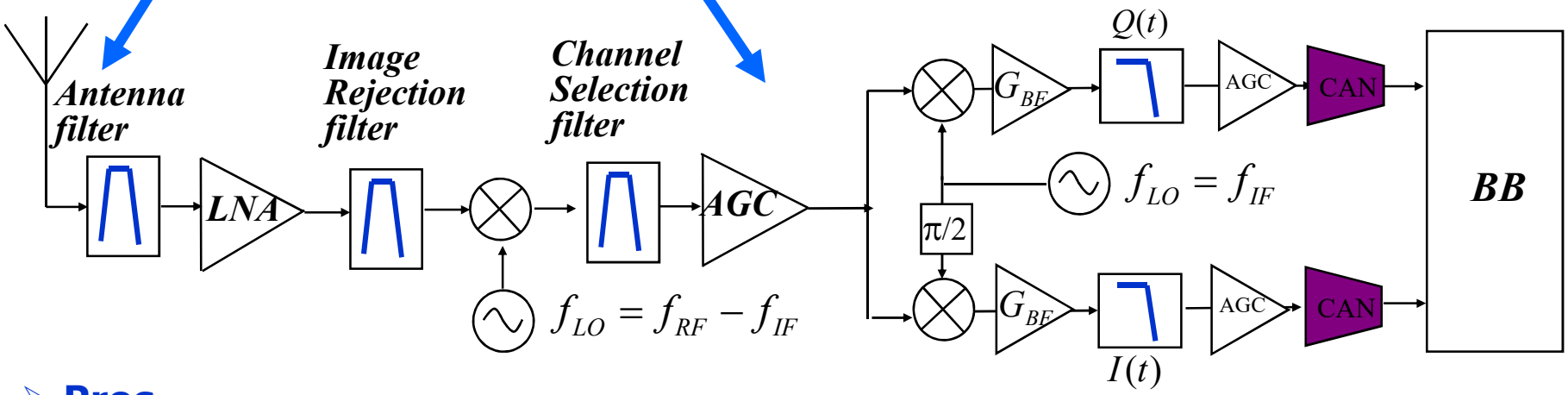
- **Rx Architectures**
  (Heterodyne / Low-IF / …)

- **Duty Cycling**
  - **RF Power Gating**
  - **Wake Up Receiver**

System Level: Heterodyne Rx

$S_{RF}(t) = I(t)\cos\omega_{RF}t + Q(t)\sin\omega_{RF}t$

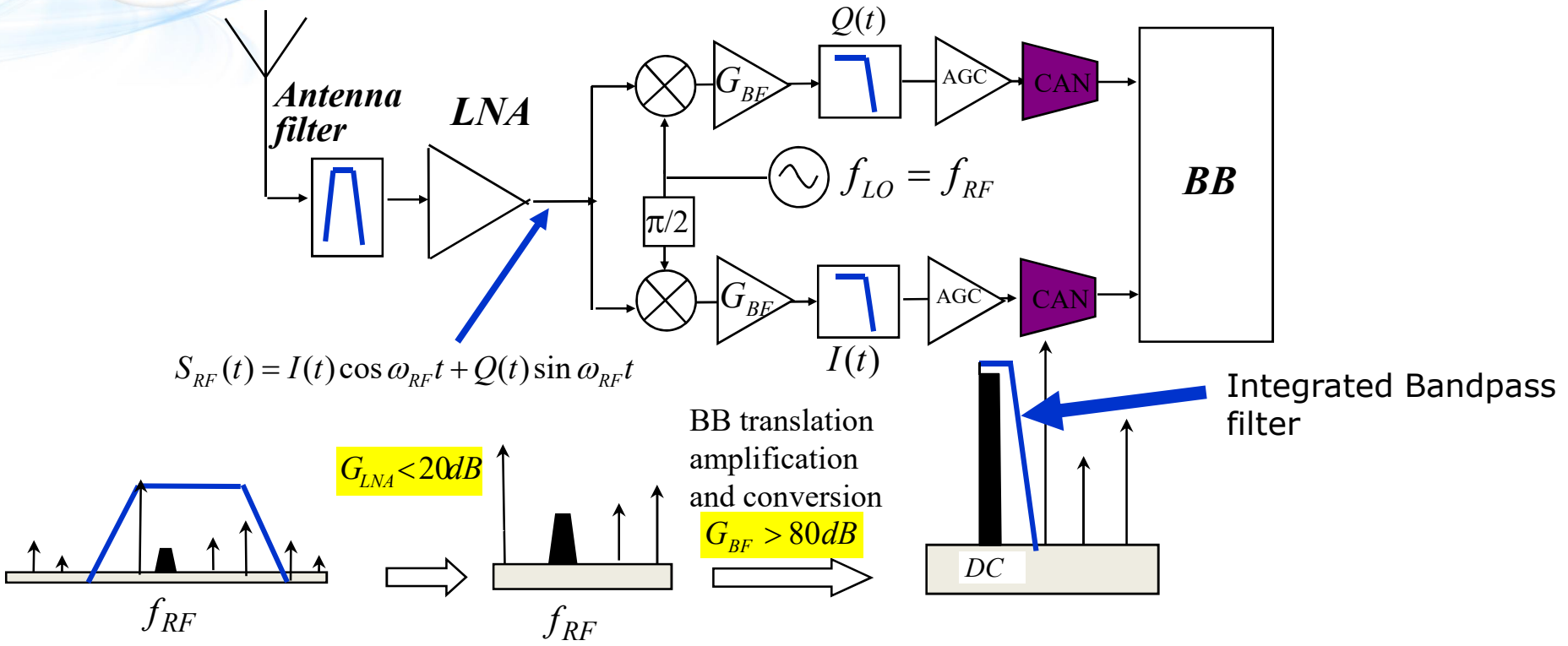
$S_{IF}(t) = I(t)\cos\omega_{IF}t + Q(t)\sin\omega_{IF}t$



- **Pros.**
  - ✓Very good tradeoff between NF and IIP3 (large dynamic): medium gain before IF and very high gain after IF filtering.
  - ✓Low sensitivity to DC coupling (high gain bandpass amplifier and DCcoupling)
  - ✓Very good tradeoff between sensitivity and selectivity
- **Cons.**
  - ✓Sensitive to image rejection (need a image filter)
  - ✓4 filtering stages: hybrid technologies (Image and IF filters are not integrated)
  - ✓High consumption (large number of stages)
  - ✓No reconfiguration (GSM+UMTS+GPS …..)

System Level: Direct Conversion

Zero-IF Structure ($F_{RF} = F_{LO}$)



Issues of this structure :

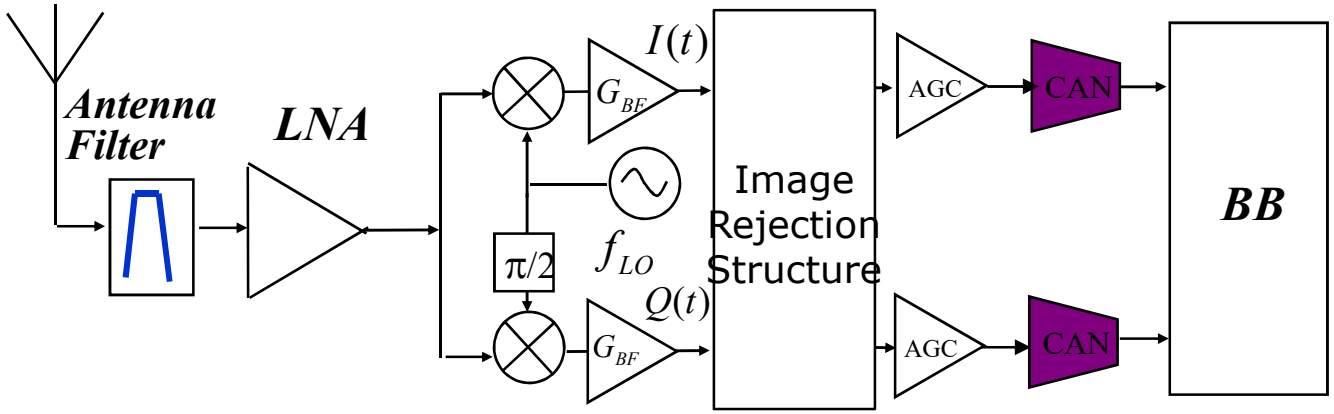
- LO leakages
- IIP2 of Mixers and BF amplifier
- 1/f noise
- No DC coupling. Active control of common mode

System Level: Direct Conversion

Low IF Structure (F_{RF} ~ F_{LO})

Good trade-off integration / performances

$$S_{RF}(t) = I(t)\cos\omega_{RF}t + Q(t)\sin\omega_{RF}t$$



Low-IF : No DC offset issue (IIP2, self-mixing, …) but it is difficult to achieve image rejection which are close to the received signal

Solution : image rejection structure with large bandwidth. The image rejection is achieved after mixing which is better for integration and multi-standard.

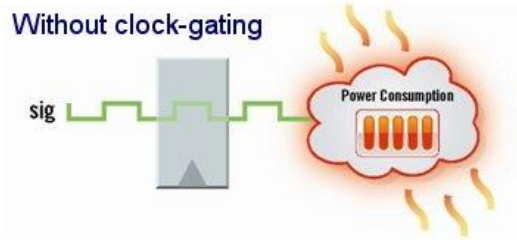
System Level

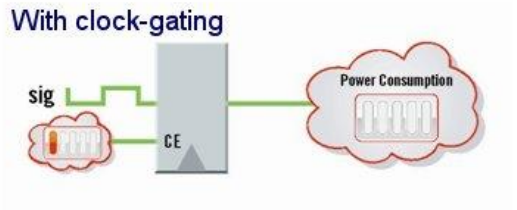
- Rx Architectures
  (Heterodyne / Low-IF / …)

- Duty Cycling
  - RF Power Gating
  - Wake Up Receiver

Duty Cycling: The Principles

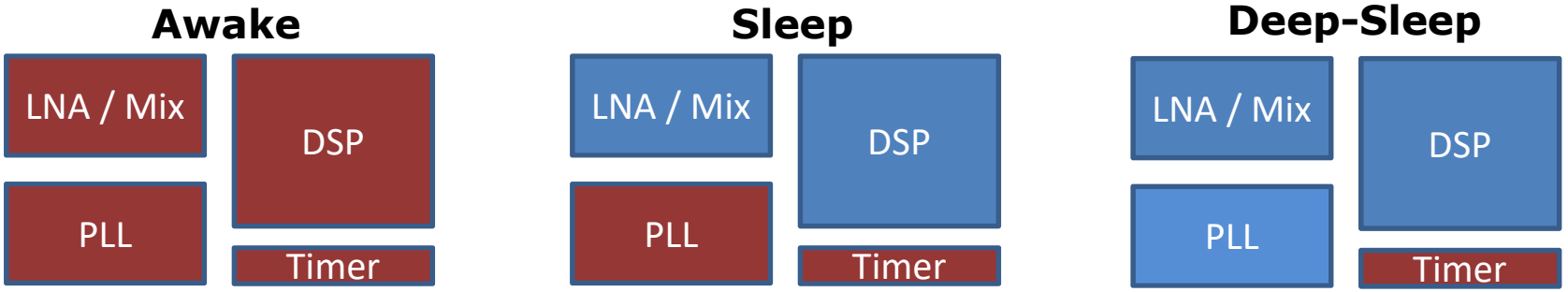
- **Power Gating**





  - Widespread Technic in Digital Design (Clock-Gating, Power Gating, …)

  - Idle Mode in Communication system
    - Several Levels (Idle, Sleep, Deep Sleep, …)
    - Idle Levels depends on the time taken to awake

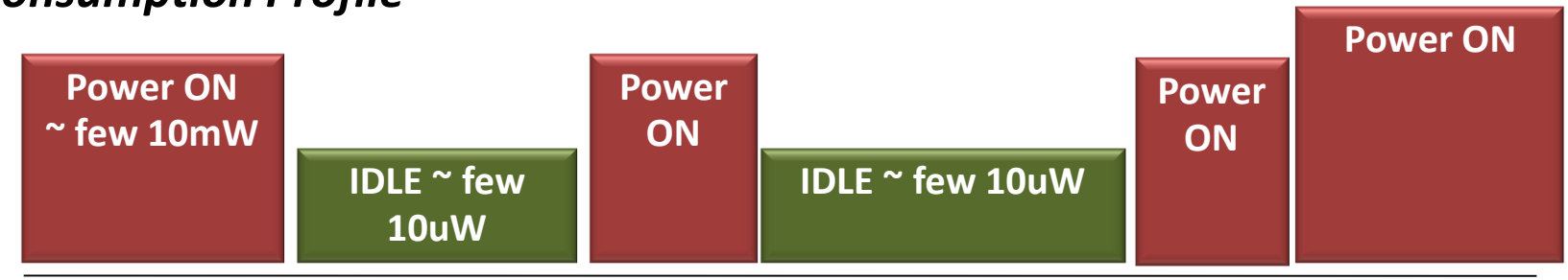


Duty Cycling: The Principles

- **Power Gating is handled by the protocol at the frame Level**

Exemple of Operating Modes

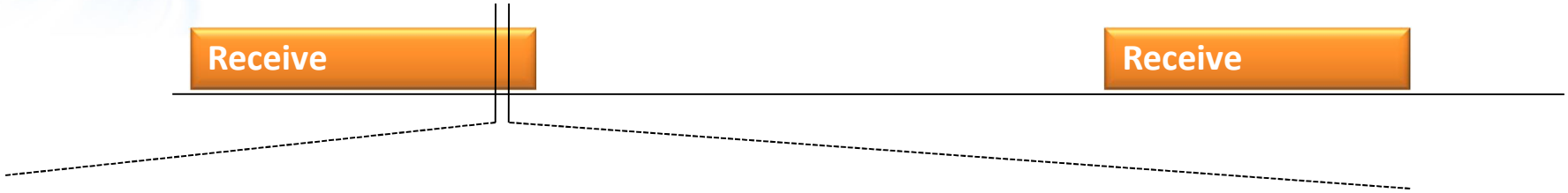
Consumption Profile



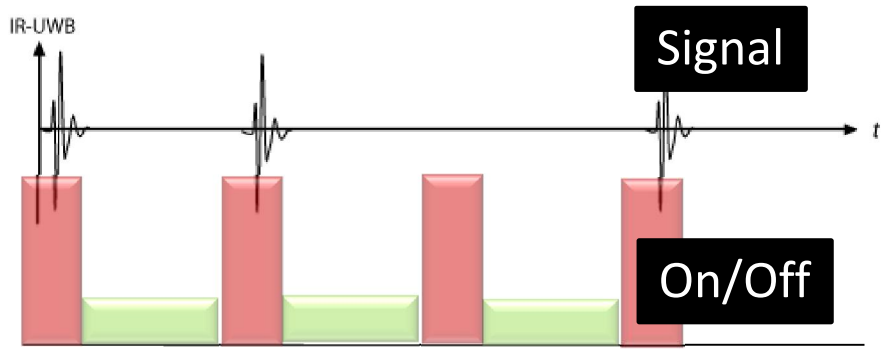
- New techniques are emerging :
  - RFPG
  - WUR

Duty Cycling: RFPG

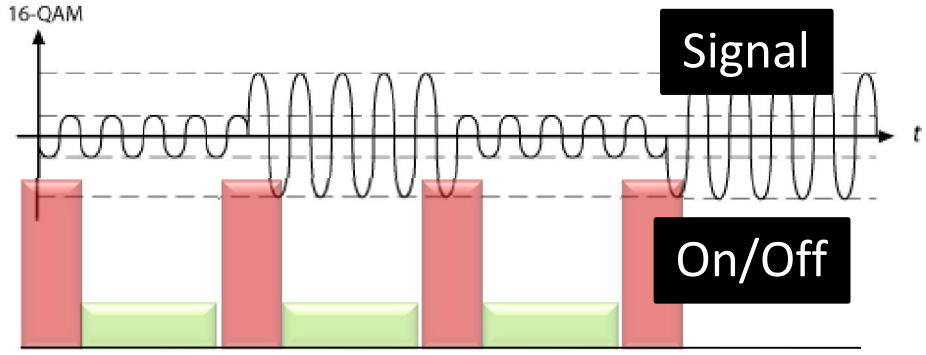
Transmission Profile at frame level



Impulse Radio - UWB

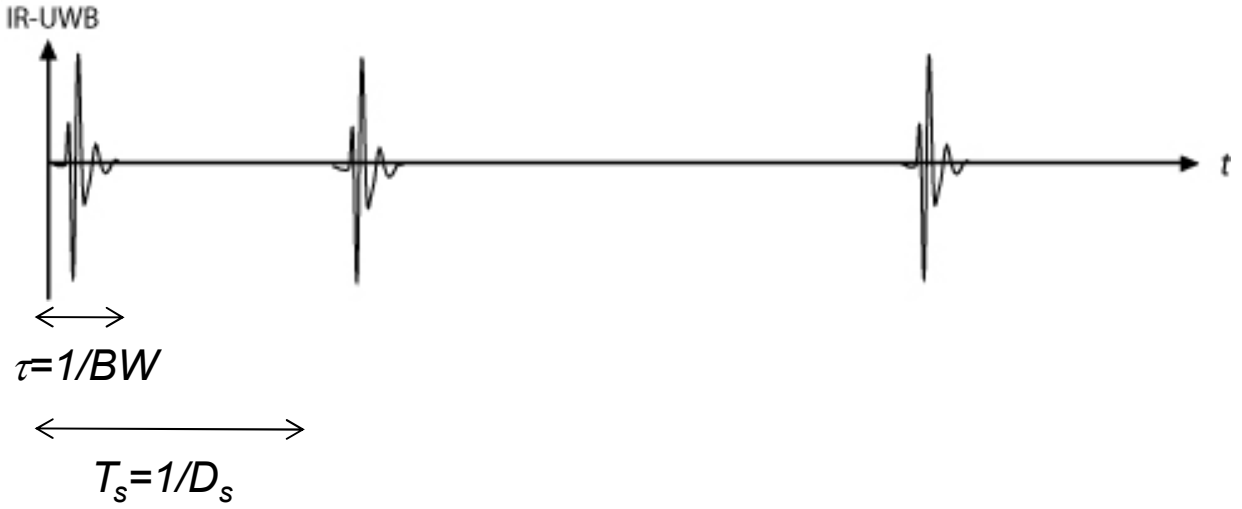


Modulated Carrier - NB



- IR-UWB :
  - No loss of information
  - Synchronisation Issues
- Narrow Band Systems :
  - Loss of information (except in OOK)
  - Non-coherent detection can solve synchronization issues

RFPG : IR_UWB



Power Gating Gain: $$\eta = \frac{T_b}{\tau} = \frac{BW}{D_s}$$

$$500MHz < BW < 5GHz$$

$$10Kbs^{-1} < D_b < 100Mbs^{-1}$$

Theoretical gain up to :
$5 .10^5$@10kbs^{-1}
50@100Mbs^{-1}

With power gating at bit level, the dependency of power consumption on the bit rate is fully exploited

RFPG : Figure Of Merit

- E_c = Nrj Consumed per bit is a the most popular FOM

$$P_{DC} = \frac{1}{T_s}\int_0^{T_s} P(t)dt = \frac{Ec}{T_s}$$

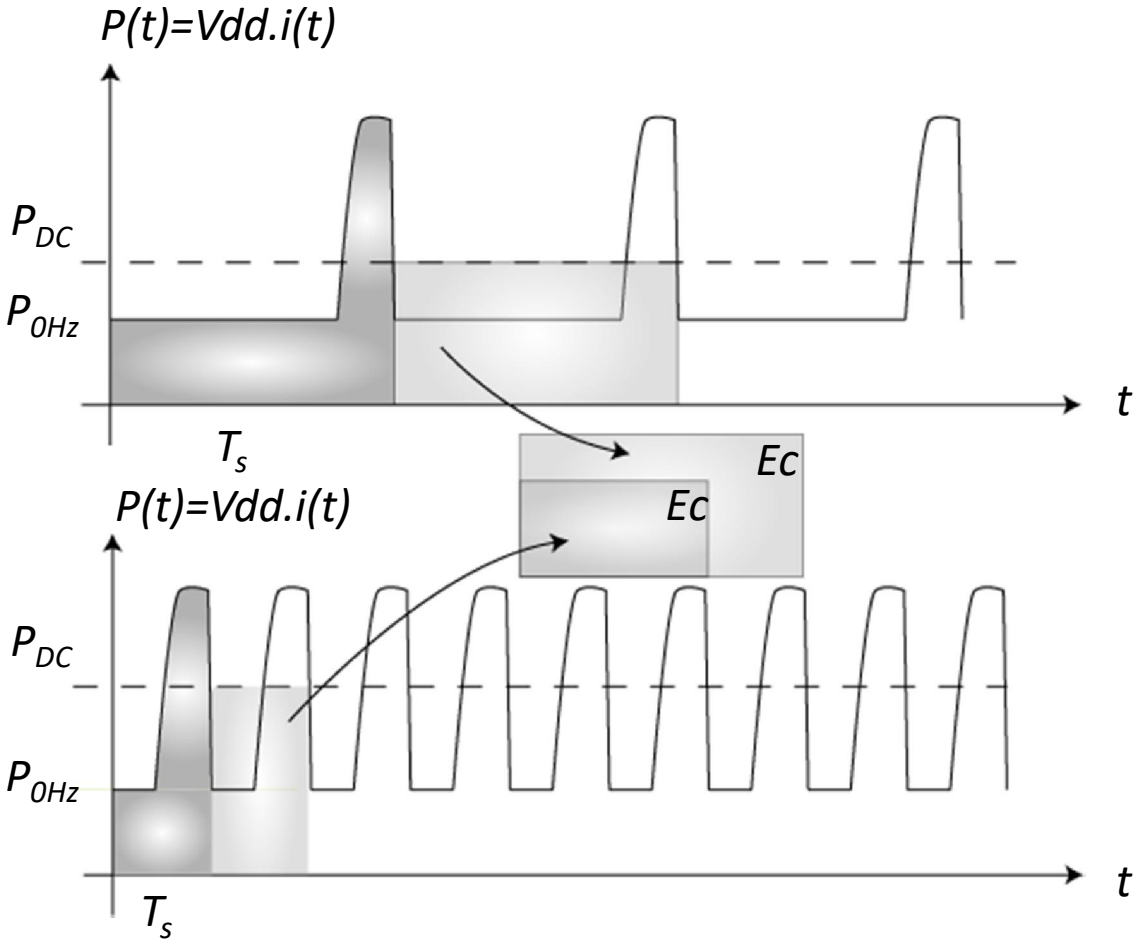
- P_{DC} increases with Ds

- Due to P_{0Hz} E_c depends on Ds

$$Ec@D_s = \left(P_{DC}@D_s\right).T_s$$

⇨ ***Valid for a given Ds***

- E_c decreases with Ds

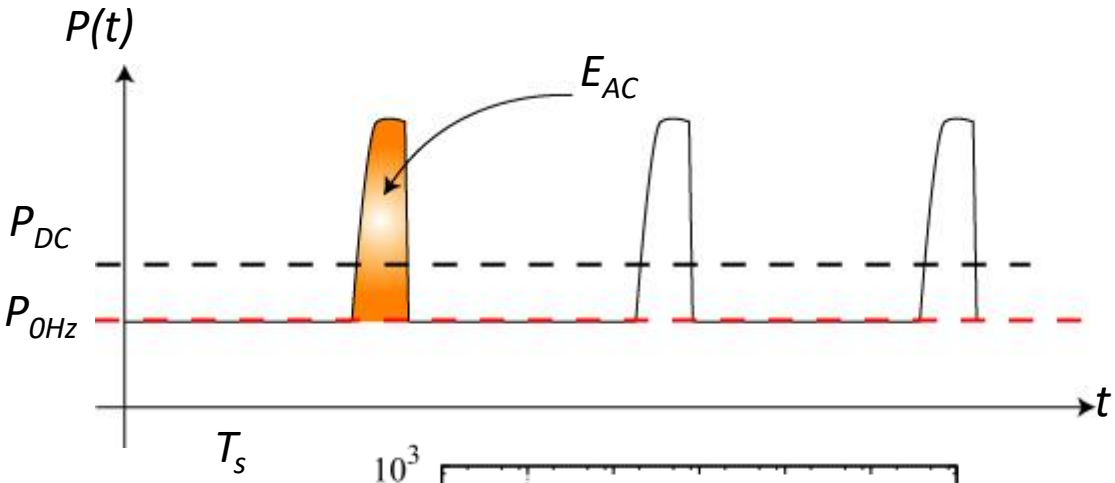


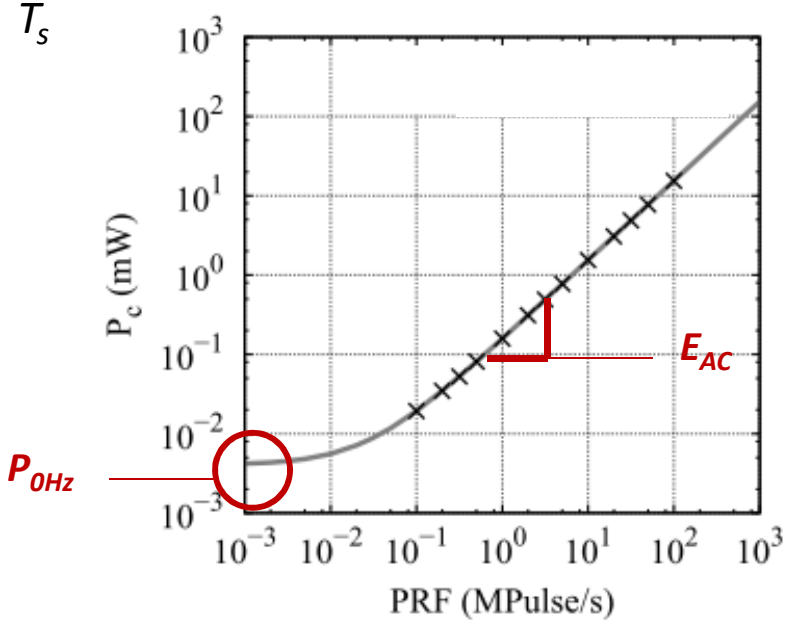
RFPG : Figure Of Merit

- E_{AC} and P_{0Hz} gives P_{DC} at any bit rates

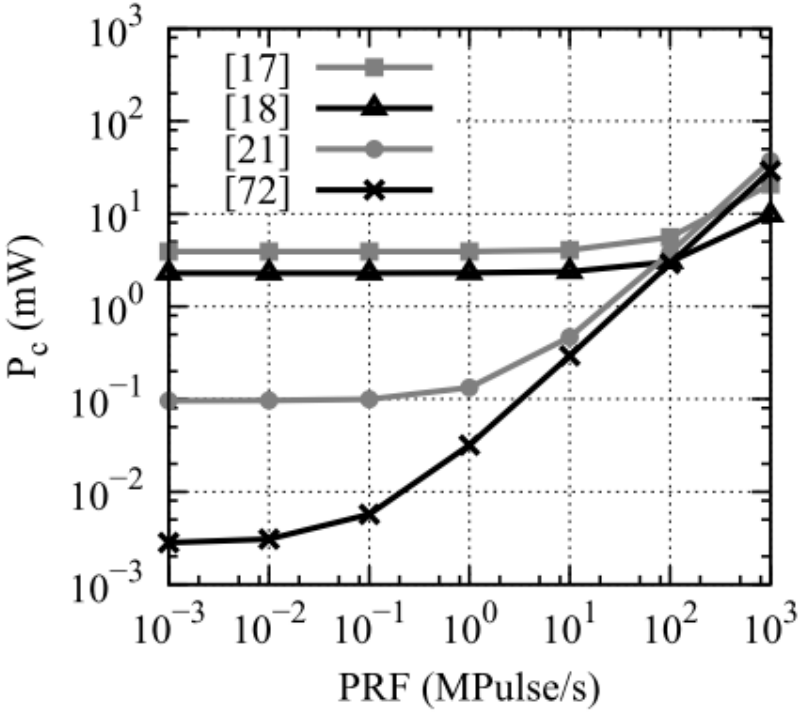
$$P_{DC} @ D_s = P_{0\mathrm{Hz}} + E_{AC}.D_s$$

- E_{AC} is invariant with Ds
- P_{0Hz} is invariant with Ds
- Allows comparison
- E_{AC} and P_{0Hz} can be obtained from measurement





Optimisation strategies on TX side



[18] : Bourdel – MTT 2009 – MCML – Filter Excitation
P_{0Hz}=2,3mW; E_{AC}=2,5pJ

[21] : Wentzlof – ISSC 2007 - CMOS – OL switching
P_{0Hz}=96uW; E_{AC}=37pJ

[72] : Dokania – ISLPED 2010 - CMOS – OL switching with Power Manager
P_{0Hz}=2,8uW; E_{AC}=29pJ

- At low rate, the P_{0Hz} must be minimized.
  Efficient power gating is needed.

FD-SOI

- At High rate, the E_{AC} must be minimized.
  Power gating is not decisive.
  Differential Mode and short conduction time are needed

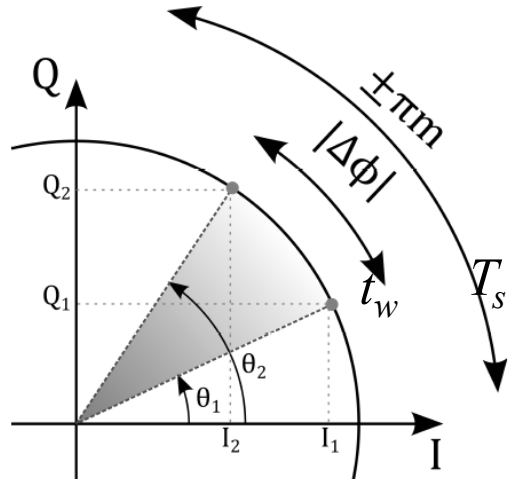
RFPG : Narrow Band

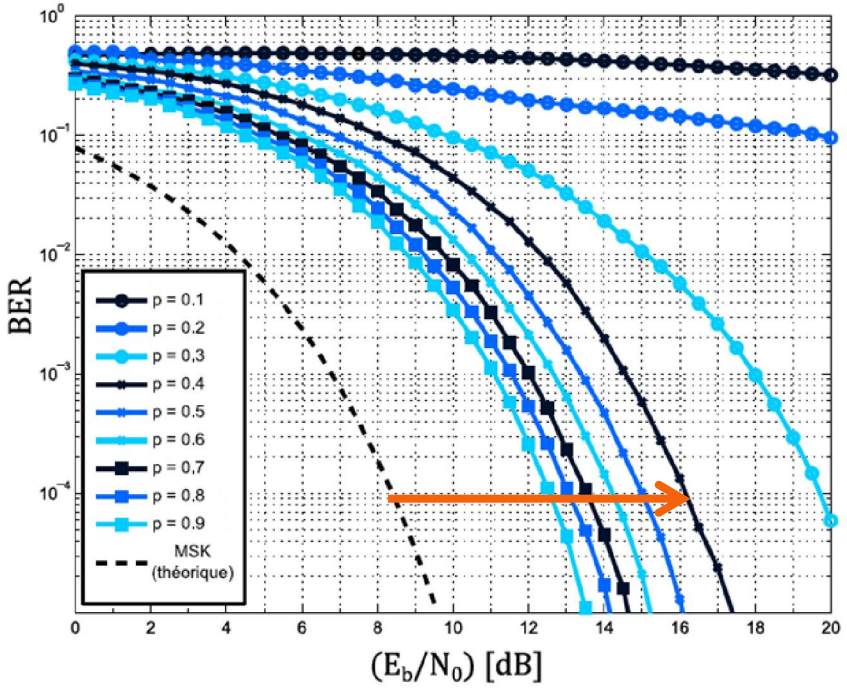
Principle [*J.F. Pons, IEEE TVLSI 2015*] **:**

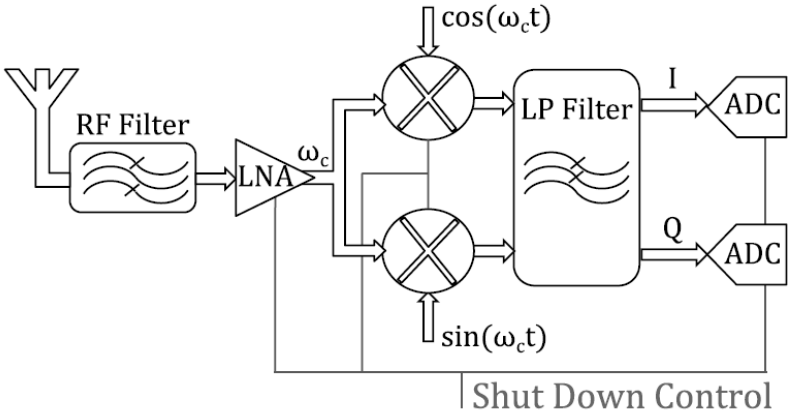
- FSK Modulation
- Maximum Active Power Ratio (p) :
- Maximum RF Power Reduction : 1-p
- Simple estimator :

$$p = \frac{t_w}{T_s} = \frac{|\Delta\varphi|}{\pi m}$$

$$d_i = \begin{cases} 1, & \text{if } \left(\frac{d\varphi}{dt}\right) > 0 \\ 0, & \text{if } \left(\frac{d\varphi}{dt}\right) \leq 0 \end{cases}$$







60% Power reduction
If we have +8dB in SNR

RFPG : Narrow Band

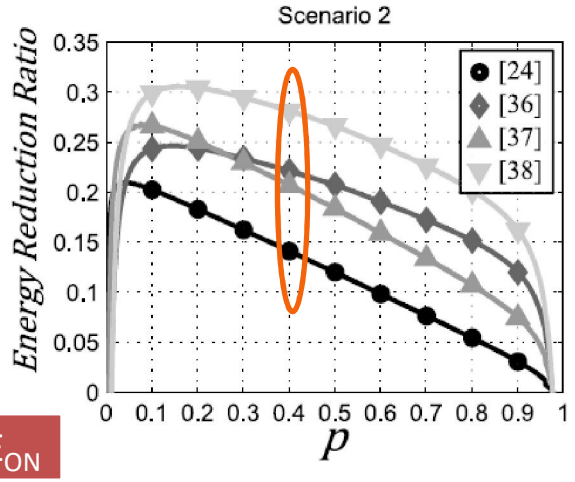
Power Consumption Reduction :

- Asynchronous RFPG
- Analog Power Reduction
- Digital Power Increase (90nm)
- Bluetooth standard

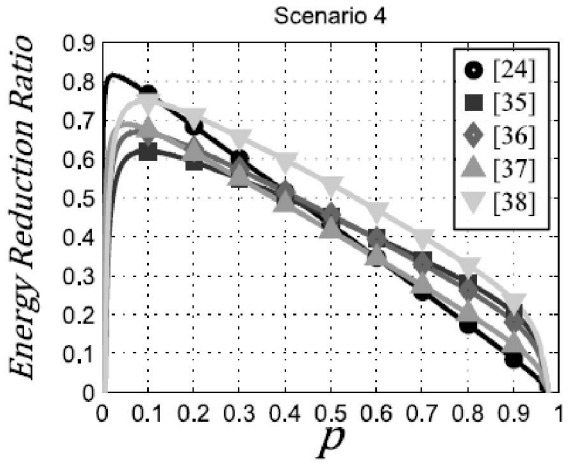
[*J.F. Pons, IEEE TVLSI 2015*]

Ref.	Technology	Consumption (mW)	Conditions
[24]	N/A	PLL : 135 LNA : 20 Mixer : 42 Filters : 5 Baseband Amp. : 5 ADC : 5.85 Other : 0.5	N/A
[36]	CMOS 90 nm	PLL : 0.915 RF analog : 0.39 Baseband analog : 0.048 Baseband digital : 0.166	OOK @ 1 Mbps VDD : 1/1.2 V
[37]	CMOS 90 nm	PLL : 1.7 LNA/RF Mixer : 1.25 IF Mixer : 0.35 LP Filter/ADC : 0.4 Other : 0.1	Bluetooth-LE IEEE 802.15.4 IEEE 802.15.6 VDD : 1.2 V
[38]	CMOS 65 nm	PLL : 3.96 LNA/Amp. : 0.95 ADC : 2.34	Bluetooth-LE IEEE 802.15.4 VDD : 1.3/3 V

Case	PLL ON-OFF	$t_{\uparrow,i}(=t_{\downarrow,i})$	Description
1	No	0	Intermediate
2	No	10 ns	Realistic
3	No	125 ns	Not adapted
4	Yes	10 ns	Ideal

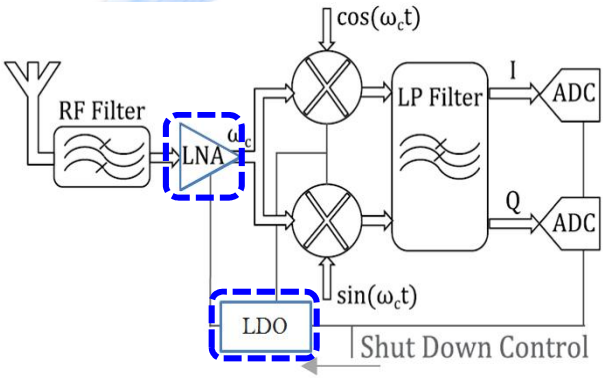


ERP=1-E_{Ts}/E_{ON}



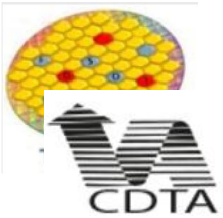
RFPG : Narrow Band

LNA and LDO for ZigBee in FDSOI

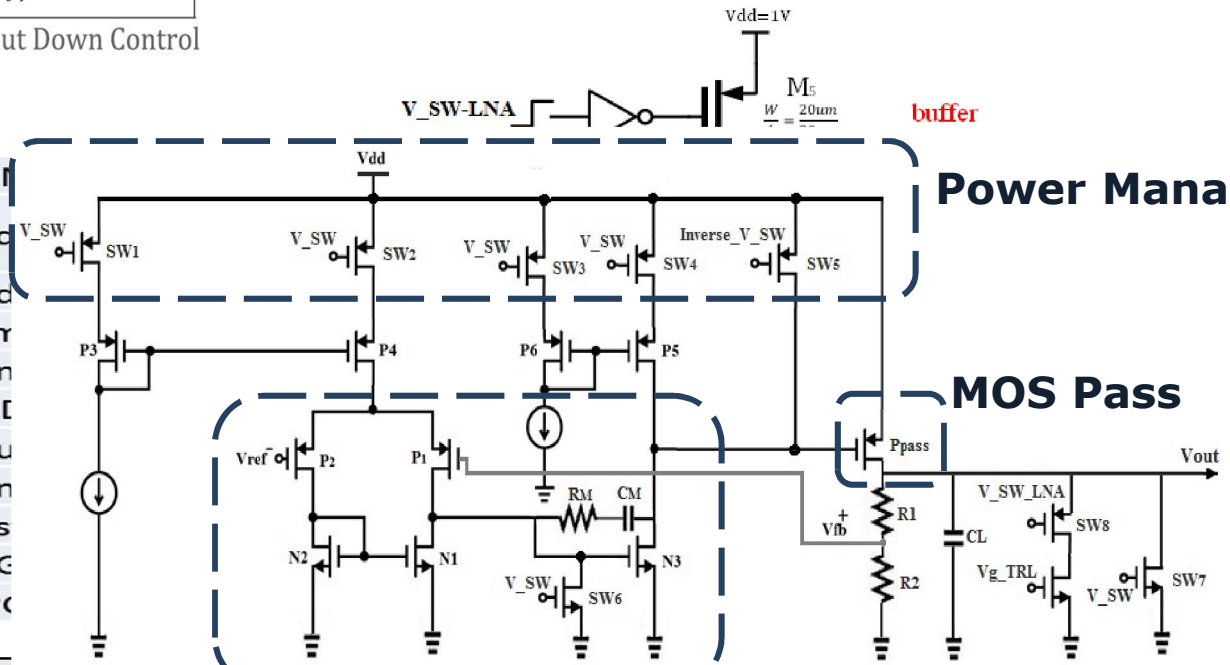


[PHD Jing-Liu]

[PHD Kader Taibi]



	LN
Voltage Gain	(d
NF	(d
ION	m
IOFF	n
	LD
ION	u
IOFF	n
	Sys
Pcons	(RFPC
Pcons	(RFPC



Ton = 35ns for Tb=1us in ZigBee

System Level

- **Rx Architectures**
  (Heterodyne / Low-IF / …)

- **Duty Cycling**
  - **RF Power Gating**
  - **Wake Up Receiver**

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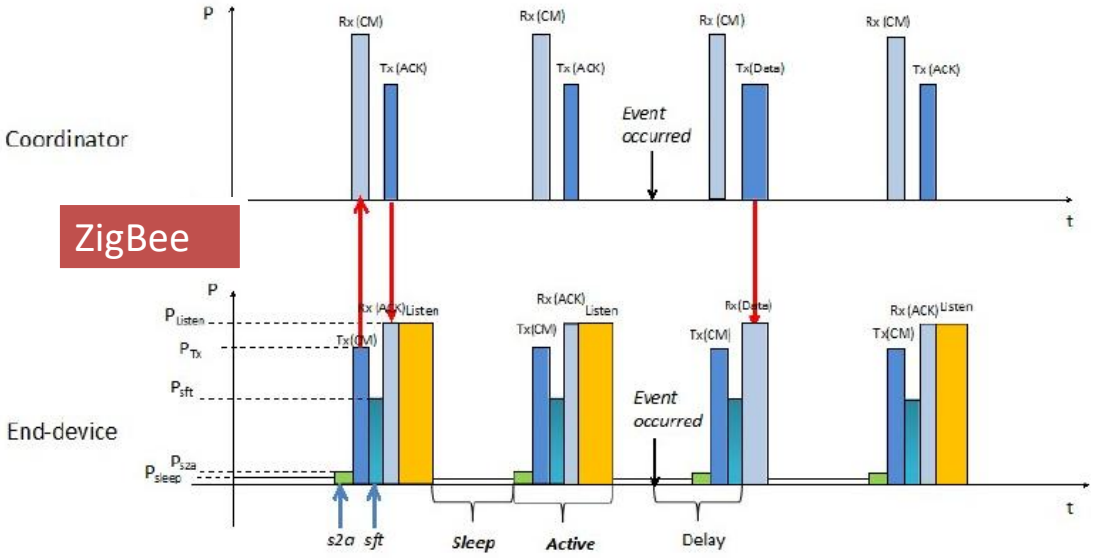
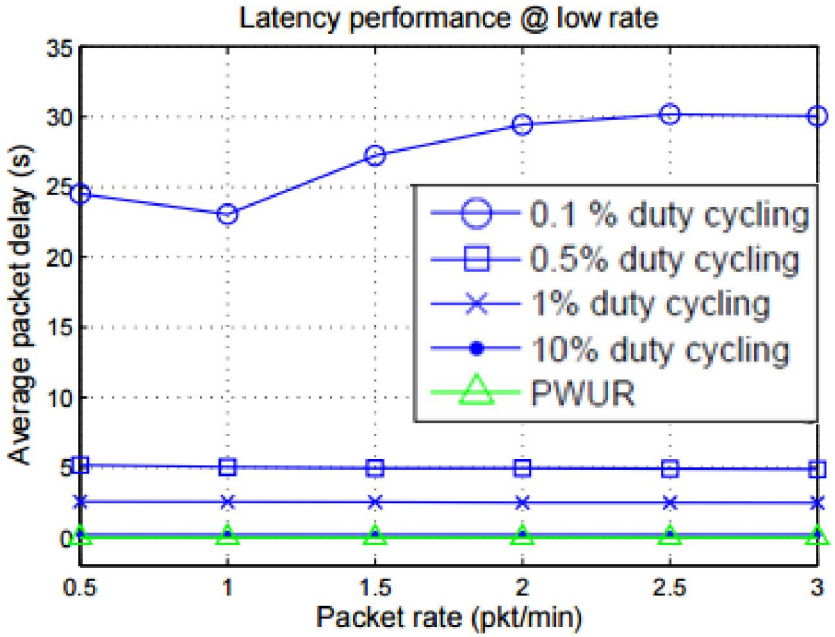
Duty Cycling: Wake Up Radio

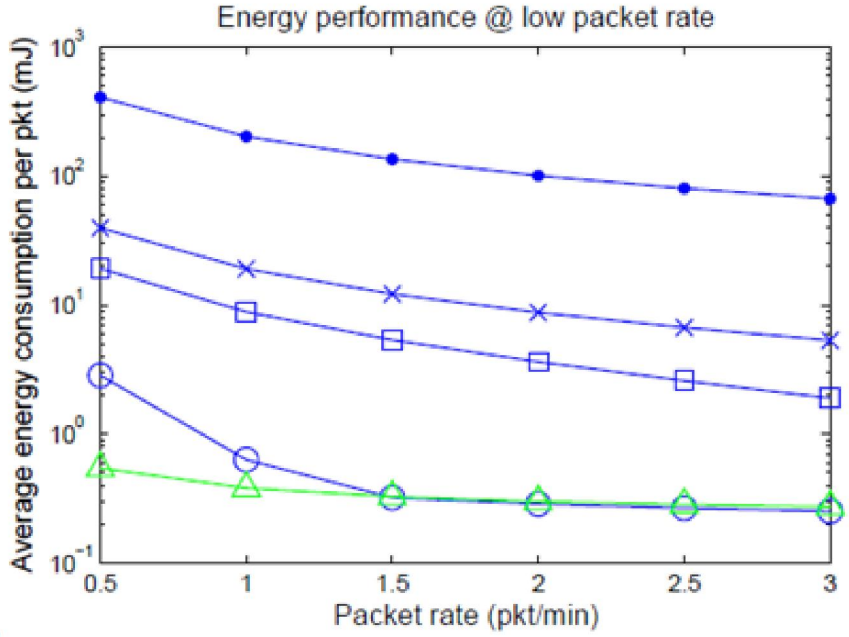
Wireless Sensor Network :

- Duty Cycled Communication
  - ⇓ Power Consumption
  - ⇑ Latency

[L. Huo "A Comprehensive Study of Passive Wake-up Radio in Wireless Sensor Networks"; Delft Univ. of Technol-2014]







Duty Cycling: Wake Up Radio

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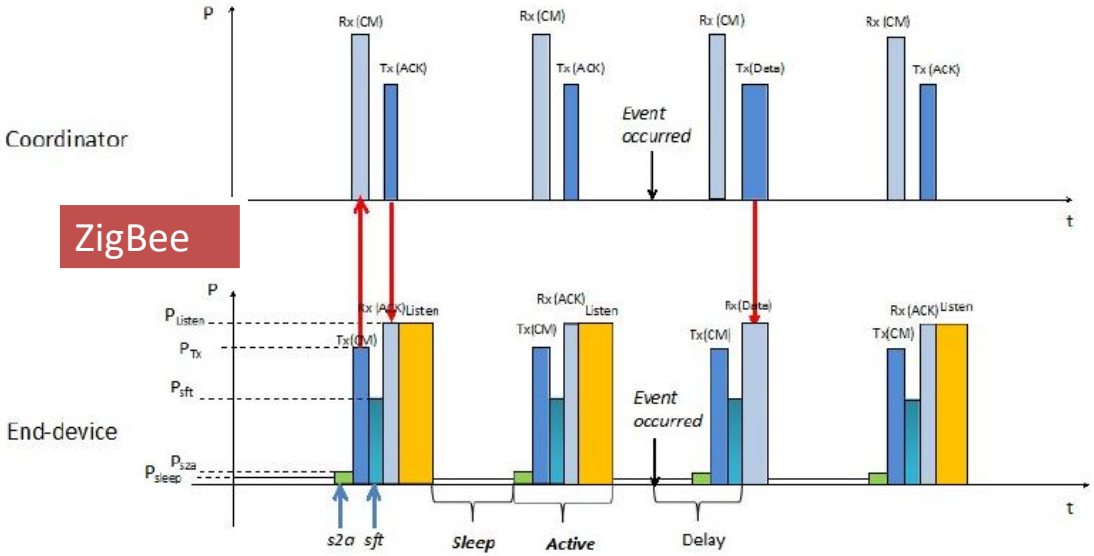
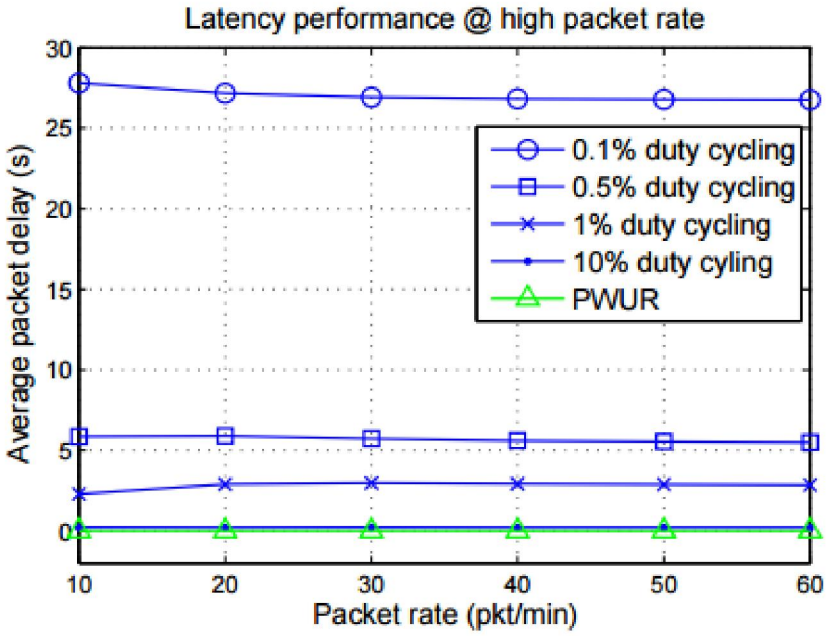
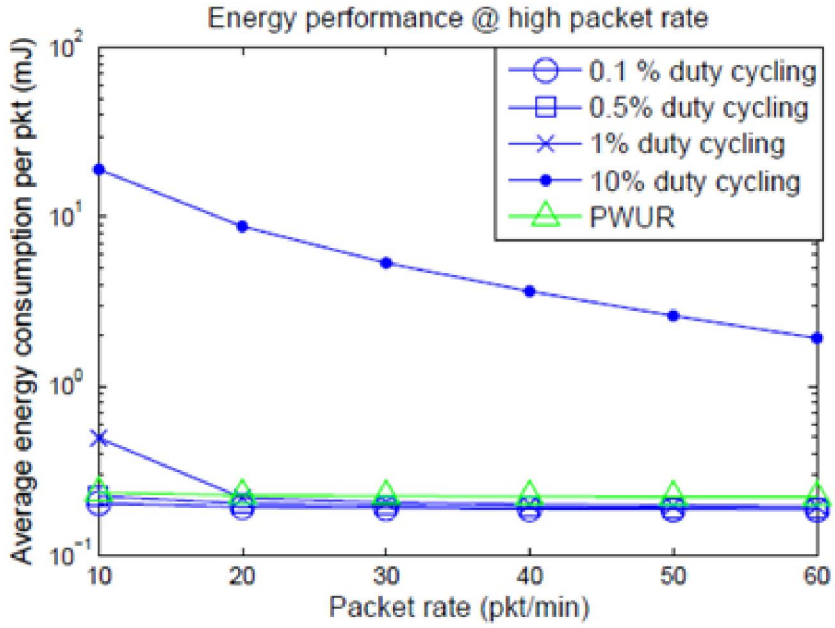






Duty Cycling: Wake Up Radio

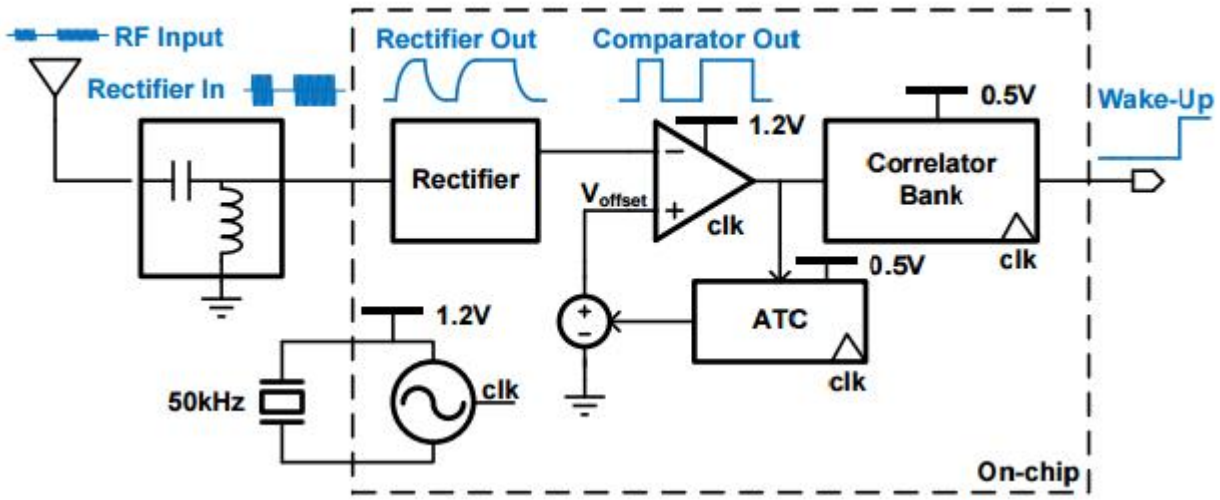
WUR Issues :

- Power consumption (few micro Watts)
- Sensitivity <-40dBm (6m range @400MHz with Pe=0dBm)
- Blocker rejection

Design solution :

- Rectifier based solution
- Correlation code for ID
- Tunable threshold for blocker rejection

=> High blocker sensitivity



-45 to -41 dBm, 116nW

[Seunghyun Oh, Nathan E. Roberts, and David D. Wentzloff, " A 116nW Multi-Band Wake-Up Receiver with 31- bit Correlator and Interference Rejection" IEEE CICC 2013]

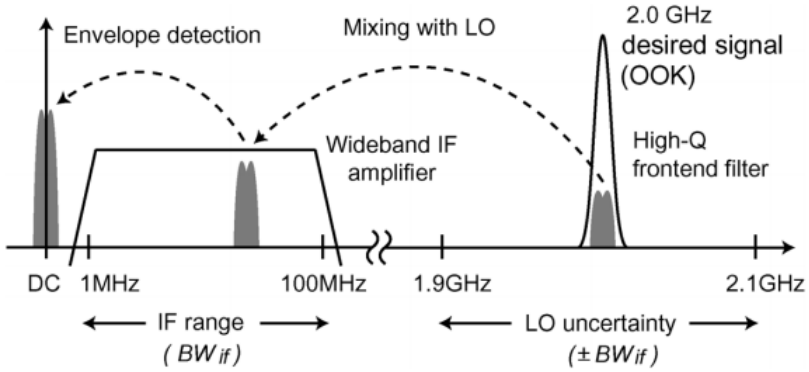
Duty Cycling: Wake Up Radio

WUR Issues :

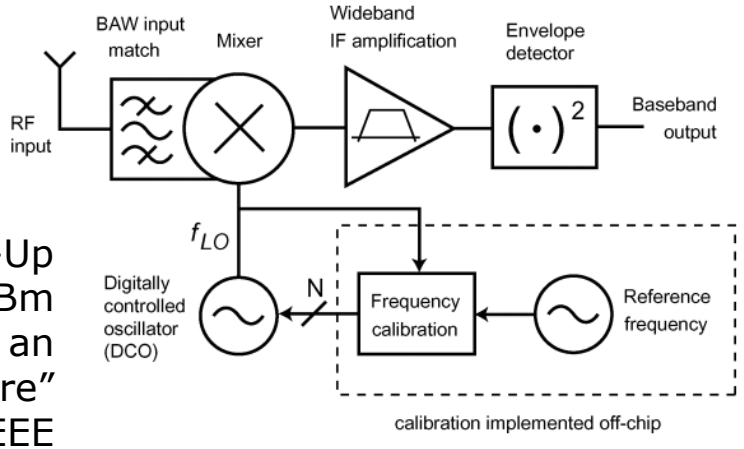
- Power consumption (few micro Watts)
- Sensitivity <-40dBm (6m range @400MHz with Pe=0dBm)
- Blocker rejection

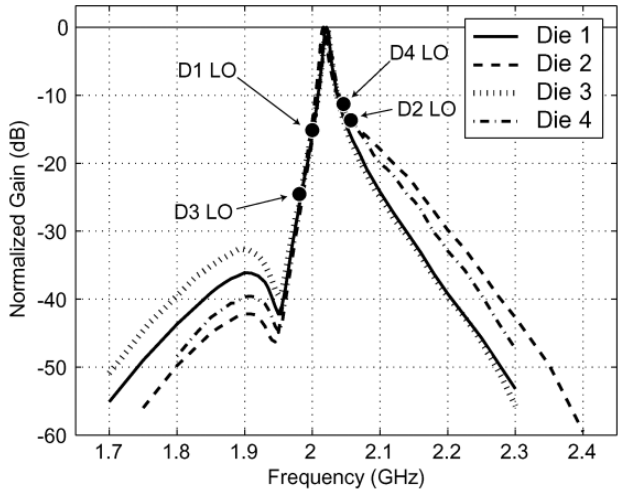
Design solution :

- Uncertain IF based solution
- Mixer and free runing VCO
- Calibration needed



-72 dBm, 52uW





["A 52 uW Wake-Up Receiver With 72 dBm Sensitivity Using an Uncertain-IF Architecture" N. M. Pletcher *et Al*, IEEE – JSSC - 2009]

SUMMARY

- Introduction
- Technological Level
  - Digital Functions
  - Analog Functions
- Electrical Level (Bloc Design)
  - Subthreshold technics
  - LNA design
- System Level
  - Direct Conversion
  - Duty Cycling
- Concluding remarks

Concluding Remarks

Several Levels

- Technological
- Electrical
- System
- Protocol

What is the best approach ? => Concurrent Approach

Several Technics more or less suited to FDSOI

- Subthreshold
- Duty-cycling

FD-SOI